ASCENT+ European Infrastructure for Nanoelectronics: a Deep Dive to All-GaN IC Technology for Power Electronics

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I. INTRODUCTION

ASCENT+ brings together 15 partners to foster the nanoelectronics community, integrating a unique research infrastructure with unprecedented credentials. ASCENT+ serves as a direct entry point to key enabling capabilities in state-of-the-art processing, modelling and simulation data sets, metrology and characterization, and devices and test structures. Focus areas include: Quantum advantage using solid-state platforms; Low-power, energy-efficient, high-performance computing based on disruptive devices; Increased functionality through advanced integration of a diverse range of materials and innovative technologies. The ASCENT+ program offers free-of-charge access to world-leading infrastructure empowering users to make advances in nanoelectronics. Below, we take a deep dive into the GaN IC offer by Imec for power electronics.

II. IMEC OFFER: ALL-GAN GANIC TECHNOLOGY

Discrete GaN devices today dominate the GaN market either as Off-the-shell components or customized designs through foundry technology. Furthermore, to unlock the full potential for fast switching GaN technology in high power application, monolithic integration is crucial. For instance, integration reduces the parasitic between the driver and the power devices or between the two power devices and a half bridge (HB) at the switching node etc. It helps to reduce ringing, switching loss which in-turn makes a smooth highly efficient circuit. Moreover, GANIC provides a faster, smaller, lighter, and more cost-effective solution compared to its other silicon alternatives. However, this monolithic integration in GaN technology faces some technological and circuit level challenges. One of the those is back-gating effect (BGE) that makes monolithic integration of half-bridge (HB) switches very difficult, in which two devices are connected in a single substrate and source of both devices are not in a same potential. This effect highly impacts the performance of the high-side switch.

As a potential solution we propose to implement it on GaNon-SOI with trench isolation to fully isolate the HEMTs as well as their respective silicon device layers that are cut off Giorgos Fagas Tyndall National Institute University College Cork Cork, Ireland georgios.fagas@tyndall.ie

horizontally by a trench. It means for a HB on SOI with deep trench isolation, the buried oxide, and the oxide field trench, isolate the HS switch galvanic from the LS devices, and from the Si substrate. The local deep Si contact connecting the source of each device to the thin Si layer which is the top of the original SOI substrate guarantees that the source-bulk potential is zero. This technology is capable to eliminate the BGE completely. Besides, p-GaN HEMTs passive components are also integrated and that can be used to make integrated circuits. An example of a HB switch with integrated driver is shown in *Fig. 1* [1].

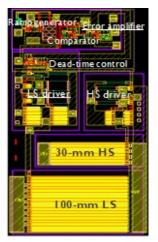


Figure 1: Layout of HB switch with integrated drivers

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References

 X. Li, N. Amirifar et al., "GaN-on-SOI : monolithically integrated All-GaN ICs for power conversion," IEEE IEDM, San Francisco, CA, USA, December 2019.