# Reliability of Mo as Word Line Metal in 3D NAND

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***Abstract*— We evaluate the reliability of Mo as word line metal for 3-D NAND Flash devices, by mimicking the stacked architecture using planar capacitors with $SiO_2/Al_2O_3$ and $SiO_2/HfO_2$ dielectric stacks. By combining TDDB and TVS measurements with simulations, we show that Mo does not drift in the two examined stacks. Moreover, our study highlights the importance of controlling the defectivity at the $SiO_2$/high-k interface and within the high-k to avoid the risk of early dielectric breakdown.**

***Index Terms* - Flash, metal drift, Mo, TDDB, word line.**

## I. Introduction

3-D architecture has become the de facto standard for NAND Flash memory devices to further increase memory density beyond the intrinsic limits of planar technology and keep lowering the price per bit [1]. Nowadays, the industrial standard for 3-D NAND relies on silicon-oxide-nitride-oxide-silicon (SONOS) memory devices [2], that are charge trapping-based devices, consisting of cylindrically shaped NAND strings with a macaroni polycrystalline Si channel and horizontal Word Lines (WLs). To ensure acceptable erase and write operations, 3-D NAND memory cells exploit a combination of High-K (HK) dielectrics (e.g., $Al_2O_3$, $HfO_2$) and Metal Gates (MG) with high work functions [3]. Both characteristics are instrumental in delaying the onset of electron injection from the gate, i.e., the electrons from the gate tunneling into the charge-trap layer. Current technology uses W in combination with a TiN liner/barrier. Although it is desirable to stack more and more WLs on top of each other to further increase the memory density, such an approach presents several challenges to the functionality and reliability of the memory cells. On the one hand, in order to minimize the mechanical stress on the individual devices, which is detrimental for their functionality, it is necessary to reduce the thickness of both the metal WLs and the dielectrics to limit the overall stack height [4]. On the other hand, reducing the thickness of the metal films increases the WL resistance and the risk of device failure, resulting in less performing and less reliable memory cells. A possible solution to this issue is contingent on replacing the W/TiN system with alternative metals such as Ru and Mo [5]-[9]. In fact, the resistivity of W, as well as other metals currently used in semiconductor technology, is strongly affected by surface scattering and thus is very sensitive to the thickness of the metal film. In addition, to ensure its functionality as adhesion layer, the TiN liner/barrier cannot be scaled together the W thickness, resulting in a larger fraction of the WL filled with a poorly conductive material, hence increasing its contribution to the overall line resistance. On the contrary, studies on alternative metals have shown that they are a valid replacement to conventional metals at ultra-scaled dimensions, showing lower resistivity values [5], [8] and no reliability issues even when a very thin barrier was used [9]. In fact, because of their high cohesive energy, alternative metals are expected to not easily ionize and drift into dielectrics; hence they can be used barrierless or require only a very thin adhesion layer [7]. In this work we focus on Mo as a potential candidate for WL metal since it has been shown that it can be used without a barrier on various back-end- and middle-of-line dielectrics [10]. In particular we evaluate the WL-to-WL reliability, assessing the risk of metal drift-induced failure in $SiO_2/Al_2O_3$/Mo and $SiO_2/HfO_2$/Mo systems, as schematized in Fig. 1a.

## II. Experimental Procedure

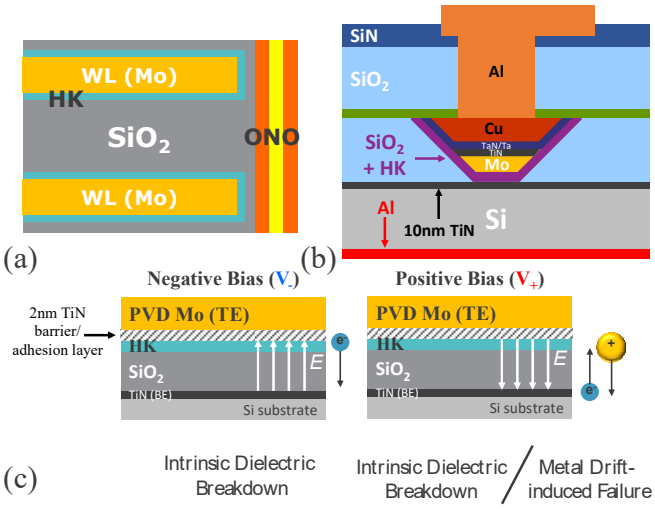


Figure 1. (a) Schematic of a 3-D NAND Flash memory showing two adjacent word lines (WL) (b) Schematic of the test vehicle (p-cap). The TaN/Ta barrier is needed to prevent Cu from drifting through the TE and into the dielectrics. (c) Different failure mechanisms can be induced depending on the polarity of the stress voltage. The black oblique lines indicate the 2nm-thick TiN barrier layer that is present in some of the samples (see Table I).

### A. Test Vehicle

The 3-D NAND Flash architecture was mimicked using 100µm x 100µm planar capacitors (p-caps) [11] (Fig. 1b). As depicted in Fig. 1c, because of the asymmetric design of the test vehicle, different failure mechanisms can be induced depending on the polarity of the stress voltage applied to the Mo top electrode (TE). A 10nm-thick TiN layer is used for the bottom electrode (BE), which is inert and not susceptible to metal drift. The 5nm-thick Mo TE is deposited by PVD and capped with a 10nm-thick TiN layer; after depositing an additional 4nm TaN/Ta barrier, the rest of the via is filled with Cu. The normal failure mode for p-caps is intrinsic dielectric breakdown; however, if mobile metal ions ($Mo^{+2}$) form and accumulate at the TE/dielectric interface, metal drift-induced

Table I. – Detailed list of the samples used in this study. The 20nm-thick $SiO_2$ layer was deposited by PE- ALD. The first entry in the list (*) is the reference wafer, fabricated with the main purpose of evaluating the impact of integration on the PE-ALD $SiO_2$. Note that a Cu metallization, with a thick TaN/Ta barrier, was used for this wafer instead of PVD Mo.

| *Oxide* | *High-k* | *Post-deposition Annealing* | *Barrier between Mo and the dielectrics* |
|---|---|---|---|
| 20nm $SiO_2$ | No HK | / | 4nm TaN/Ta + Cu (*) |
| 20nm $SiO_2$ | No HK | / | No Barrier |
| 20nm $SiO_2$ | 1nm $Al_2O_3$ | 1050°C 2min | No Barrier |
| 20nm $SiO_2$ | 1nm $Al_2O_3$ | 1050°C 2min | 2nm TiN |
| 20nm $SiO_2$ | 2nm $Al_2O_3$ | 1050°C 2min | No Barrier |
| 20nm $SiO_2$ | 2nm $Al_2O_3$ | 1050°C 2min | 2nm TiN |
| 20nm $SiO_2$ | 2nm $Al_2O_3$ | No Annealing | No Barrier |
| 20nm $SiO_2$ | 2nm $HfO_2$ | 750°C 2min | No Barrier |
| 20nm $SiO_2$ | 2nm $HfO_2$ | 750°C 2min | 2nm TiN |

failure can occur when applying a positive voltage to the TE. The TaN/Ta barrier is sufficient to prevent Cu from drifting through the Mo layer and into the dielectric; hence, metal drift-induced failure can be caused by $Mo^{+2}$ ions only [12]. A 20nm-thick PE-ALD $SiO_2$ film mimicked the oxide layer between adjacent word lines while $Al_2O_3$ or $HfO_2$ were used as HK liner. For each $SiO_2$/HK combination, a split with and one without a 2nm-thick TiN barrier between the HK and the Mo TE was fabricated and characterized, in order to have a direct assessment of role played by the TiN barrier in preventing Mo drift [12]. In order to mimic the thermal budget seen by HK liners in 3-D NAND flows [5], high temperature anneals were performed after deposition of the HK liner. This can also isolate and shed light into the impact of such high thermal budget on the failure mechanism. A detailed list of the samples used in this study is provided in Table I.

### B. *Measurement Procedure*

First, J-V curves at 25°C were recorded on all wafers to extract positive ($+E_{BD}$) and negative ($-E_{BD}$) breakdown fields. Subsequently, Time-Dependent Dielectric Breakdown (TDDB) measurements were performed on the p-caps at 100°C and 200°C. Devices were stressed using both positive and negative constant stress voltages applied to the TE and the failure criterion was defined as an abrupt change in the leakage current. A wide range of stress fields and temperatures were needed to discriminate intrinsic dielectric breakdown from metal drift-induced failure using TDDB [12]. For each stress condition the Time-To-Failure ($TTF_{63.2\%}$) was extrapolated and then used to extract the field acceleration factors for positive ($m_{V+}$) and negative ($m_{V-}$) stress voltages using the power law model ($t_{63.2\%} \sim E^{-m}$) [13]. Dealing mostly with bi-layer dielectric systems, metal drift-induced failure cannot be simply assessed by comparing $m_{V+}$ and $m_{V-}$ [12]. Both extrinsic, i.e., Mo metal drift, and intrinsic factors, i.e., differences within the dielectric stack may result in substantially different positive and negative field acceleration factors. In fact, the BE/$SiO_2$ and the TE/HK interfaces will inevitably result in different injection currents; moreover, the $SiO_2$/HK interface is likely to affect the overall response of the dielectric stack [14].

## III. RESULTS

### A. *Leakage Current Measurements*

The positive and negative breakdown fields extracted from the I-V measurements at 25°C are plotted in Fig. 2a and Fig. 2b, respectively. As schematized in the band diagram in Fig. 2d, the positive leakage current (+J) and breakdown fields are expected to be the same for all samples, being mainly determined by the injection of electrons from the $SiO_2$/BE interface, particularly at high fields. On the contrary, the negative leakage current (–J) and breakdown fields should be sample-dependent being affected by both the TE/HK interface and by the HK thickness and dielectric constant. Although the

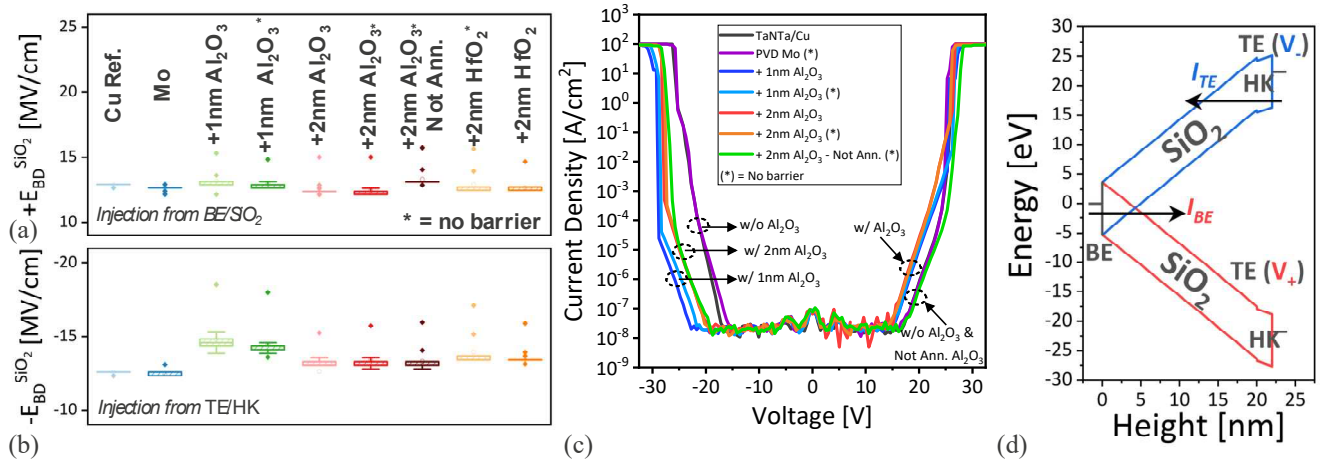


Figure 2. (a) Positive ($+E_{BD}$) and (b) negative ($-E_{BD}$) breakdown fields extracted at 25°C. (c) Experimental leakage current recorded at 25°C on single layer $SiO_2$ p-caps and bi-layer systems with $Al_2O_3$. (d) Band diagram schematic for the $SiO_2$/HK systems; for large positive applied voltages the leakage current is dominated by the electron injection at the $SiO_2$/BE interface.

experimental data plotted in Fig. 2c confirmed such expectations, we also observed a larger –J and lower $-E_{BD}$ for stacks with 1nm- than for stacks with 2nm-thick $Al_2O_3$ layer, regardless of the TiN presence and the annealing step. Nothing anomalous was observed for the samples with $HfO_2$ (I-V not shown). To better understand the unexpected result, the two dielectric systems were simulated in Ginestra™ [15], using 100nm x 100nm p-caps to reduce the computational demand. Three different scenarios were evaluated:

- #1 a higher defectivity in the $Al_2O_3$ than in the $SiO_2$ layer and uniformly distributed within the films;
- #2 a higher surface defectivity at the top $SiO_2$ layer, at the $SiO_2/Al_2O_3$ interface;
- #3 a combination of scenarios #1 and #2.

For each scenario, a Design of Experiment (DOE) was set up in Ginestra™ whose details are reported in Table II. Defect-free devices were also simulated and used as a reference in Fig. 3 in which only a selection of extreme cases is plotted. As expected, the extracted J-V curves for the defect-free devices show a higher $-E_{BD}$ and lower –J for the stack with 2nm- (blue circles) than for the one with 1nm-thick $Al_2O_3$ (red circles). However, as for the experimentally measured devices, once defects are introduced into the devices, the leakage current increases significantly only for the stack with 2nm-thick $Al_2O_3$ layers. Almost no variation is observed for devices with 1nm $Al_2O_3$ films for the three simulated scenarios. Although not shown in Fig. 3a, it is worth noting that for scenario #1 $-J_{2nm}$ was larger than $-J_{1nm}$ for all cases in which the $Al_2O_3$ had a higher defect density than the $SiO_2$ film. On the other hand, the higher defect density had no visible effect on the positive leakage current in scenarios #1 and #2 while we observed an impact on +J in scenario #3 that appears to better approximate the experimental data. Finally, it is worth mentioning that the post-deposition annealing of the $Al_2O_3$ films has no impact on –J while its impact is clear on the positive leakage current as visible in Fig. 2b. For the not-annealed stack, +J matches the response the $SiO_2$ films, suggesting that the high temperature annealing may have a larger impact on the interface defectivity rather than on the HK film. In conclusion, the anomalous response of the $SiO_2$-$Al_2O_3$ stacks is likely caused by a high defect concentration at the $SiO_2/Al_2O_3$ interface and by a higher defect density within the HK layer compared to the $SiO_2$. It is reasonable to assume that such a defect-rich interface is present also in the $SiO_2/HfO_2$ stacks, but its impact appears negligible, probably because of the much lower post-deposition annealing temperature (see Table I).

Table II. – Complete list of the volume ($cm^{-3}$) and surface ($cm^{-2}$) defect density used for the Ginestra™ simulations.

| | | Scenario #1 | Scenario #2 | Scenario #3 |
|---|---|---|---|---|
| $SiO_2$ | min | 1e17 $cm^{-3}$ | Defect free | 1e17 $cm^{-3}$ |
| | max | | | |
| $SiO_2/Al_2O_3$ interface | min | | 1e8 $cm^{-2}$ | 1e8 $cm^{-2}$ |
| | max | | 1e14 $cm^{-2}$ | 1e14 $cm^{-2}$ |
| $Al_2O_3$ | min | 1e17 $cm^{-3}$ | Defect free | 1e17 $cm^{-3}$ |
| | max | 1e19 $cm^{-3}$ | | 1e19 $cm^{-3}$ |

## B. *Time-Dependent Dielectric Breakdown Measurements*

The TDDB data obtained at 100°C and 200°C for all the samples are plotted in the top and bottom row of Fig. 4, respectively. Each subfigure shows data from a different dielectric stack, providing a direct comparison between the barrierless Mo splits and those with the 2nm TiN barrier/liner. The positive and negative field acceleration factors extracted using the power law model are shown in Fig. 5a and Fig. 5b, respectively. First of all, a good match was obtained for the $SiO_2$/Mo system both at 100°C and at 200°C, as for the Cu reference wafer, confirming that Mo does not drift into single-layer $SiO_2$ films. On the contrary, we observed a large difference between positive and negative TDDB for the $SiO_2$/HK stacks, particularly at 200°C. However, there is a good overlap between samples with and without the TiN, even at 200°C, suggesting the failure mechanism is the same for both splits. In fact, even if 2nm TiN were not sufficient to prevent Mo from drifting into the dielectric stacks, the TiN barrier should have had a sizeable effect on both $m_{V+}$ and

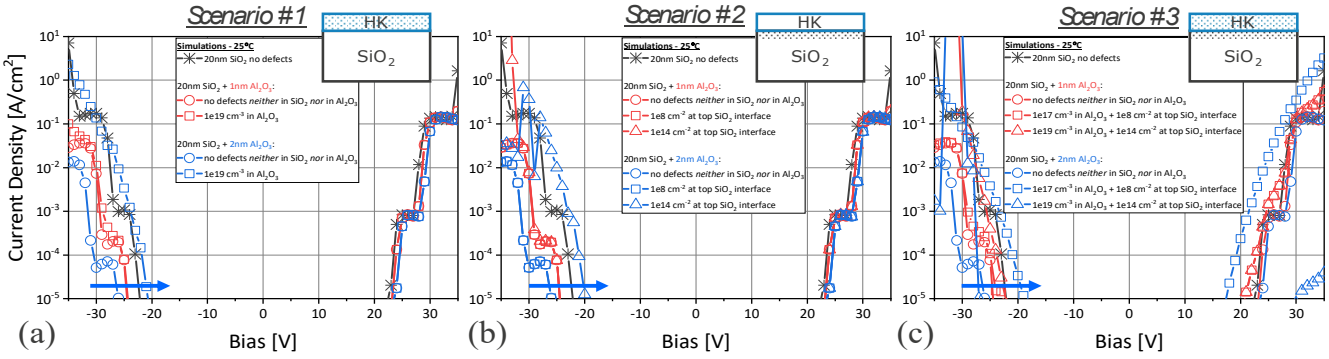


Figure 3. Current density extracted from Ginestra™ simulations for (a) scenario #1, (b) scenario #2 and (c) scenario #3. Details of the DOE are reported in Table II. In the schematics the dotted area represents the area with higher defectivity with respect the rest of the samples. The blue arrows highlight the visible shift in negative leakage induced by the increased defectivity of the stacks with 2nm $Al_2O_3$ films. Such a shift is not visible for the stacks with 1nm $Al_2O_3$ films (in red).

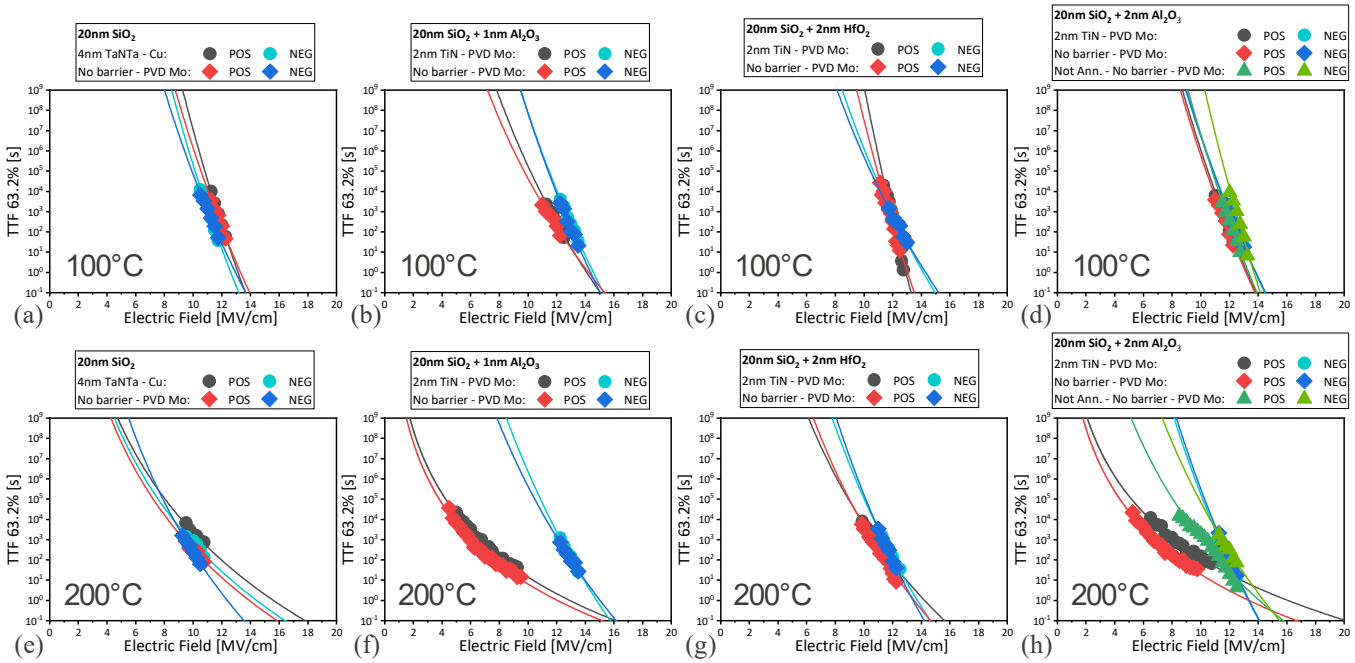


Figure 4. TDDB data obtained at (a) 100°C and (b) 200°C for a wide range of positive and negative stress voltages. TDDB data are grouped by the composition of the dielectric stack, in each subplot a direct comparison between the split with and without the barrier is provided.

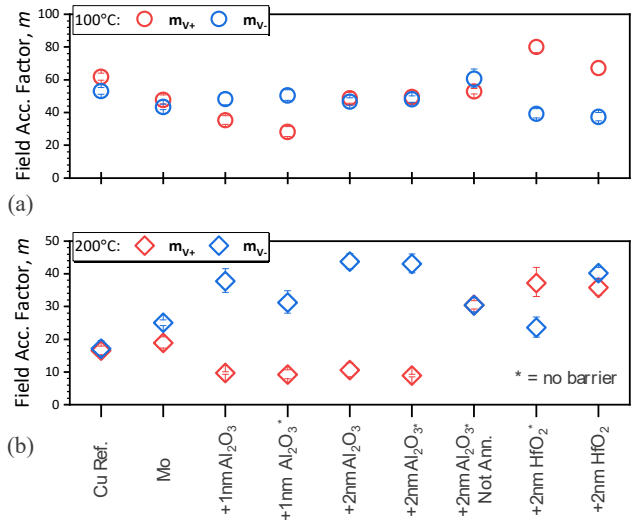


Figure 5. Field acceleration Factors extracted from positive ($m_{V+}$) and negative ($m_{V-}$) TDDB data at (a) 100°C and (b) 200°C. Only for single layer p-caps, a match between $m_{V+}$ and $m_{V-}$ indicates that Cu and Mo do not drift.

positive TDDB data [12]. Moreover, it is worth noticing how $m_{V+}$ at 200°C is the same for all the samples with the annealed $Al_2O_3$ samples, regardless of the thickness, while $m_{V-}$ changes from sample to sample depending on both the HK thickness and the TE/HK interface. Once again, the only visible exception is the not-annealed stack with $Al_2O_3$, that shows a higher resilience to positive stresses compared to the annealed ones, resulting in a better match between positive and negative TDDB data at both temperatures. The results are in agreement with both the experimental and simulated J-V curves discussed in the previous sub-section. All these observations suggest that all devices fail because of intrinsic dielectric degradation and not by metal drift-induced failure; a major role is likely played by the defects within the HK dielectrics and at the $SiO_2$/HK interface.

### C. *Triangular-Voltage-Sweep Measurements*

To better assess whether Mo drifts in the studied dielectrics or not, we performed Triangular Voltage Sweep (TVS) measurements at 200°C on all wafers, using both positive and negative stress currents. If $Mo^{+2}$ ions drift into the dielectric under a positive stress voltage, by using the TVS technique it is possible to study in a controlled way the formation and the dissolution of the metal filament, potentially restoring the device to its pristine status. TVS is a long-standing technique used to study mobile charges within semiconductor devices [16]. First, I-V are recorded on a fresh device; secondly, a constant stress current is applied to the device while recording the voltage [V(t)] across the capacitor; finally, a series of I-V measurements is performed on the stressed device until it breaks or it is restored to a pristine state, if metal drift occurred during the stress phase. As for TDDB measurements, negative TVS measurements were used to probe the intrinsic dielectric breakdown since no metal drift is induced. As visible in Fig. 6a-d and Fig. 7a-b, for all the stressed devices, regardless of the polarity of the stress current, either we observed hard breakdown for large stress currents or soft breakdown events for smaller stress currents, i.e. a drop in the voltage measured across the p-caps to approximately +10V and -10V, for positive and negative stress currents, respectively. The time frame within which the voltage drop occurs strongly depends on the magnitude of the stress current and on the dielectric stack composition, i.e. HK type and thickness.

Also, as visible in Fig. 6a (or Fig. 6c), for a given dielectric stack, there is no difference between the splits with and without the TiN barrier for positive stress currents that are capable of inducing metal drift. However, the most relevant outcome of the measurements is that all the post-stress I-V measurements (Fig. 6e-n and Fig. 7c-f) had the same characteristics, independently of the polarity of the stress current and of the HK characteristics: In none of the cases it was possible to restore the p-cap to its pristine state and a much higher leakage current was measured after the stress phase. We concluded that for none of the samples $Mo^{+2}$ ions drifted into the dielectrics; in reality, we observed a soft breakdown event at the $SiO_2$/HK interface that eventually leads to a breakdown of the HK. The chain of events is likely favored by the large defect concentrations discussed above. The two-step breakdown process is very similar to the one reported in [12]. The same occurs also for the $SiO_2$/$HfO_2$ stacks but the two-step breakdown process is easier to observe with $Al_2O_3$ due to its higher defectivity, lower permittivity value and higher annealing temperature. Such a hypothesis is validated by the outcome of the TVS measurements performed on the $SiO_2$ samples with TaNTa/Cu and shown in Fig. 7. Also, for this sample very similar soft breakdown events occur for both stress polarities and the post-stress I-V measurements have the same features of those shown in Fig. 6e-n. for bi-layer systems. In conclusion, the TVS measurements validated the hypothesis that intrinsic dielectric breakdown is the ultimate cause of failure for both polarities and hence Mo does not drift in the studied dielectrics. The large difference observed between positive and negative TDDB data is linked to the intrinsic differences between top and bottom interface. For negative stress voltages, because of the direct electron injection from the TE into the HK ($I_{TE} \neq I_{BE}$, Fig. 2d), only hard breakdown was observed; much lower stress fields would be required to observe soft breakdown events during TDDB measurements.

## IV. Conclusions

In this study we evaluated the reliability of Mo, a potential candidate to replace W as word line metal in 3-D NAND Flash memory devices. By combining TDDB and TVS measurements with simulations we concluded that Mo can be barrierless and it does not drift into the High-k/$SiO_2$ stacks that separate adjacent word lines. The extensive and diverse set of measurement techniques provided sufficient evidence that intrinsic dielectric breakdown is the sole cause of failure for all the characterized samples. In particular, the failure can be described as a two-step process, driven by the defectivity at

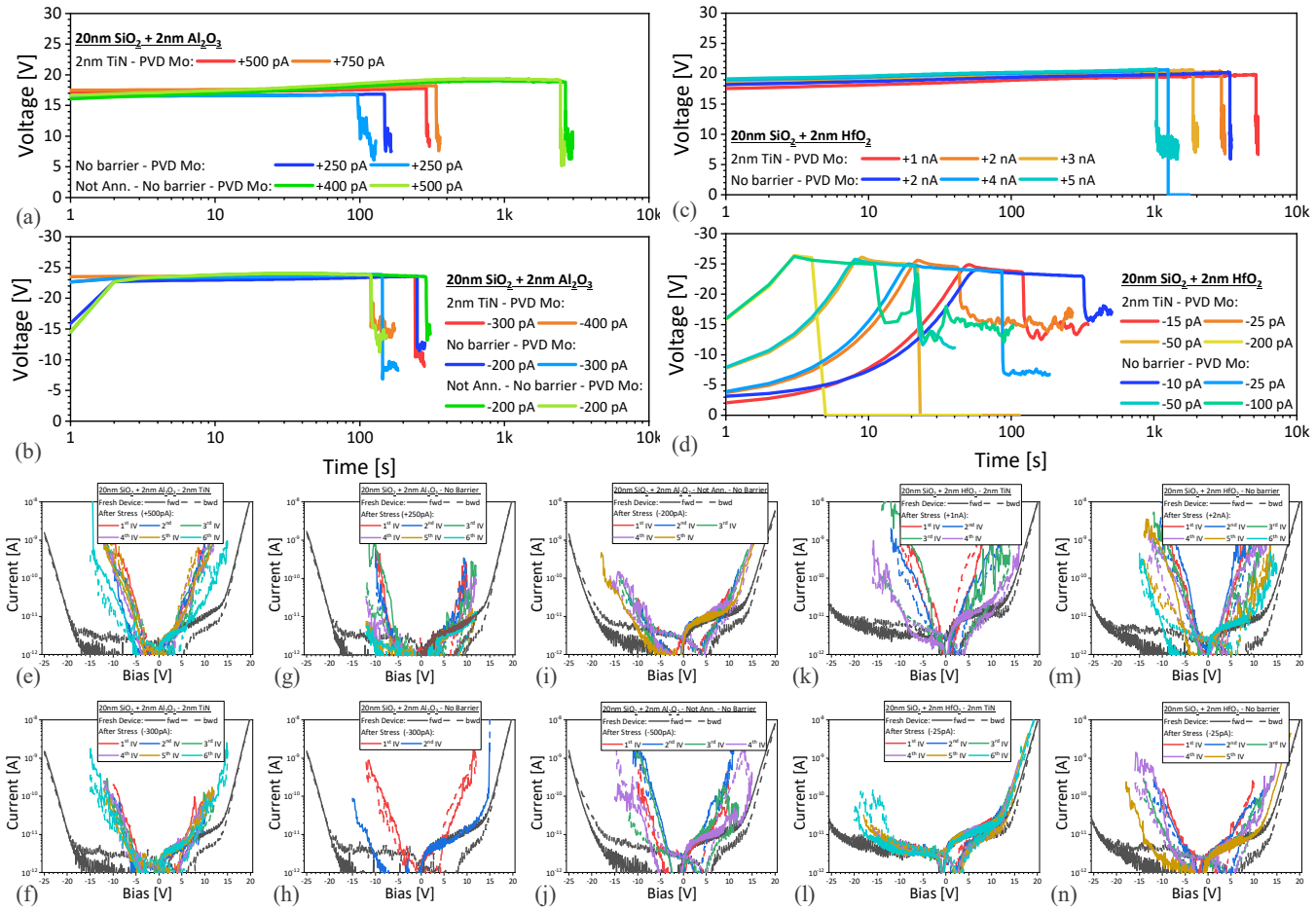


Figure 6. Triangular Voltage Sweep (TVS) measurements performed on $SiO_2$/(2nm)$Al_2O_3$ and $SiO_2$/(2nm)$HfO_2$ stacks, with and without the 2nm TiN barrier. While stressing the p-caps with constant (a) (c) positive and (b) (d) negative currents, the voltage across the capacitors was recorded until either a soft or hard breakdown event occurred. In (e) – (n) the I-V curves recorded on the devices before (in black) and after the stress phase are plotted.

the $SiO_2$/HK interface. Experimental data and simulations show a defect-rich top $SiO_2$ interface that has a detrimental impact on the performance of the dielectric stack, made even larger by the high temperature post-deposition annealing of the HK films. Although the dielectric stacks passed the 10-year lifetime test and were not affected by metal drift-induced failure, minimizing the defectivity at the $SiO_2$/HK interface is critical to ensure the correct functionality of the devices.

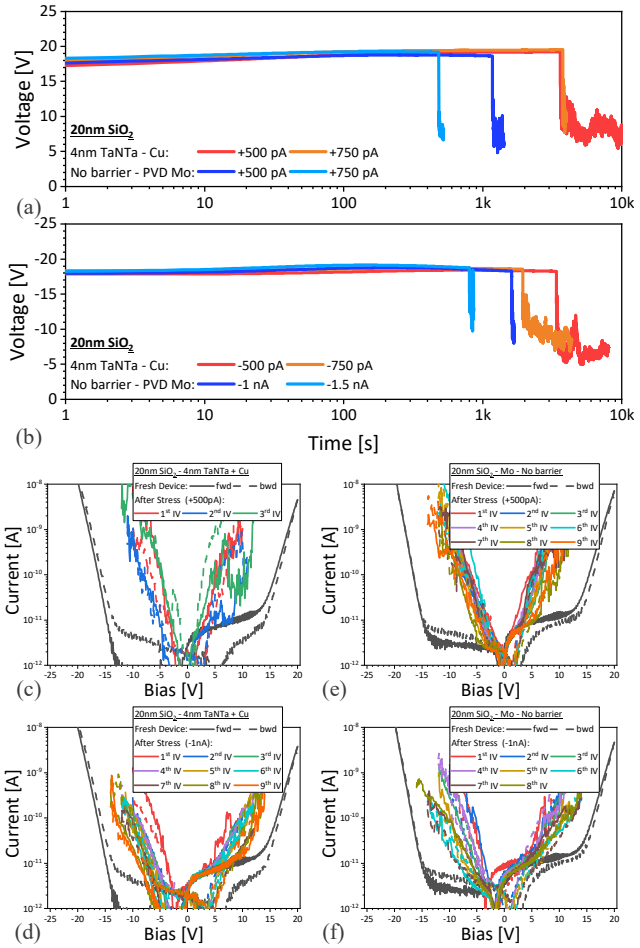


Figure 7. Triangular Voltage Sweep (TVS) measurements performed on $SiO_2$/TaNTa/Cu and $SiO_2$/Mo p-caps. While stressing the p-caps with constant (a) positive and (b) negative currents, the voltage across the capacitors was recorded until either a soft or hard breakdown event occurred. In (c) – (f) the I-V curves recorded on the devices before (in black) and after the stress phase are plotted.

## ACKNOWLEDGMENT

This work is supported by imec's Industrial Affiliation Program on Advanced Flash Memory devices. The authors are also thankful to Ivan Ciofi, Alicja Leśniewska and Olalla Varela Pedreira for their insightful comments and feedback.

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