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EUV Single Patterning Exploration for Pitch 28 nm

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ABSTRACT

EUV single patterning opportunity for pitch 28nm metal design is explored. Bright field mask combined with a negative tone develop process is used to improve pattern fidelity and overall process window. imec N3 (Foundry N2 equivalent) logic PNR (place and route) designs are used to deliver optimized pupil through source mask optimization and evaluate OPC technology. DFM (Design For Manufacturing) related topics such as dummy metal insertion and design CD retarget are addressed together with critical design rules (e.g. Tip-to-Tip), to provide balanced design and patterning performance. Relevant wafer data are shown as a proof of above optimization process.

Keywords: Design Rule, Design Retarget, EUV Lithography, NTD Process, EUV Single Patterning

1. INTRODUCTION

The International Technology Roadmap for Semiconductors (ITRS) shows that the pitch scaling is continuing and will push EUV Lithography (EUVL) to its limits. To further reduce the cost in manufacturing for advanced technology node, number of layers using EUVL patterning will be increase significantly.[1] Currently, single exposure (SE) EUV for metal layers has being developed and evaluated at imec to replace multiple patterning.[2,3] However, certain characteristics unique of EUV single patterning at tight pitch requires some changes in the way of process and design are optimized. In particular, the occurrence of stochastic printing failures has been recognized as a key element to consider when defining the minimum pitch and critical dimension (CD) of the design for EUVL patterning.[4–7] Furthermore, Mask three-Dimensional (M3D) effect has a significant impact on lithographic imaging at wafer level, which can introduce telecentricity error, best focus shift and through slit printability issues.[8–11] Therefore, to maintain logic technology scaling trend and lithographic performance, it is becoming vital to force combinations between the design and process, which is well known as Design Technology Co-Optimization (DTCO), several methodologies have been proposed.[12–14] In this paper, the concurrent design rule, optical proximity correction (OPC) and process optimization[15] is applied to explore the opportunity of pitch 28nm EUV single patterning.

Figure 1 shows the trade-off relationship among design rule, design retarget, OPC, resist and process, and source. To meet all the patterning requires (defect insensitivity, low dose patterning, and etc.) via balancing the trade-off relationship of these five parameters is difficult. In the paper, we are trying to optimize these five parameters concurrently to achieve our goals for pitch 28nm EUV single patterning:

1. EUV Litho-friendly Design;
2. Defect in-sensitive design / OPC;
3. Lower EUV patterning cost by increasing the throughput, thus using a lower exposure dose.

Since negative tone development (NTD) process can obtain superior imaging quality and overall large process window,[16,17] metal-oxide (MOx) resist combined with bright field mask are used during our two iterations of patterning optimization for pitch 28nm.

The paper is organized as follows. Section 2 introduces the first iteration and patterning performance of pitch 28nm EUV single patterning at imec, a simple dipole source and relaxed design rule are used. Section 3 introduces the second iteration of pitch 28nm EUV single patterning with the optimized source (SMO (Source Mask Optimization) source). Various types of design retarget and OPC techniques are optimized together with a tighter design rule. The last section will provide the summary.

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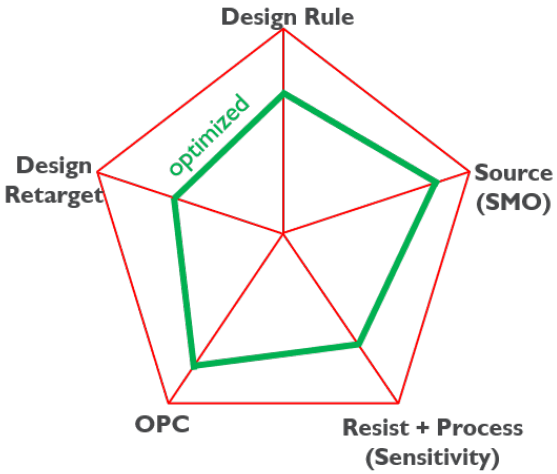

Figure 1: Trade-off relationship among design rule, design retarget, OPC, resist and process, and source

2. ITERATION I: SIMPLE DIPOLE WITH NTD PROCESS

To demonstrate the ability of extending EUV single patterning on imec N3 technique node (foundry N2 equivalent) at pitch 28nm, one of the most critical metal layers M1 is considered in our study. The M1 layer contains mainly vertical metal trenches, the minimum pitch and CD are 28nm and 14nm, respectively. In our first iteration, the design rule only allows to draw relaxed Tip-to-Tips (T2Ts).

2.1 Process Anchor and Limitation

Figure 2 shows the optimized simple aggressive dipole source, to improve the pattern fidelity and process window at denser pitch. The process anchor is targeting at minimum pitch 28nm with minimum CD 14nm according to the design rule. Fig. 3 shows the linearity of wafer CD with respect to the exposure dose for different mask CDs

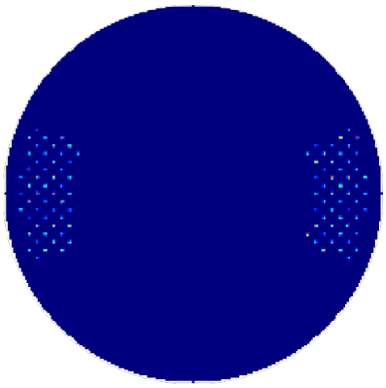

Figure 2: Aggressive simple dipole source optimized for Line/Space

at pitch 28nm. The result shows that, there are two options for targeting wafer CD 14nm: either using mask CD 13nm with a lower dose or using mask CD 14nm with a higher dose. The SEM image in the plot shows that both options can give us good pattern fidelity. However, since this is our first iteration and considering the manufacturability issues (low Line Edge Roughness (LER), stochastic failures free), pitch 28nm with mask CD 14nm is chosen as our process dose anchor feature to target wafer CD 14nm, therefore, a higher dose is used in our first iteration.

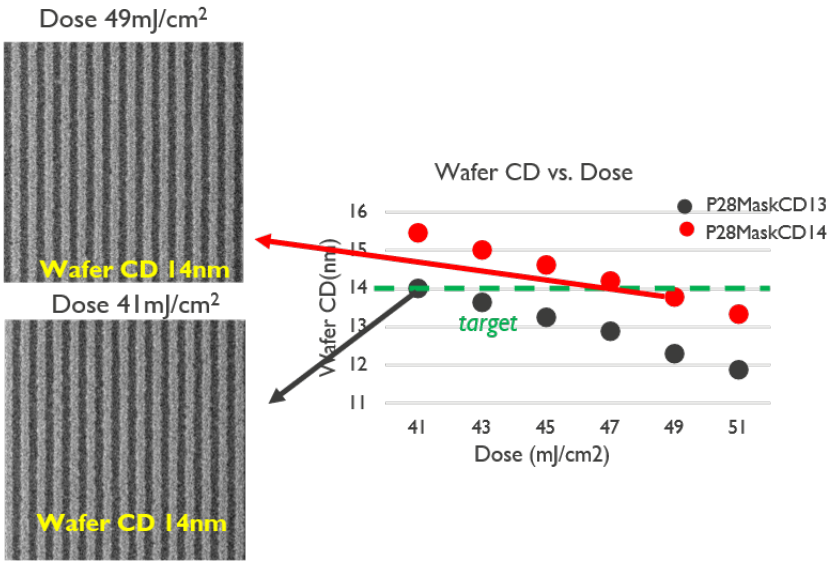

Figure 3: Wafer CD has a linear relationship with respect to the exposure dose

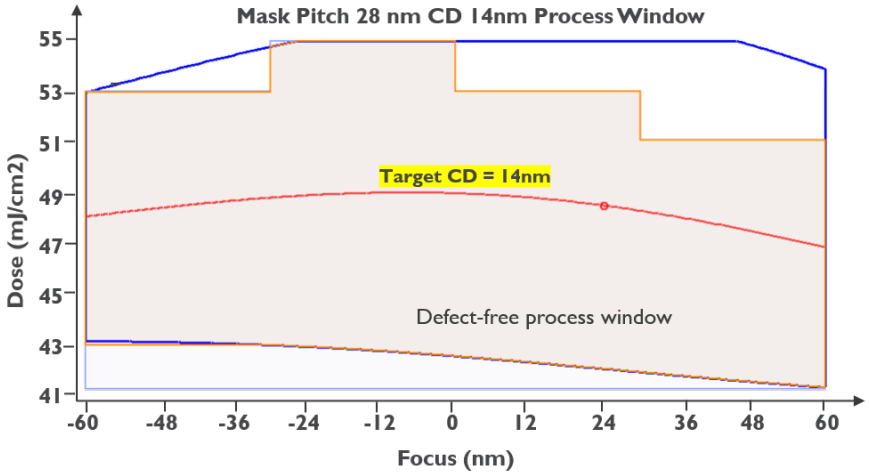

Figure 4: Overall process window of pitch 28nm with mask CD 14nm for target wafer CD 14nm (Red curve is the target CD; blue curve is the process window with +/-10% target CD variation, and the light orange region is the defect-free process window checked by per dose/focus condition)

Figure 4 shows the overall process window and defect-free process window of pitch 28nm. The defect-free process window is checked by per dose/focus condition. Compared to the overall process window, the defect-free process window is slightly smaller. Fig. 5 shows the process printability through pitch for targeting wafer CD 14nm. As shown in the figure, the stochastic effect becomes server as the pitch becomes larger, the microbriges appear for semi-isolated features. When the feature becomes more isolated, the 14nm trench CD is not printable. The problem must be solved during the OPC to guarantee the quality of the tapeout.

2.2 Design Retarget and OPC Optimization

EUV OPC needs to consider and balance several physical phenomena that are unique to EUV lithography. The OPC model must understand and compensate for the EUV related phenomena.[18] The main issue needs to be solved here is the process printability limitation through pitch, and maintaining a reasonable overall process

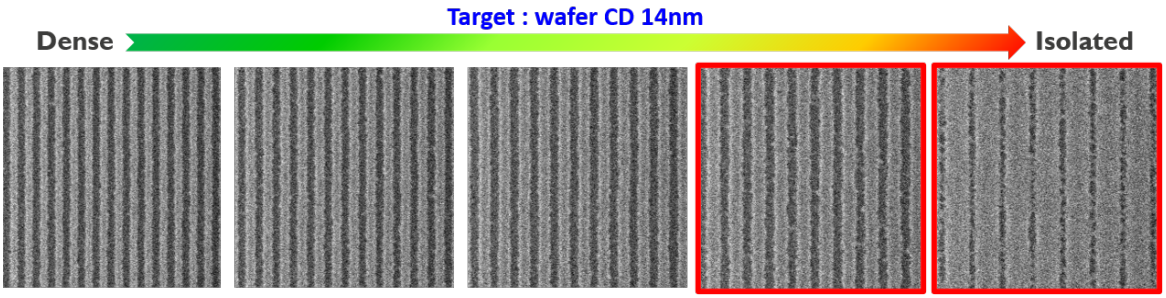

Figure 5: Process printability through pitch for targeting CD 14nm on the wafer

window such as Depth of Focus (DoF) and Exposure Latitude (EL). To successfully deploy a solution, CD retarget and dummy metal insertion are considered.

A) CD Retarget

Figure 6 demonstrates an example of the benefit by applying CD retarget on the design. The process can not print wafer CD 16nm at pitch 42nm, the CD-SEM image in the Fig. 6 (a) has a high LER and some microbridges due to stochastic effect. The stochastic failure-free CD window (from Bisschop et al.[7]) indicates that microbridges occur when the small space between two resist lines becomes smaller, and such small space-CDs occur at thicker resist lines when the pitch increase. Therefore, to reduce the stochastic effect on the target, the trench CD can be slightly biased upward. As shown in Fig. 6 (b), instead of printing wafer CD 16nm, the wafer CD is retargeted to 19nm, the stochastic issues can be solved. However, the disadvantage is that CD retarget changes the metal line width on the wafer, and the enough space is needed for retargeting.

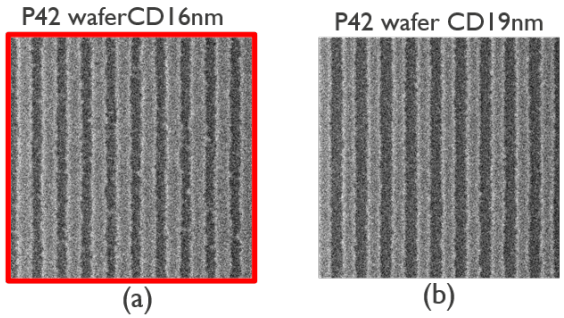

Figure 6: Example of CD retarget to reduce the stochastic effect (wafer CD increases from 16nm to 19nm)

B) Dummy Metal Insertion

As shown in Fig. 5, the process can not open the trench CD 14nm of semi-isolated and isolated features. SRAF insertion is a well known and well described method to improve the process window. Figure 7 shows an example of inserting SRAFs. However, imec assumes the minimum SRAF CD is 8nm. The image profile of the feature with SRAF CD equal to 8nm shows that the minimum intensity of inserted SRAF touches the OPC model threshold, which means SRAF with CD equal to 8nm will print on the wafer. Figure 7 demonstrates an example of SRAF printing. The risk of SRAF printing is that SRAF may merge to the main feature, and destroy the main design and functionality. Therefore, instead of inserting SRAF, dummy metal insertion is considered.

Dummy metal insertion is a strategy to achieve a highly uniform density of design layout,[19] to simplify the design and enhance the process window. In this paper, the methodology is adopted to pitch 28nm EUV single patterning. Figure 8 shows an example of dummy metal insertion on the semi-isolated feature at pitch 56nm. The dummy metal CD is the same as the main feature in the shown example, so the pitch 56nm design can be

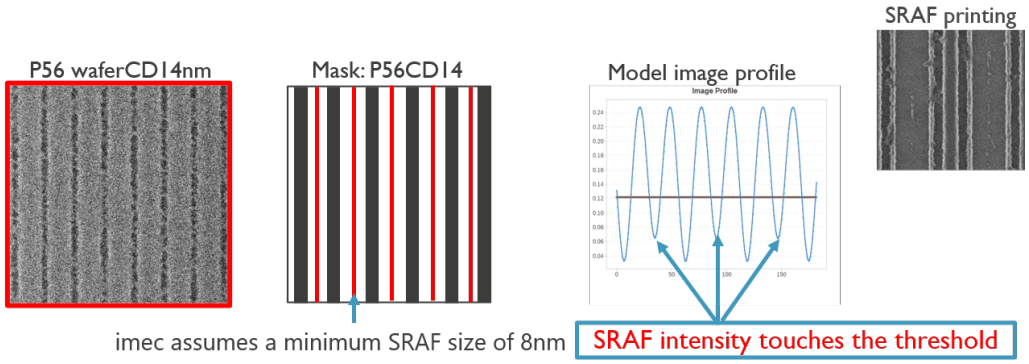

Figure 7: SRAF prints on the wafer

converted to pitch 28nm, where the process has good printability and large process window. During running OPC, the dummy metal size and position can be determined by the OPC software. However, stochastic effect should be aware during dummies insertion. And the impact of dummy metal on signal capacitance must be minimized.

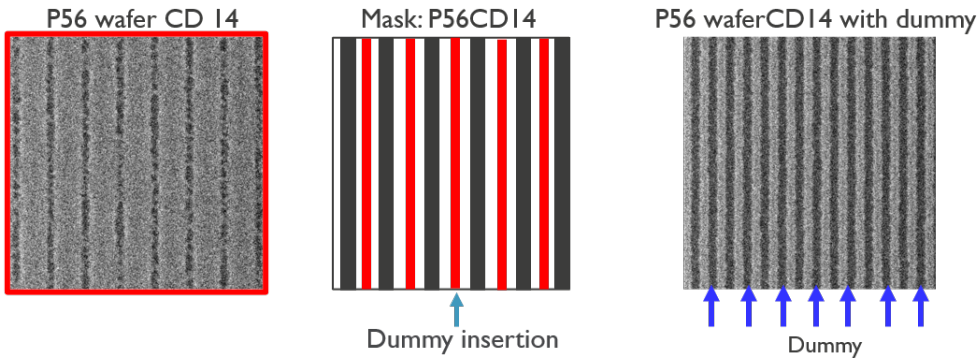

Figure 8: Example of dummy metal insertion

C) Post OPC Verification

The first pitch 28nm mask tapeout had been done at imec at the end of 2019. Post OPC and electrical test have been verified in 2020. Figure 9 shows the post OPC verification results at some of the interested positions on the design. The upwards row shows the designs and the downwards row shows the corresponding CD-SEM images. CD retarget is applied in the Fig 9 (b) and (c), to print isolated trench around 17nm instead of designed trench 14nm. The dummy metals are inserted in the Fig. 9 (a) and (d), the sizes and positions of dummies are determined by OPC software. A very good printability can be achieved with the design retarget and OPC solutions. The electrical test demonstrates that with dummy metals, the capacitance increase remains acceptable. The post OPC verification results show that using MOx EUV resist and bright field mask is a viable option for pitch 28nm EUV single patterning. Design CD retarget and dummy metal insertion provide a sufficient way to improve patterning fidelity and overall process window. D. Simone et al will show more details about the process verification, materialization and electrical test.[20]

3. ITERATION II: SMO SOURCE WITH NTD PROCESS

As introduced in the Section 3, to explore the opportunity of pitch 28nm EUV single patterning, the design rule only allows to draw relaxed T2Ts in our first patterning iteration,. A simple dipole source and a higher dose is

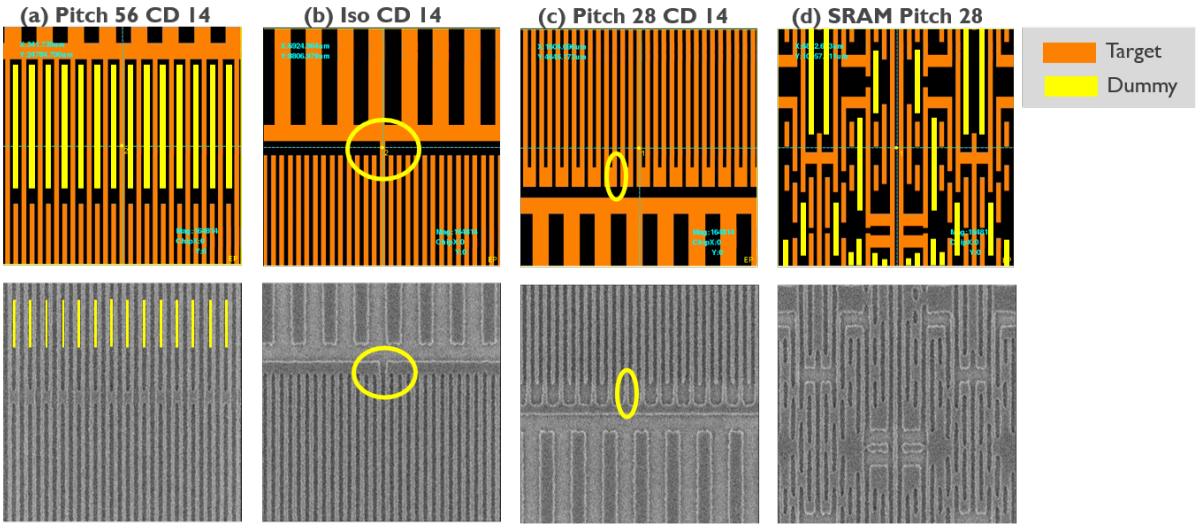

Figure 9: Post OPC verification at some interested positions

used to improve the pattern fidelity (reducing stochastic effort and improving LER) and overall process window. The post OPC results dedicates a good patterning performance of this process.

To continue our patterning study, the source, design rule and design retarget are optimized together in our second iteration. Figure 10 shows the design clip drawn based on the optimized design rule: minimum pitch and trench CD are 28nm and 14nm, respectively. The minimum T2T CD is down to 20nm. Figure 11 shows the

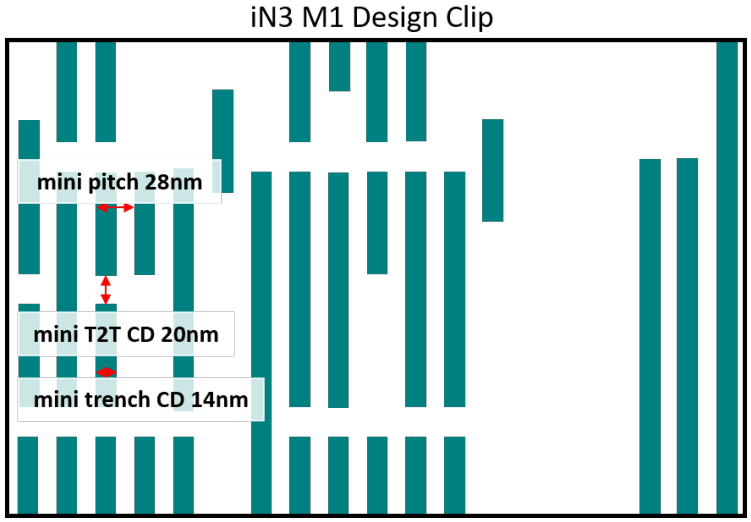

Figure 10: Design clip drawn based on the optimized design rule

optimized source and SMO overall process window based on this design clip. The new source together with NTD process can give us a large overall process window (DoF is around 44nm and EL is around 11%), higher T2T resolution and more room for T2T OPC.[21] As we known, enabling patterning using a lower exposure dose is a key to lower the EUV patterning cost by increasing the throughput. To lower the exposure dose, a slightly smaller mask CD (13.5nm, instead of 14nm) at pitch 28nm is used as the process anchor, to target wafer CD 14nm (Linearity of wafer CD with respect to the expose dose for different mask CDs is shown in Fig. 3). However,

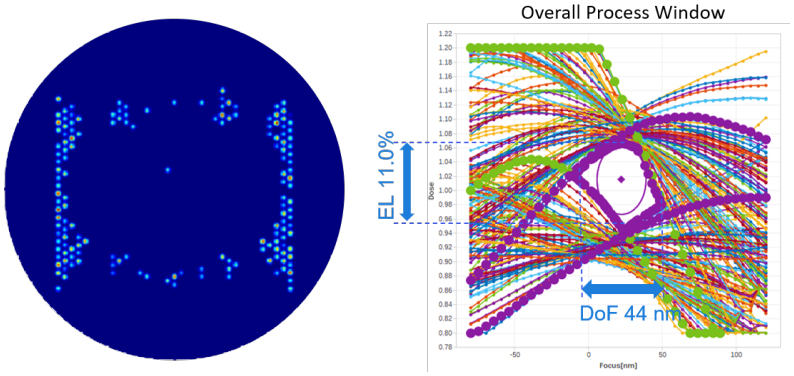

Figure 11: Source optimization for iN3 M1 design clip and SMO overall process window[21]

using smaller mask CD and lower dose to anchor the process, which will impact the overall process window, wafer defectivity, wafer CD Uniformity (CDU), as well as the Normalized Image Log-Slope (NILS) etc. All aspects have to be considered and compromised.

3.1 Process Limitation

A) Lithographic Process

Figure 12 shows the Line/Space NILS map with respect to the pattern printablity on the wafer through pitch and through CD. The red zone on the left side is the low NILS zone, corresponding to the features that are not printable on wafer or stochastic defects found in the SEM images. The green zone on the right side is the high NILS zone, where the features have good printablity. The yellow zone is the transition zone, the features are printing but with high LER. As shown in the figure, the high NILS zone is shifted as the pitch becomes larger, the current process can only print wafer CD 14nm at denser pitches. For larger pitches (semi-isolated and isolated features), design retarget is required to improve the pattern fidelity and overall process window.

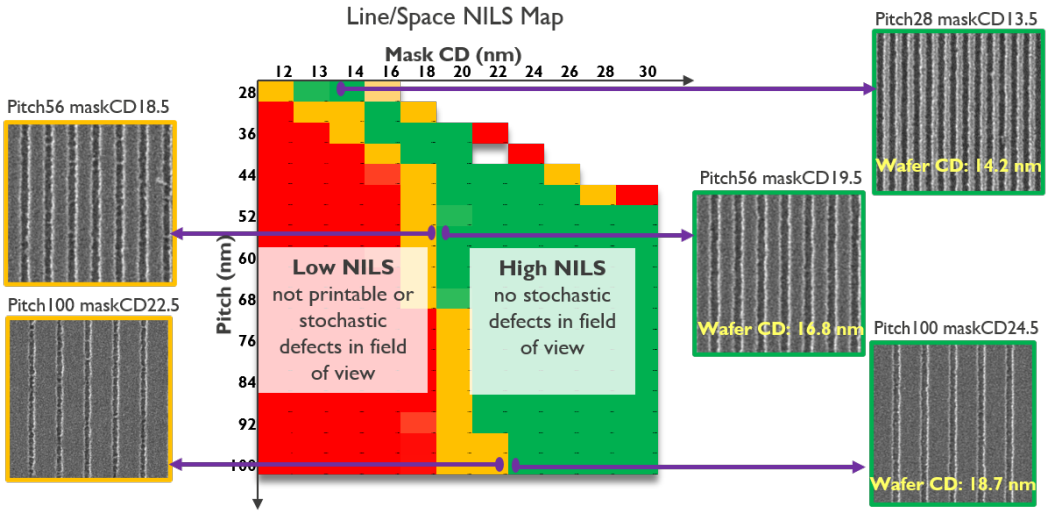

Figure 12: Line/Space normalized image log-slope (NILS) map with respect to the printablity on the wafer through pitch and through mask CD

Figure 13 shows the Two-Bar printability limitation of this process. For pitch 28nm design, 14nm wafer trench CD is not printable, microbridges found on the SEM image (as shown in Fig. 13), CD retarget is needed.

However, the resist line between the two trenches is very thin, applying CD retarget on both inner and outer edge of the trench might break the resist line (stochastic failure). Therefore, the CD retarget can only be applied to the outer edge of the trench. As shown in the Fig. 13, the pitch of the design will be slightly modified. For instance, applying 1nm bias on the outer edge of the two trenches at pitch 28nm, the design will be retargeted to pitch 30nm with the CD 15nm.

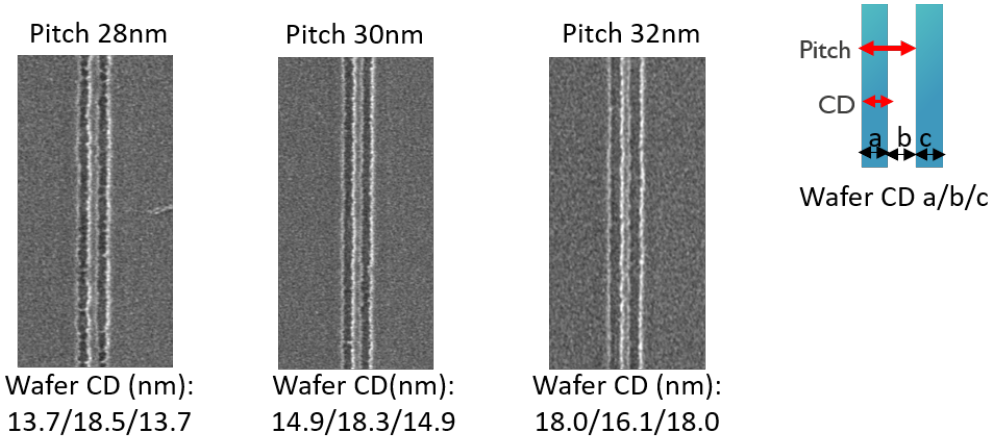

Figure 13: Two-Bar printability limitation of the process

B) Etch Process

Etch process is applied after lithography, to transfer the target from lithographic to etch. Figure 14 shows the comparison results for transferring the target from lithographic to etch. The line edge of etch taget is smoother than lithographic target, which means etch process can help to clean and reduce the pattern LER. For the target

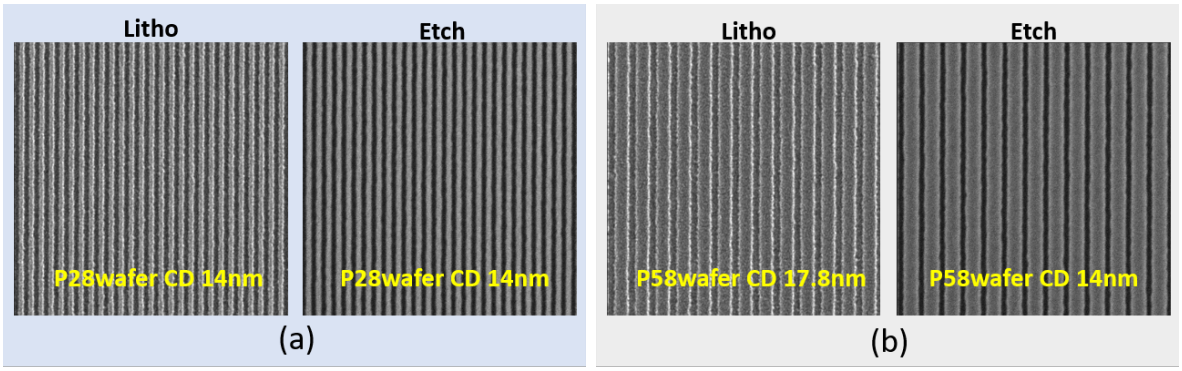

Figure 14: Transferring the target from litho to etch ((a) pitch 28nm: lith-etch bias is 0nm; (b) pitch 58nm: lith-etch bias is 3.8nm.

CD at pitch 28nm (as shown in shown in Fig. 14 (a)), the bias of transferring target from lithographic to etch is 0nm. However, as the pitch becomes larger, a larger lithographic target CD is needed to target the etch CD 14nm (as shown in shown in Fig. 14 (b), there is 3.8nm (1.9nm per edge) litho-etch bias at pitch 58nm). Lithographic target CD of semi-isolated and isolated features must be bias upwards.

To fully understand the etch process impact, the litho-etch bias is measured through pitch and through CD. Figure 15 (a) shows litho-etch bias per dege for target CD 14nm. As shown in the figure, litho-etch bias is 0nm at pitch 28nm, and the bias is become larger to 3nm per edge as the pitch becomes larger. Before running OPC,

the lithographic target has to be defined firstly. Figure 15 (b) shows an example for applying litho-etch bias on the design, after applying litho-etch bias on the design (etch target), the lithographic target CDs of semi-isolated and isolated features become larger. Etch process has the ability to enhance the process window.

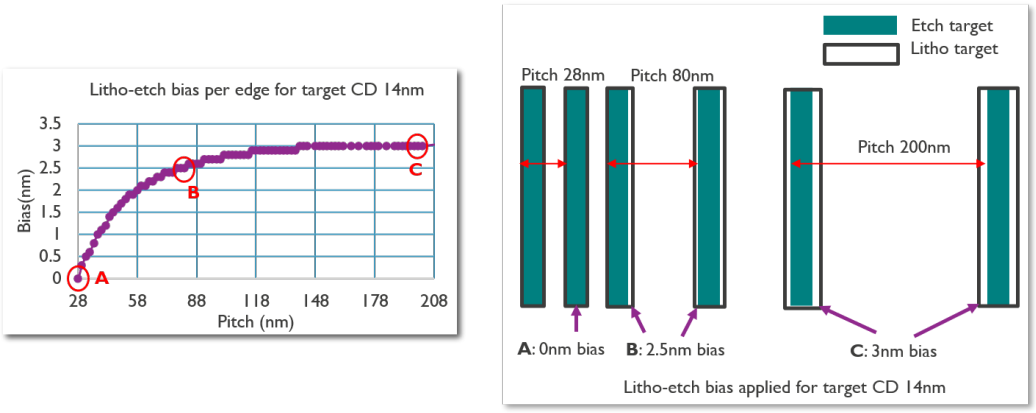

Figure 15: Litho-etch bias per dege for target CD 14nm and the example for applying litho-etch bias to the design

3.2 Various Types of Design Retarget and OPCs

To challenge the process limitation, iN3 M1 design contains Line/Space features from dense to isolated, Two-Bars, Three-Bars and short metals at the random patterns region. The minimum pitch and CD on the design are 28nm and 14nm, respectively. The random patterns contain 20nm T2T, short metal (14nm x 20nm) (as shown in Fig. 16). To enhance process window and improve the pattern fidelity, different types of design retarget are

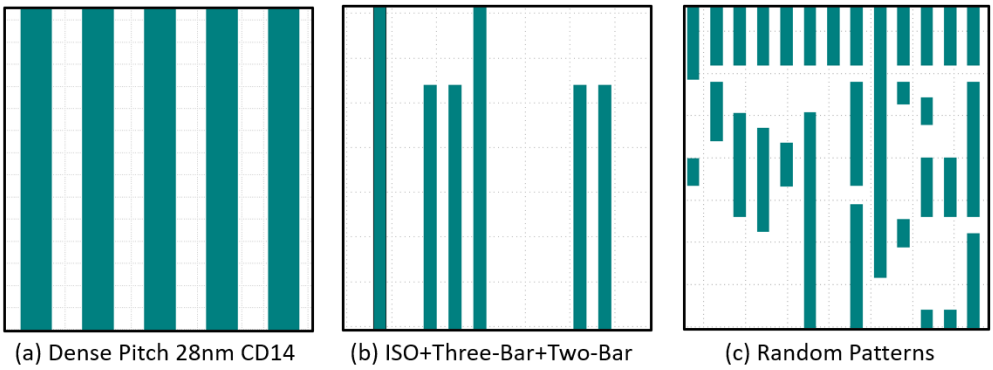

Figure 16: Details of iN3 M1 design clip

applied and tested on the new tapeout (as shown in Fig. 17):

1. Apply litho-etch bias firstly, then insert dummy metal;
2. Insert dummy metal directly;
3. Design CD retarget: semi-isolated feature CD 14nm is retargted to 17nm, isolated feature CD 14nm is retargeted to 20nm.

After applying design retargets, various types of OPC approaches are carried out to verify the abilities of enhancing process window:

1. Using extra CD retarget based on hotspots to the OPC solution;

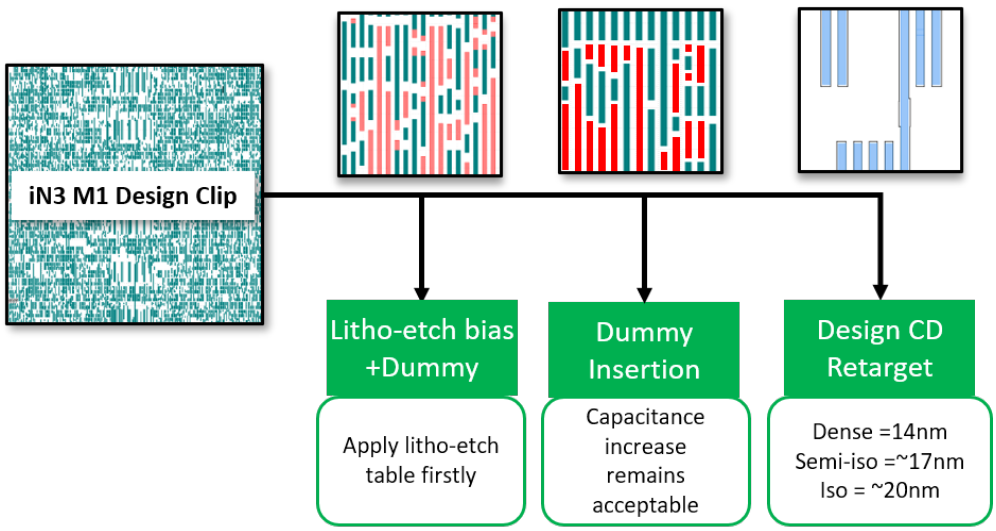

Figure 17: Three types of design retarget are applied and tested on the new tape out of pitch 28 EUV single patterning

2. Using process window aware OPC adds extra retarget to the OPC solution;
3. Using SRAFs: 6nm (aggressive assumption, imec typically assumes minimum SRAF size of 8nm) and 8nm SRAFs are inserted and evaluated. However, since the model shows that 8nm SRAFs are printable, the OPC solution will be verified with wafer data;
4. Using inverse lithography OPC to give the freedom of the OPC.

The different combinations of there four types of OPC solutions have been placed on the new tapeout, and all the solutions will be verified as soon as the mask arrived.

4. SUMMARY

EUV Single patterning ability for pitch 28nm metal design has been explored at imec. Metal-oxide (MOx) EUV resist and bright field mask is a viable option for patterning logic iN3 pitch 28nm technology node. In the paper, source, design rule, design retarget and OPC are optimized together to push the process limitation and enhance the process window. The post OPC verification shows good patterning performance by using CD retarget and dummy metal insertion. To lower the exposure dose and increase the throughput, a smaller mask CD at pitch 28nm has been used to anchor the process for the second iteration. To extend our study, different types of design retargets and OPCs splits have been placed on the new tapeout.

Further work will focus on different types of design retarget and OPC approaches verification, larger area defectivity, CDU, LER etc. The results will be presented.

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