Influence of Driver Integration on GaN Enhancement Mode Transistor Performance

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***Abstract*—GaN components are finding their way into power electronic applications as their increased switching speed allows for augmented switching frequencies, leading to higher power densities. However, raising the switching speed causes parasitic effects degrading part of the components superior performance. The main problem is the gate loop inductance which should be as small as possible. A low inductance can be achieved by integrating the driver and GaN component into the same IC. In this paper, a practical implementation of an enhancement mode GaN device with integrated driver IC and external driver is tested and comparisons between the performance of these devices in a boost converter will be reported. This allows to evaluate and compare efficiency and the influence of parasitic effects in the driver loop of a power converter.**

***Index Terms*—GaN HEMTs, integrated driver, half-bridge**

I. Introduction

GaN components are finding their way into power electronic applications. Their ability to operate at high switching frequency, due to the lower turn-on times causing only little switching losses, leads to higher power densities. Their specific on-resistance is lower in comparison to the classical *Silicon* (Si) components as well, leading to lower parasitics for the same power handling capabilities [1]. The principle of driving an *enhancement mode* (e-mode) GaN component is very comparable to driving a Si N-type MOSFET. However, the gate voltage margins and threshold voltage of e-mode GaN transistors are much smaller which makes the driver design challenging due to the use of higher switching speeds [2]. The parasitic components may be lower than their Si counterparts but the higher voltage and current slewrates makes these components more prominent. This causes damage and unwanted turn-on when the circuit is not designed properly, urging to use lower switching speeds, causing higher switching losses. This implies that a lot more care needs to be taken when designing the driver circuit. Also the *Printed Circuit Board* (PCB) design becomes a lot more important. The general objective is to limit parasitic effects by minimizing the size of loops in the gate drive and power stage [3].

A way to minimize the parasitics between drivers and transistors is to integrate all components into the same *Integrated Circuit* (IC). This way a lot of the PCB design challenges are moved towards the IC. The use of GaN-on-SOI (Silicon-On-Insulator) and trench etching was already proposed by X. Li et al. [4] to isolate two transistors from each other forming a half bridge. In [5] this was extended further by also including the drivers on engineered substrates of Qromis substrate technology. Here a low power 48V to 1V single stage buck converter using this technology was already successfully demonstrated. In this paper, the realized *GaN half-bridge with integrated driver* (GaNint) will be tested in a 25V to 50V single stage boost converter setup for powers up to 40W. In addition to that, this paper will not only evaluate the performance of GaNint but also benchmark it against available commercial external drivers. To enable this, a very similar GaN half-bridge IC with and without integrated driver is used (GaNint and GaNbridge).

The paper is organized as follows: First the parasitic problems that may occur in a synchronous boost converter circuit while using GaN components are briefly recapitulated in Section II. After that, the experimental setup and the most important component parameters are described in Section III. Then, in Section IV, the experimental results are discussed looking at the converter efficiency and switching speeds. At the end, Section V will conclude this paper.

II. Parasitic effects

As covered in Section I, GaN components were developed striving for lower losses in order to enable the use of higher switching frequencies thus allowing higher power densities. GaN components have lower losses because of higher switching speeds, lower gate charge and no reverse recovery.

Higher switching speeds means larger voltage and current slew-rates over and through the component, which introduce a series of problems. The parasitic elements of GaN components are smaller than their silicon counterparts but still remain present. The lower threshold voltage in the e-mode transistor combined with a very low voltage margin between recommended and maximum gate voltage makes gate driver and PCB design more challenging. This section is going to look deeper into the most important phenomena that occur.

A. Gate ringing

First the different elements that are present in the gate loop given in Fig. 1 are described. These are the gate capacitance C_G, the gate loop inductance L_G, the internal gate resistance

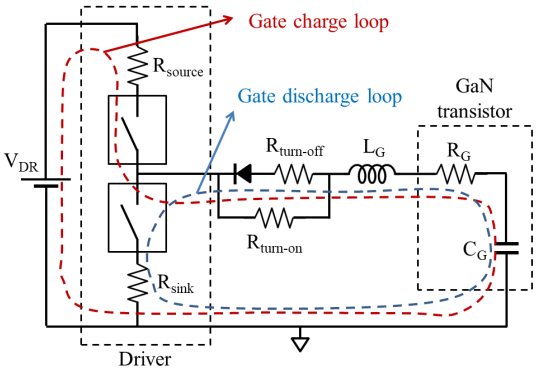


Fig. 1: Gate drive loop during turn-on and turn-off.

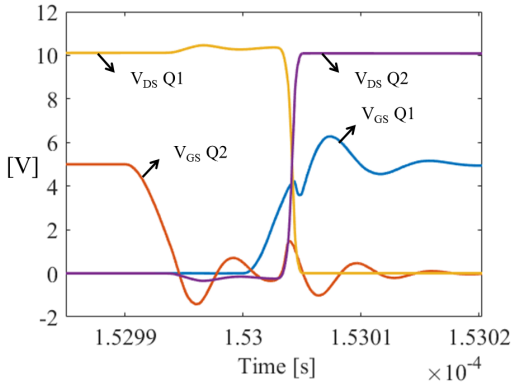


Fig. 2: Simulation of an EPC2023 GaN bridge in a boost converter setup with a parasitic inductances $L_G = 500\ pH$ in the gate loop. No external gate resistance is added. (Drain to source voltages scaled by a factor ten)

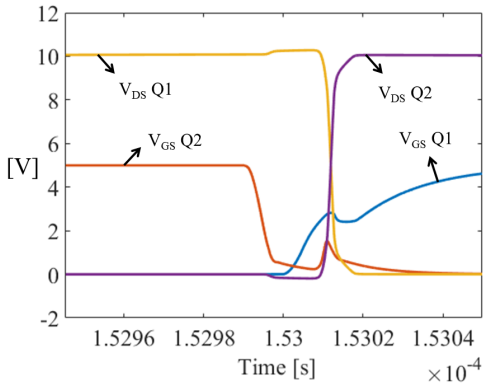


Fig. 3: Simulation of an EPC2023 GaN bridge in a boost converter setup with $R_{turn-on} = 10\ \Omega$ turn-on and $R_{turn-off} = 1\ \Omega$ turn-off external gate resistance and a parasitic inductance of $L_G = 500\ pH$ in the gate loop. (Drain to source voltages scaled by a factor ten)

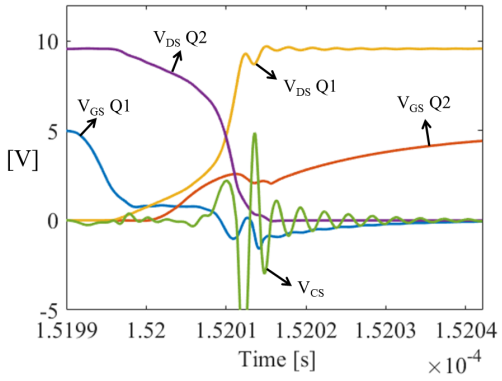


Fig. 4: Simulation of an EPC2023 GaN bridge in a boost converter setup with $R_{turn-on} = 10\ \Omega$ turn-on and $R_{turn-off} = 1\ \Omega$ turn-off external gate resistance and added common source inductance $L_{CS} = 50\ pH$. (Drain to source voltages scaled by a factor ten)

R_G and the pull-up resistance $R_{pull-up}$ during turn-on or the pull-down resistance $R_{pull-down}$ during turn-off. $R_{pull-up}$ is the sum of the internal driver resistance R_{source} and the externally added gate resistance $R_{turn-on}$, $R_{pull-down}$ is the sum of R_{Sink} and $R_{turn-off}$.

When charging the gate, resonance between C_G and L_G occurs. This so called 'ringing' gets damped by the resistance $R_G + R_{turn-on} + R_{source}$. For e-mode GaN transistors, the recommended gate voltage is around 5V while the maximum gate voltage is around 6V. The very small region in between both means that only very little overshoot is allowed. It is thus advisable to choose the gate resistance $R_{turn-on}$ such that the gate charge loop is critically damped [6].

When discharging the limit of -5V causes less problems, the resistance used for discharging $R_{turn-on}$ may thus be smaller and a little ringing can occur. Discharging thus can happen faster than charging. Care has to be taken to make sure the discharge ringing stays under the threshold voltage to prevent unwanted turn-on [7]. To make it possible to select different charge and discharge resistors, some manufactures provide a separate driver pin for charging and discharging. When this is not the case, a Schottky diode makes sure the off resistance is only used when discharging [8], [9].

Fig. 2 shows an example of unacceptable ringing that occurs in a synchronous boost converter when no gate resistance is added. It shows the forced commutation where the *control switch transistor* (Q1) is turning on and the *synchronous rectifier transistor* (Q2) is turning off. The reverse conduction through Q2 is visible as a negative voltage between the drain and source of Q2 [10]. Fig. 3 shows that the ringing can be suppressed by adding a 10 Ω turn-on and 1 Ω turn-off resistance to the gate circuit. Ringing is indeed avoided but the turn-on has become 25 ns slower. When choosing the resistance, a tradeoff has to be made between suppressing the ringing and high switching speed.

B. Cross talk or Miller turn-on

The gate resistance that is needed to limit ringing contributes to some other effects caused by the parasitic capacitances C_{DS}, C_{GD} and C_{GS}. In Fig. 5 a GaN transistor

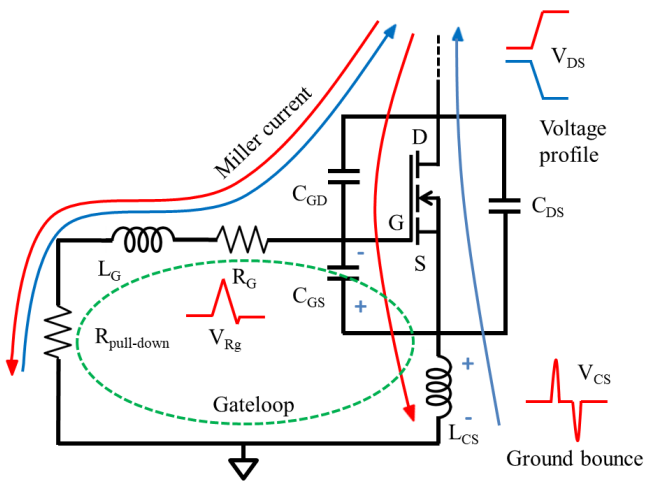


Fig. 5: Parasitic elements with indication of the mayor parasitic effects.

including these parasitics is shown together with the gate circuit when the transistor is turned off. D stands for Drain, S for Source and G for Gate, also the common source inductance L_{CS} is defined which will be of importance later on.

This subsection will briefly discuss cross talk or Miller turn-on. When a positive dv/dt over the transistor happens, C_{DS} charges. This causes C_{GD} and C_{GS} to charge as well. The voltage drop over the gate transistor due to this charging current causes the voltage at the gate to rise [11]. This phenomenon is depicted in red on Fig. 5. When the voltage becomes larger than the threshold voltage of the component, unwanted turn-on can occur. The most obvious cure is using a small resistor for turn-off $R_{turn-off}$ so a strong pull down is achieved. This however is limited by the internal gate resistance R_G and a too small off resistance may cause V_{GS} undershoot and ringing as shown in Subsection II-A. There are several additional methods to prevent this from happening but each of them have disadvantages such as increased cost, size and often also slower switching [7], [12].

C. Common source inductance

Some others problems are caused by the presence of the common-source inductance L_{CS}. This is the inductance that is common to both the gate loop and the power loop.

A first problem is current induced parasitic oscillations. A current though L_{CS} causes a voltage step at the source which induces an opposing voltage over C_{GS} as depicted in blue on Fig. 5. When the current is rising this causes a negative gate voltage. When the gate loop is under damped in the off state, this initial negative voltage can result in positive ringing causing unwanted turn-on [10]. Fig. 4 is a demonstration of this phenomena, the induced voltage over L_{CS} causes a distorted gate voltage profile.

A second problem is ground bounce which is a side effect of high dv/dt. These fast voltage transitions generate large current pulses due to the charging of parasitic capacitances [10]. Large currents induce a voltage over the L_{CS} causing a deviation between the transistor and driver ground reference as shown in red on Fig. 5.

D. Solution

All the problems described above are caused by the presence of inductance in the gate loop (L_G and L_{CS}). Several solutions exist to avoid problematic behavior of the component due to parasitic effects but these all degrade the performance resulting in slower switching thus leading to higher losses. The best solution is to eliminate the root cause of the problem as much as possible by minimizing the gate loop inductance. This can be done by integrating the driver into the GaN component IC because inductance resulting from the bond wires and PCB layout is avoided. Doing this makes the PCB design a lot less critical making the component more user friendly.

III. Experimental setup

This section will describe the experimental setup. The performance of an integrated GaN driver will be evaluated after which the performance of two commercially available external GaN drivers will be measured in the same circuit. This will give an idea of the performance range of available commercial drivers and allows to compare their performance with the integrated driver.

First the characteristics of the GaN bridge and drivers will be covered. Than the circuit parameters of the synchronous boost converter used in the PCB design are given.

A. Components

The circuits used in this section, are designed to facilitate the performance evaluation of the integrated driver and benchmark it against available commercial external drivers. In order to achieve a fair comparison, the same transistors should be used for all the conducted experiments. In general, this is difficult as the experimental chip with integrated driver is not using a commercial transistor but a custom GaN design. Comparison with industrial drivers is thus mostly not accurate because the transistor characteristics might differ significantly.

For the experiment in this paper, a transistor package with integrated driver and a similar (high side switch width $30\mu m$ and $50\mu m$ respectively) transistor without driver is available, allowing for a very accurate and fair comparison. The GaNint prototype is packaged as a bare die in a DIL18 package. This housing makes the device very sensitive and may not have very good cooling characteristics. Influence of the results due to the temperature dependent properties of GaN transistors may be expected. A picture of the die layout is given in Fig. 6.

The *GaN transistor half bridges without driver* (GaNbridge) are delivered in an UTAC package. This is a custom design, comparable to a 24L HSOP package. A thermal path is provided at the bottom of this package to help evacuate the heat trough the PCB. This feature is incorporated in the PCB design by the use of thermal vias leading to a copper plane that helps removing the heat. The most important parameters

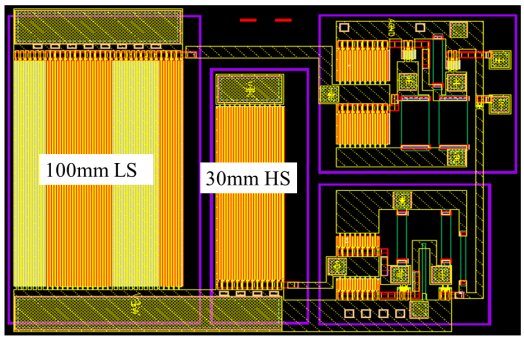


Fig. 6: Internal layout of the transistor with integrated driver.

Parameter	Value	Unit
$V_{DS\ max}$	200	V
$I_{d\ sat}$	8	A
$I_{d\ con}$	3-4	A
V_{GS}	5-6	V
$f_{s\ max}$	2	MHz
$R_{DS\ on}$ @25°C	7	Ω mm
$R_{DS\ on}$ @150°C	14	Ω mm

TABLE I: Parameters of the enhancement mode GaN transistor at 25°C.

of the half bridge are summarized in Table I, more details can be found in [5].

Because the GaNint has a bridge driver with two separate signal inputs, the same option will be chosen for the commercial drivers (not one *Pulse Width Modulation* (PWM) signal with resistor dead time selection). Some drivers are also suited to drive MOSFETs and IGBTs so it is important to select a driver with the correct *under voltage lockout* (UVLO) value. Finally *Si8273GB-IS1* (SiL) and *LMG1210RVRT* (TI) are selected as the appropriate drivers for the experiments. The most important characteristics of these drivers can be found in Table III.

B. Circuit parameters and PCBs

To test the performance, a synchronous boost converter circuit is used. Placing the components in this setup will allow to evaluate the behavior in a realistic situation. Table III lists the circuit parameters. $R_{turn-on}$ and $R_{turn-off}$ are only applicable to the external drivers.

Drivers	LMG1210 [13]	Si827x [14]
Manufacturer	TexasInstruments	Silicon Labs
Rated	200 V	650 V
T_{max}	150 °C	150 °C
f_{max}	50 MHz	Not given
Packaging	WQFN	SOIC-16 NB
$t_{rise\ max}$	5.6 ns	16 ns
$t_{fall\ max}$	3.3 ns	18 ns
R_{sink}	Not given	1.0 Ω
R_{source}	Not given	2.7 Ω
$C_{input-output}$	Not given	0.5 pF
max dv/dt	300 V/ns	400 V/ns

TABLE II: Parameters of different drivers according to the datasheet.

Parameter	Symbol	Value	Unit
Switching frequency	f_s	0.2	MHz
Dead time	t_{DT}	25	ns
Duty cycle	D	0.5	-
Input voltage	V_{in}	25	V
Output voltage	V_{out}	50	V
Power	P	5-50	W
Output capacitance	C	5.22	μF
Main inductance	L	100	μH
Turn-on gate resistance	$R_{turn-on}$	20	Ω
Turn-off gate resistance	$R_{turn-off}$	10	Ω

TABLE III: Parameters of the boost converter.

(a) Imec integrated driver (GaNint). (b) Texas Instruments LMG1210RVRT driver (GaNbridge and TI). (c) Silicon Labs Si827GB-IS1 driver (GaNbridge and SiL).

Fig. 7: Pictures of the three boards used in the experiments. All three boards are synchronous boost converters with the same components except for the driver.

In total, three PCBs are designed. The first PCB contains the GaNint, the second the GaNbridge with TI and the third the GaNbridge with SiL. A picture of the finished boards that were used in the experiments can be seen in Fig. 7.

IV. Experimental results

This section will look at the experimental results. The efficiency of the components is a very important, if not the most important criteria. First the converter efficiency of both the integrated and external drivers will be shown, allowing to compare their performance. After this, the drain to source switching waveforms will be shown as this allows to explain the seen differences. Then, some time will be spent looking at the switching speed. This is an important parameter that is influenced by the driver and determines for a large part the converter performance. At the end of this section some remarks will be made on the results seen in the previous parts.

A. Efficiencies of different drivers

Fig. 8 shows the converter efficiencies in function of the input power using the three different drivers. The input voltage of the boost converter was 25 V and the switching frequency was 200 kHz. The duty cycle is 0.5 lowered with the dead time of 25 ns which amounts to 1% of this duty cycle. The measurements were all taken in thermal equilibrium while

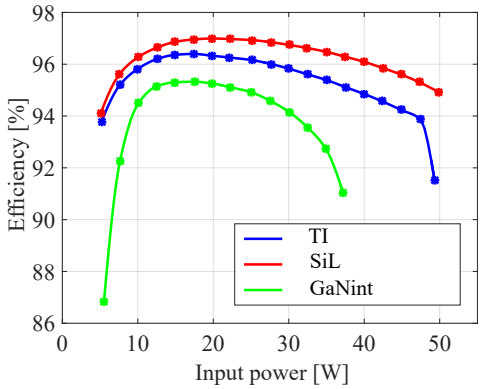


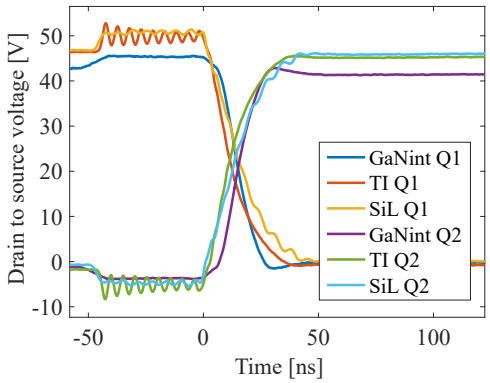
Fig. 8: Converter efficiency in function of the converter input power for different drivers. The test is done at an input voltage of 25 V, a switching frequency of 200 kHz, a dead time of 25 ns and a duty cycle of 0.5 (without a correction for the dead time).

the board was cooled using forced convection. Because the dissipation at each power level is different for each driver, the temperatures can be different for each driver in the same operation point.

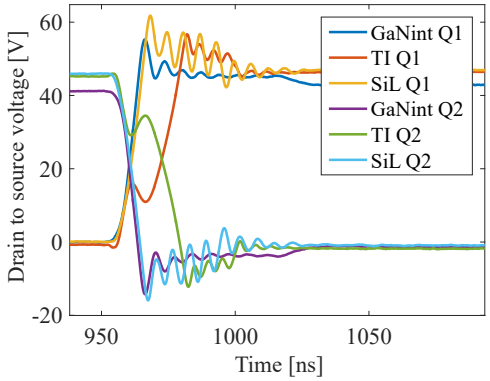
It can be seen that SiL has the best performance over the entire range of tested input powers peaking at 97.2%. The efficiency is lowest for small input powers because the fixed losses, like gate charge loss, are relatively more important. At higher powers, the conduction losses become most important, causing the curve to drop again towards the end. TI has the second best performance with a peak efficiency of 96.5%. GaNint is performing the least, peaking at 95.3%. In comparison with GaNbridge, which is equipped with a thermal pad, GaNint has a larger thermal resistance causing higher temperatures. The larger downward slope of the efficiency curve can be understood by taking the temperature dependence of the on-resistance of GaN into account.

B. Drain to source waveforms

The bad performance in terms of efficiency with GaNint is quite surprising. It has the least parasitic components and the gate resistance is also very low so a good performance is thus expected. To better understand the origin of the difference in efficiency between the drivers, Fig. 9 gives the drain to source waveforms at 25 W while the other input parameters are the same as during the efficiency measurement. During forced commutation, the transistor needs to switch the full voltage and current. This transition causes the largest stresses and generally creates the highest switching loss. It is useful to compare the times the transistors need to switch, for each driver installed. SiL took 40 ns, GaNint 30 ns and TI 37 ns. GaNint has the best and SiL the worst switching speed as was expected from looking at the datasheet. The same comparison can be made at self commutation where the voltage is naturally lowered by the reverse conduction through Q2 when Q1 turns off. SiL and GaNint show a switching time of 12 ns and 10 ns



(a) Forced commutation, Q1 turns on and Q2 turns off.



(b) Self commutation, Q1 turns off and Q2 turns on.

Fig. 9: Comparison of the drain to source waveforms of the different drivers. The measurements are done at a constant input voltage of 25 V and an input current of 1 A (25 W). The switching frequency is 500 kHz, the dead time is 50 ns and the duty cycle is 0.5 (without dead time).

respectively. The TI needs 26ns to complete this transition, deteriorating its global efficiency. The advantage of integration is directly visible in these waveforms. GaNint causes very little ringing compared to the other two drivers, while maintaining the fastest switching speed.

C. Switching speed as function of load current

The previous section already showed the switching speed achieved with the different drivers. This however, only gives the result at a particular power. To get a broader view on the behavior of the switching speed, in this section the input current is varied while the input voltage is kept constant. This is also how the efficiency curve in Fig. 8 was constructed.

The relation between switching speed and load current during self commutation should be linear as the load current discharges the output capacitance through reverse conduction. The forced commutation will slow down because the plateau voltage is dependent on the drain to source current but this dependence is less than linear. From these theoretical relations the resulting influence on the switching losses can be estimated as well. The switching loss during self commutation should

Driver	Current	0.5 A	0.7 A	1 A
Imec integrated (GaNint)	Self	16 ns	12 ns	10 ns
	Forced	18 ns	22 ns	30 ns
Texas Instruments (TI + GaNbridge)	Self	48 ns	35 ns	26 ns
	Forced	33 ns	35 ns	37 ns
Silicon Labs (SiL + GaNbridge)	Self	20 ns	16 ns	12 ns
	Forced	36 ns	38 ns	40 ns

TABLE IV: Switching speed for different converter input currents during self and forced commutation. The measurements are done at a constant input voltage of 25 V, the switching frequency is 500 kHz, the dead time is 50 ns and the duty cycle is 0.5 (without compensation for dead time).

remain unchanged as the influence of current and switching speed cancels each other. The switching loss during forced commutation rises in a more than linear fashion as the influence of the current is enforced by the slightly longer switching time. This behavior also explain, next to the temperature effects, why the efficiency curve drops for higher powers.

In Table IV the converter input voltage is fixed at 25 V while the input current is augmented from 0.5 A to 0.7 A and 1 A. It can be seen that the switching speed indeed decreases during self commutation and increases during forced commutation when the input current is raised. The three measurements points are to limited to see the real relations but the main purpose of this table is to give a good idea of the switching time magnitudes and the differences between the tested drivers. It can be seen that GaNint always has the best switching performance, preserving the earlier findings.

D. Remarks

GaNint, who clearly was the least efficient during the tests, seems to have the best switching characteristics, up to 16 ns faster than the external driver, which is very contradictory. The high temperature of the die, due to the packaging, may be a possible cause of its under-performance. Higher conduction losses may indeed lead to a large loss, certainly at higher powers where the measured difference is the most. The large discrepancy at low power is caused by the relatively high self consumption (100 mW against 50 mW) of the driver but this is negligible at higher powers. The authors expect that different packaging might lead to results that exceed the commercial driver performance. To confirm this theory, measurements of the package temperatures are necessary.

V. Conclusion

The theoretical discussion in Section II showed that the gate loop inductance is the driving force behind parasitic problems such as ringing and it should be minimized as fast switching is wanted. A possible way to do this, which also reduces the difficulties during PCB design, is to integrate the driver in the same package as the transistor. To verify this, an experiment was set up where an integrated driver is compared against two commercial external drivers. The unique approach in this experiment is that a similar custom GaN bridge was used, both for the integrated driver and the external drivers, allowing for a comparison that is as fair as possible. This makes it possible to evaluate the effects of integration and also see the performance spread present within the available commercial drivers.

The tests were performed using a synchronous boost converter. The use of a basic converter topology makes it easier to interpret the results. Silicon Labs and Texas Instruments drivers were selected for the tests with commercial external drivers. The setup with commercial devices reached efficiencies up to 97.2% and 96.5%, showing that there is a spread in commercial performance. The integrated driver reached 95.3% at its peak. With this result it seems like integration is not a solution to achieve better performance.

Closer investigation of the switching waveforms showed that the switching speed of the integrated driver is up to 16 ns faster than the commercial drivers. This confirms that the integration indeed leads to less parasitics, resulting in a better switching speed. The fact that this is not visible in the efficiency results, is believed to be caused by the integrated driver packaging, which has very bad thermal properties. Further measurement of temperature profiles is needed to quantify these findings.

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