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High-Speed Low-Power Rail-to-Rail Buffer using Dynamic-Current Feedback for OLED Source Driver Applications

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Abstract
In this work, we propose a rail-to-rail output buffer with low static-power and high speed for OLED display applications. To guarantee low static power consumption, low tail-current is designed in the buffer's first stage and the output stage is cut off in the static operation. To improve the transient response, dynamic-current-bias technique is used, and it also improves the system stability by pushing away the non-dominant pole. Meanwhile, we balance the large-signal slew-rate and system stability with dual-output buffer structure. Placing compensation resistor across the dual outputs creates zero for suitable phase margin, while the real output still behaves with low ON resistance and keeps high slew rate. The proposed design has been verified by a 0.18 μm 1.8 V/5 V CMOS process, which shows that the buffer only draws 2.8-μA static current. Under a 1-nF capacitance load and a 5-V power supply, the buffer achieves 1.18-μs settling time, which is only 41% of the single-output-stage structure with the same chip size (52 μm × 59 μm).

Keywords Low-power · High-speed · Rail-to-rail · Slew rate · Settling time · Current feedback · Compensation resistor · Stability · Output buffer · Source driver · OLED display

1 Introduction

In recent years, as OLED displays are moving toward high resolution, high refresh rate and low power consumption, implementation of high-speed low-power source drivers has become increasingly important. The output buffer amplifiers play a significant role in achieving these targets [1]. Hundreds or even thousands of output buffers are built in a display chip and each buffer amplifier has to be limited to a small area, so its static power consumption should be low [2, 3]. As OLED displays are widely employed in battery-powered systems, the power consumption of the buffers is more significant. Besides, settling time of the buffer should be as small as possible to meet the requirement by high-refresh-rate and high-resolution displays [4]. For a 2 K display, its horizontal scanning time is less than 4.069 μs with the refresh-rate of 120 Hz. The settling time has to be smaller than the horizontal scanning time. In addition, output buffer needs to offer an almost rail-to-rail voltage driving, which enables the OLED designs with higher grey levels [5]. The output buffer realized by operational amplifiers (op-amp) in unity-gain structure is used to drive capacitive column lines of the display panel. If the buffer can drive a wide range of load capacitance, it means that it can be used in large-/small-size displays and even AR/VR microdisplays. Moreover, op-amp with high open-loop gain is essential to obtain a low systematic offset voltage [6].

Researchers proposed output buffers with a floating current source structure, which are widely used in display drivers due to their low tail current and high stability [7–9]. However, the stability and slew rate constrain each other, and the high speed and low power cannot be achieved at the same time. Yu creatively proposed a current comparator structure, which shuts down the output stage to save power when the buffer is in static state [10]. Based on this idea, some papers further increased the buffer speed by

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increasing the slew rate [5, 11–16]. However, the tradeoff between static power consumption and settling time has not been settled yet.

The output buffer requires compensation for stability and the conventional compensation scheme uses a Miller capacitor, which occupies a large area. Furthermore, the output buffer with Miller capacitors usually need to set the output pole as the non-dominant pole [7, 11], which limits its application for large-size displays. Some buffers adopt the output terminal as the dominant pole to achieve enough phase margin without a Miller capacitor [13, 16–20]. But it is less flexible and not suitable for small size displays and AR/VR microdisplays. To solve this problem, some other buffers have been designed to achieve the phase compensation by adding a zero [21–23]. This is realized by a load capacitor and a compensation resistor connected between the output of the buffer and the load capacitor. But the large-signal slew-rate is limited by its compensation resistor.

To further solve the tradeoff between low static-power and fast transient-response, here we propose rail-to-rail output buffer with dual output stage and dynamic-current feedback. Firstly, we start with a dual-output-stage buffer and add the zero (compensation resistor) to improve the system stability. As the real ON resistance at output terminal is unchanged, fast slew-rate is guaranteed. Besides, low quiescent-power is achieved by low tail current in input-pair and prerequisite cut-off state in output stage. Its fast transient-response can be obtained with limited sacrifice of dynamic power. During the transient time, the request-current information is fed to input pair and results in larger dynamic tail-current. This speeds up first stage. It also pushes away the non-dominant pole and results in a more robust system. By this design, we solve the tradeoff between low quiescent-power and transient response. For detailed discussion, we present its fundamental building block in Section II. Its transistor-level circuit is given in Section III. In Section IV, we provide silicon data to prove our concept. Finally, we conclude our work in Section V.

2 Proposed low-power high-speed driving scheme

Figure 1 depicts the simplified block diagram of a class-B output buffer with current comparators. Two complementary boosting transistors, MOP and MON, are designed to be turned off in the static state. Because of the settings of Vos1 and Vos2, the current comparators C1 and C2 both output high voltage while the input voltage is stable. Consequently, transistors MOP and MON are both turned off, so no static power consumption is introduced by output stage. If Vin becomes higher, the output voltage of C1 will

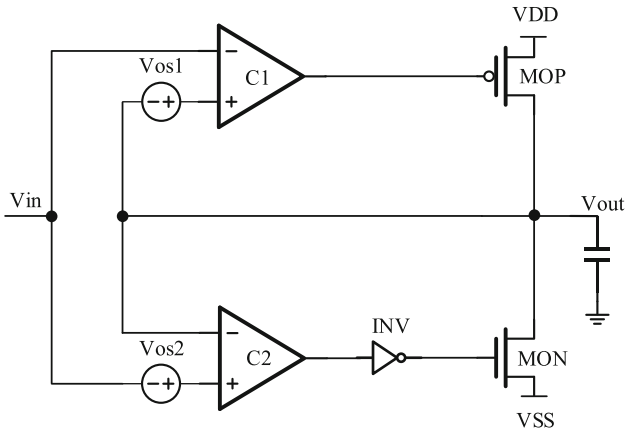


Fig. 1 Block diagram of a class-B output buffer with current comparators [10]

rapidly decrease to switch on MOP. As the voltage at MOP's gate can reach approximately VSS, a large output current is provided to charge the capacitance load.

Similarly, if Vin becomes lower, MON will be turned on to discharge the capacitance load quickly. Therefore, high-slew-rate driving capabilities can be easily achieved during the output buffer transient response. The proposed buffer amplifier exploits two current comparators, which are freely incorporated in a stacked mirror input differential stage to reduce power consumption and improve speed.

Figure 2 shows the traditional zero compensation scheme. It simply uses series-RC-chain at output terminal to obtain the zero shown in

$$Z_C = -\frac{1}{R_C C_L} \tag{1}$$

where C_L is the load capacitance and R_C is the compensation resistance. The non-dominant pole can be cancelled by the zero to enhance the op-amp stability. According to the analysis by Itakura [17], the damping factor ζ of the closed-loop second-order system is proportional to the value of $R_C\sqrt{C_L}$:

$$\zeta \propto R_C\sqrt{C_L} \tag{2}$$

The phase margin (PM) is more than 60 degrees for $\zeta \geq 0.6$ and the buffer amplifier is stable. The phase margin can be approximated as follows for $\zeta < 0.6$ [24]:

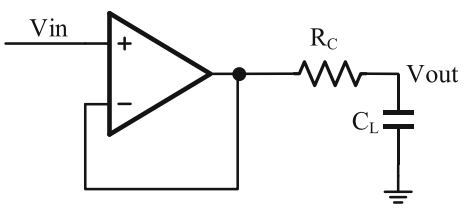


Fig. 2 Configuration of the traditional output buffer amplifier with the zero compensation [5, 22]

$$PM \approx 100 \times \zeta \tag{3}$$

It means the compensation resistor should be large enough to obtain an adequate value of phase margin. In addition, the larger the compensation resistor, the smaller the small-signal settling time [5]. However, increasing the value of the compensation resistor reduces the charge and discharge current and limits the large-signal slew rate.

The dual output stage is adopted in this proposed design. As shown in Fig. 3, the compensation resistor is connected between the output nodes of the two output stages, and the output node of A21 is fed to the negative input of the op-amp. The compensation resistor can be designed to be large enough to obtain sufficient phase margin and short small-signal settling time [5], while it does not affect the large-signal slew rate of A22. The transistor aspect ratio (W/L) of A21 can be designed to be smaller (with larger channel length) to achieve higher voltage gain and reduce offset voltage of the output buffer. The architecture of the proposed output buffer is shown in Fig. 4. The dual output stage is turned off by the current comparators C1 and C2 during the static state. With the advantages of low power, high speed and low offset, this buffer is suitable for high-resolution, high-refresh-rate OLED display applications.

3 Schematic of the proposed output buffer

Figure 5 depicts the circuit schematic of the proposed dual-output-stage dynamic-bias output buffer. Transistor MB1-MB3 consist a static bias network. In the application of display driver system, only two bias networks are placed on the left and right sides of source driver to provide bias voltage for static tail current transistors MB4 and MB5 of hundreds or even thousands of output buffers. We design the same transistor size for MB1, MB2 and MB4, and also for MB3 and MB5. This leads to the tail current of the input-pair equal to I_B. Transistors M1-M4 consist a rail-to-rail input differential pair. The diode-connected transistors M5, M7, M9, and M10 form symmetrical load to reduce mismatch. The output of the differential input-pair is

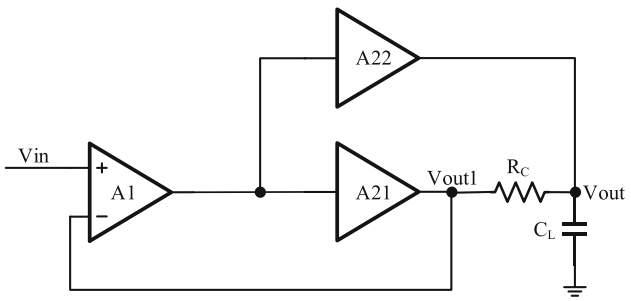


Fig. 3 Configuration of the proposed output buffer amplifier with the zero compensation [5]

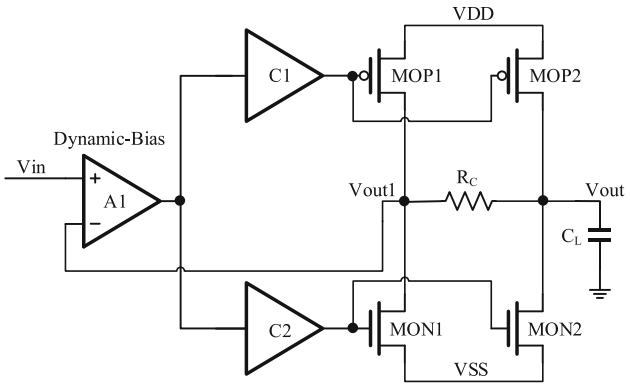


Fig. 4 Architecture of the proposed output buffer with dual output stage and dynamic-current feedback

mirrored by the current mirror to the comparator stages MC1-MC2 and MC3-MC4.

By designing a special aspect ratio, the current mirrored by M10 to MC2 is slightly larger than the current of M9 mirrored to MC1, and the current mirrored by M10 to MC4 is slightly less than the current of M9 mirrored to MC3. This can be obtained with the special design shown in

$$\frac{(W/L)_{MC2}-\Delta(W/L)}{(W/L)_{M10}} = \frac{(W/L)_{MC1}}{(W/L)_{M9}} \tag{4}$$

$$\frac{(W/L)_{MC4}}{(W/L)_{M10}} = \frac{(W/L)_{MC3}-\Delta(W/L)}{(W/L)_{M9}} \tag{5}$$

Taking the comparator composed of MC3 and MC4 as an example, as shown in Fig. 6(a). In static state, it is assumed that both MC3 and MC4 are in the saturation region. Since the current mirrored to MC4 is slightly smaller than the current mirrored to MC3, MC3 will leave the saturation region and enter the linear region. The drain voltages of MC3 and MC4 are pulled to high potential, and the output transistors MOP1 and MOP2 are turned off. Since MC3 is in the triode region, the source-to-drain voltage of MC3 can be approximately expressed as

$$V_{SDMC3} = \frac{\frac{(W/L)_{MC4}}{(W/L)_{M10}} I_{M10}}{\mu_p C_{OX}(W/L)_{MC3}(V_{SGMC3} - |V_{THp}|)} < |V_{THp}| \tag{6}$$

where

$$V_{SGMC3} = V_{SGM9} = \sqrt{\frac{I_{M9}}{0.5\mu_p C_{OX}(W/L)_{M9}}} + |V_{THp}| \tag{7}$$

Here μ_p is the hole mobility, C_{OX} is capacitance of gate oxide per unit area, and V_{THp} is the threshold voltage of the PMOS transistor. I_{Mi} (i = 9, 10) is the static current of the related transistors and it can be equal to either I_B (both buffer's input-pairs are turned on) or $0.5I_B$ (only one input-pair is turned on).

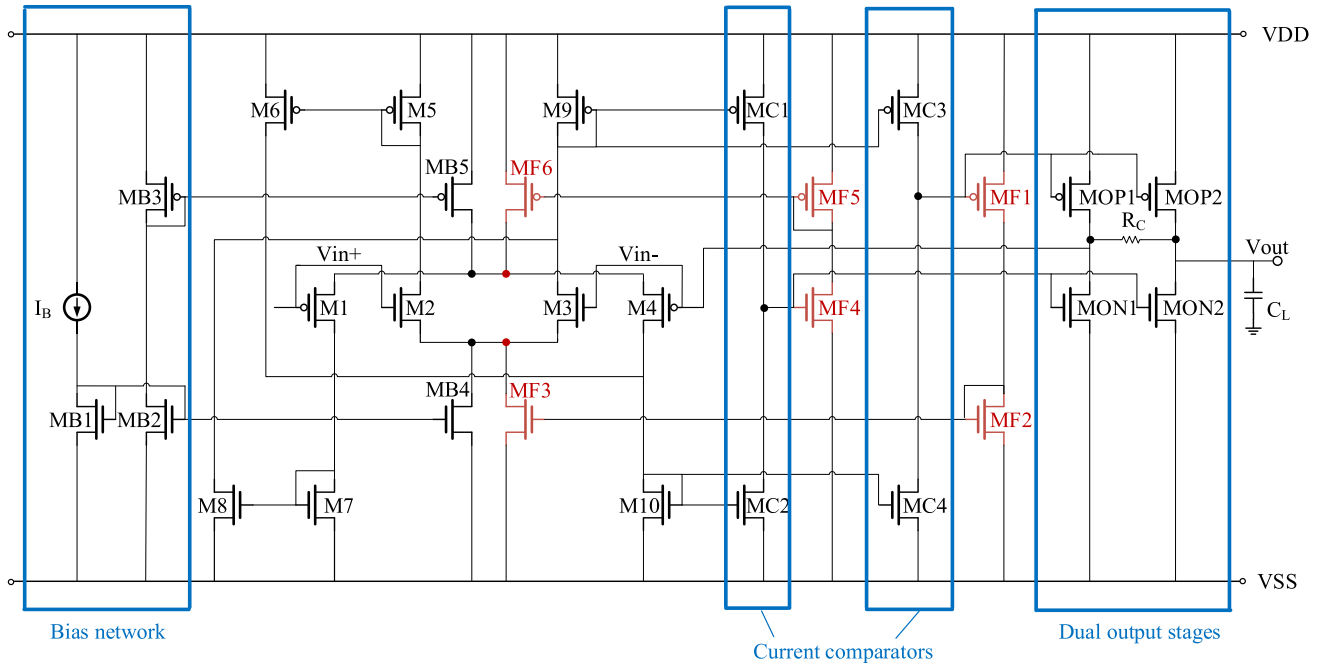


Fig. 5 Transistor-level of this proposed output buffer with dual output stage and dynamic-current feedback

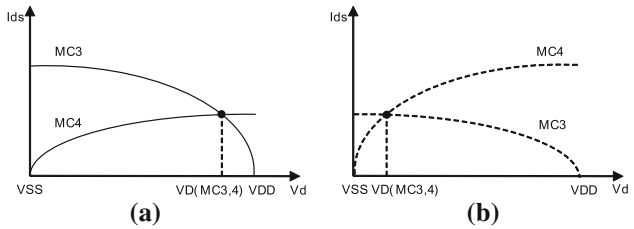


Fig. 6 The output characteristic curve of MC3 and MC4 during the **a** static state and **b** dynamic state

Similarly, the drain voltages of MC1 and MC2 are pulled down, and the output transistors MON1 and MON2 are turned off. The drain-to-source voltage of MC2 is given by

$$V_{DSMC2} = \frac{\frac{(W/L)_{MC1}}{(W/L)_{M9}} I_{M9}}{\mu_n C_{OX}(W/L)_{MC2}(V_{GSMC2} - V_{THn})} < V_{THn} \quad (8)$$

where

$$V_{GSMC2} = V_{GSM10} = \sqrt{\frac{I_{M10}}{0.5\mu_n C_{OX}(W/L)_{M10}}} + V_{THn} \quad (9)$$

Here μ_n is the electron mobility in the n channel, and V_{THn} is the threshold voltage of the NMOS transistor. Therefore, the output transistors consume no power during the static state. MF1-MF3 and MF4-MF6 (marked in red in Fig. 5) are dynamic biased structures. Taking MF1-MF3 as an example, since the gate of MF1 is connected to the gates of output transistors MOP1 and MOP2, MF1 is turned off in static state. Thus, the current positive feedback of MF1-MF3 is disconnected.

Given $g_{mIN} = g_{m1} + g_{m2}$ as the transconductance of op-amp's input-pair. When the input common mode voltage is.

close to VSS (VDD), g_{m2} (g_{m1}) is equal to 0. If the input-signal toggles, and the input-variation ΔV is sufficiently large to satisfy

$$\Delta V > \frac{I_B}{2} \frac{\Delta(W/L)}{g_{mIN}(W/L)_{MC3} - g_{m1}\Delta(W/L)}, \ \Delta V > 0 \quad (10)$$

or

$$-\Delta V > \frac{I_B}{2} \frac{\Delta(W/L)}{g_{mIN}(W/L)_{MC2} - g_{m2}\Delta(W/L)}, \ \Delta V < 0 \quad (11)$$

the output transistors will be turned on due the fact that I_{MC3} (I_{MC2}) is smaller than I_{MC4} (I_{MC1}) [22]. As shown in Fig. 6 (b), assuming that the input voltage increases, the drain-source current of M1 decreases, and the drain-source current of M10 increases, so the current mirrored to MC4 increases, and MC4 enters the linear region from the saturation region, while MC3 enters the saturation region from the linear region. The gate voltage of MF1 is pulled down, MF1 and the output transistors MOP1-MOP2 are turned on. Therefore, a feedback current is generated, which is added to the tail current source through the current mirror MF2-MF3, which greatly increases the bias current of the first stage. By dynamically increasing tail (bias) current, the slew-rate for buffer's input-stage is improved, while the actually required static tail-current can be quite low and the static power consumption is minimized.

3.1 A. Small-signal analysis

The small-signal equivalent circuits of the proposed output buffer is shown in Fig. 7, where g_{m1}, g_{m2}, g_{m31} *and* g_{m31} are the small-signal transconductances of the stacked-mirror differential amplifier stage, current comparators, and two output stages, respectively.

R_{o1}, R_{o2}, R_{o31}, R_{o32}, C_{o1}, C_{o2}, C_{o31}, C_{o32}, *and* V_1, V_2

are the equivalent output resistances, capacitances and voltages of the relevant amplifier stages, respectively.

The open-loop transfer function $A_{o1}(s)$ can be derived from Fig. 7. Assuming R_{o1}, R_{o2}, R_{o31}, $R_{o32} \gg R_C$ and C_{o1}, C_{o2}, C_{o31}, $C_{o32} \ll C_L$, it can be expressed by

$$A_{o1}(s) = \frac{V_{out1}(s)}{V_i(s)} \approx A_{dc} \frac{\left(1+\frac{s}{z_C}\right)}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)\left(1+\frac{s}{p_3}\right)} \tag{12}$$

where A_{dc}, p_1, p_2, p_3 *and* Z_C are given by

$$A_{dc} \approx g_{m1}R_{o1}g_{m2}R_{o2}(g_{m31}+g_{m32})(R_{o31}//R_{o32}) \tag{13}$$

$$p_1 \approx \frac{1}{(R_{o31}//R_{o32})C_L} \tag{14}$$

$$p_2 = \frac{1}{R_{o2}C_{o2}} \propto I_b \tag{15}$$

$$p_3 = \frac{1}{R_{o1}C_{o1}} = \frac{g_{mload}}{C_{o1}} = \frac{\sqrt{2\mu C_{OX}\left(\frac{W}{L}\right)_{M9,M10} I_b}}{C_{o1}} \tag{16}$$

$$z_C \approx \frac{g_{m31}+g_{m32}}{g_{m31}R_C C_L} \tag{17}$$

A_{dc} is the DC open-loop gain, while p_1, p_1, p_1 and z_C are the frequencies of the dominant pole, sub-dominant pole, third pole and left-half-plane zero contributed by the compensation resistor R_C. μ is the effective mobility for p-/n- type input-differential-pair. For analysis, the the bias current (including dynamic feedback) at the first stage is named as I_b. R_{o1} is equal to $1/g_{mload}$, while g_{m2} is approximately equal to g_{mload} in the proposed buffer. g_{mload} is the transconductance of the load current mirror transistors for the differential amplifier stage. The small-signal equivalent circuit contains three poles. However, the sub-dominant pole p_2 is cancelled by the left-half plane zero. The frequency of the zero is a function of R_C, C_L, g_{m31} and g_{m32}. The larger value of C_L increases the phase margin.

From Eqs. (15) and (16), it can be observed that larger tail current (dynamic-current-bias, no static-current penalty) at the first stage pushes the poles p_2 and p_3 to be higher to gain benefit of system stability. Meanwhile, to achieve lower system offset, we can design larger channel length for output stage to obtain a higher A_{dc}.

3.2 B. Large-signal analysis

If the input experiences a large signal, the output transistors and the current positive feedback will be turned on. The increased tail current in the first stage can be expressed by

$$I_{nf} = \frac{1}{2}\mu_p C_{OX}\left(\frac{W}{L}\right)_{MF1}(V_{DD}-|V_{THp}|)^2 \tag{18}$$

$$I_{pf} = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_{MF4}(V_{DD}-V_{THn})^2 \tag{19}$$

Figure 8(a and b) depict the large-signal equivalent circuits of the output stages for the rising and falling edges. The output step responses for rising and falling edges of the input waveform can be expressed as

$$V_{LH}(t) = V_L + (V_H - V_L) \times \left[1-\exp\left(-\frac{t/C_L}{(R_{MOP1}+//R_{MOP2})}\right)\right] \tag{20}$$

$$V_{HL}(t) = V_L - (V_L - V_H) \times \left[\exp\left(\frac{t/C_L}{(R_{MON1}+R_C)//R_{MON2}}\right)\right] \tag{21}$$

where V_L and V_H are respectively the initial low value and the final high value of the output voltage, while R_{MOPi} and R_{MONi} (i = 1, 2) are the ON resistances of the related transistors.

The settling time depends on the small-signal amplifier performance and the slew-rate time period. If the proposed buffer is required to drive the large-size OLED display panel, the settling time is dominated and restricted by slew rate, so the slew rate is very important, which can be expressed by

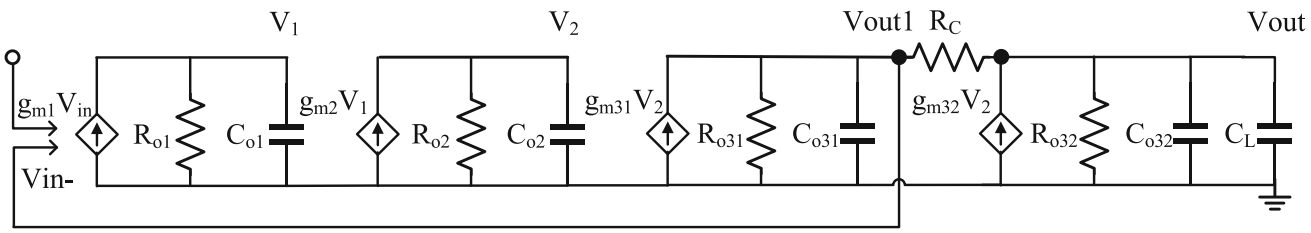


Fig. 7 Small-signal equivalent circuit of the proposed output buffer

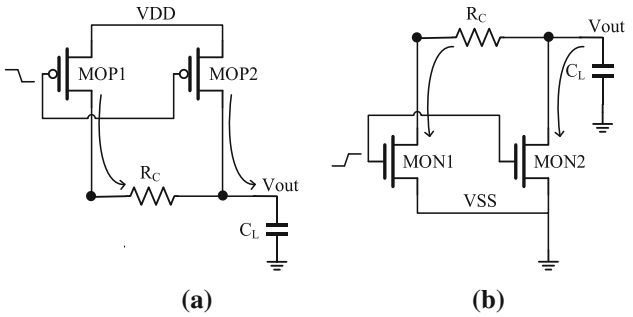


Fig. 8 Large-signal equivalent circuits of the output at **a** the rising and **b** the falling edges

$$SR^{+} = abs\left(\frac{dV_{LH}(t)}{dt}|_{t=0}\right) = \frac{(V_H - V_L)/C_L}{(R_{MOP1} + R_C)//R_{MOP2}} \tag{22}$$

$$SR^{-} = abs\left(\frac{dV_{HL}(t)}{dt}|_{t=0}\right) = \frac{(V_H - V_L)/C_L}{(R_{MON1} + R_C)//R_{MON2}} \tag{23}$$

The value R_C can be chosen to be larger to obtain the adequate stability, while still keeping a low small-signal settling time [5, 17]. And the slew rate can be improved by the second output stage, and the large-signal slew rate is no longer limited by the compensation resistance R_C. Moreover, the current positive feedback not only pushes the non-dominant pole to be higher (more stable system) but also further improves the driving speed of the output buffer.

3.3 C. Layout verification result

The designed amplifier is dynamically biased from under 5-V supply, and the compensation resistor is set to 600 Ω. We designed layout based on 0.18 μm 1.8 V/5 V BCD process to verify the advantages of the proposed output buffer. Table 1 shows the dimensions of all devices in the buffer with dual output stage.

Based on post-layout simulation, Table 2 gives the results of peak dynamic-feedback current ($I_{nf,\max}$ and $I_{pf,\max}$ for n − /p − different-pair's bias) under a 50-kHz 4-V input step waveform and different load conditions. Approximately 500 × times boost in bias current helps to push away the non-dominate pole for stability concern.

The quiescent current of the proposed buffer can be very small due to the dynamic-current feedback and low-tail-current comparators. Post-layout simulated data shows that the circuit draws only 2.8-μA quiescent current. Because there are hundreds or even thousands of output buffers in source driver for OLED display application, it is important to estimate the sensitivity of the proposed output buffer under different process corners and temperature variations. The post-layout simulations have been carried out at − 10

Table 1 Device sizes used in the proposed output buffer

Device	Dimension (μm/μm or Ω)
MB1, MB2, MB4, MF4	2/1
MB3, MB5	12/1
M2, M3	6 × (6/2)
M1, M4	6 × (36/2)
M5, M6, MF5, MF6	2 × (6/1)
M7, M8, M10, MC2	2 × (2/2)
MC4	2 × (1.8/2)
M9, MC3	2 × (24/2)
MC1	2 × (22/2)
MF1	2 × (12/1)
MF2, MF3	2 × (4/2)
MF4	2/1
MON1	4 × (8/2)
MOP1	4 × (24/1)
MON2	8 × (16/2)
MOP2	8 × (96/2)
R_C	600

Table 2 Post-layout simulation result of buffer's dynamic feedback current with different load capacitances

Current/Time	200 pF	400 pF	600 pF	800 pF	1000 pF
$I_{nf,max}$(μA)	273.6	273.8	274.0	274.0	273.9
$I_{pf,max}$(μA)	280.6	278.8	279.7	279.1	278.3

Table 3 Corner simulation results at different temperatures (C_L = 1 nF)

Corner	TT	FF	SS	SF	FS
t = − 10 °C					
Idd (μA,Vcm = 3 V)	2.80	2.87	2.74	2.79	2.81
SR (V/μs)	7.48	9.26	6.04	8.10	6.71
Settling time (μs,V_{swing} = 4 V)	1.27	0.97	1.57	1.23	1.33
Offset (mV,Vcm = 3 V)	3.52	2.27	2.48	3.41	2.64
t = 27 °C					
Idd (μA,Vcm = 3 V)	2.80	2.87	2.74	2.79	2.81
SR (V/μs)	6.79	8.44	5.47	7.33	6.09
Settling time (μs,V_{swing} = 4 V)	1.38	1.05	1.72	1.34	1.44
Offset (mV,Vcm = 3 V)	3.31	2.23	2.43	3.10	1.75
t = 85 °C					
Idd (μA,Vcm = 3 V)	2.81	2.89	2.75	2.80	2.82
SR (V/μs)	5.93	7.42	4.76	6.38	5.35
Settling time (μs,V_{swing} = 4 V)	1.52	1.15	1.91	1.47	1.58
Offset (mV,Vcm = 3 V)	3.52	2.27	2.48	2.64	3.41

°C, 27 °C and 85 °C, and the results are summarized in Table 3 under 1-nF load-capacitance. We found that the static current only varies within 5%. Meanwhile, input offset of this buffer is within 3.52 mV under 3-V common-mode input voltage. Its slew rate is above 4.76 V/μs to keep small setting time.

As can be observed in Fig. 9, with the amplitude of the input step waveform ranging from 0 to 5 V, the average value for.

the absolute value of the offset voltage is only 2.18 mV, which is very suitable for high-precision displays. The simulation results of transient response and spectrum to a 50-kHz 5-V input sinusoid signal are also provided in Fig. 10. The THD and SNDR are 2.29% and 32.78 dB respectively under the same condition. The spectrum diagram is calculated after sampling 65,536 points of the time domain signal from 0 to 100 ms, and five harmonics are considered for the harmonic power calculation.

4 Silicon results

Figure 11 shows the microphotograph and layout of the dual-output-stage structure buffer. The active area of the main part for the proposed buffer is 52 μm × 59 μm, which is placed in hundreds or thousands for display source driver. Figure 12 depicts the measured tracking behavior of the proposed output buffer driven by 50-kHz full-swing (5 V) triangular wave. With 150-pF load capacitance, it is found that the buffer's output keeps good following performance and fast transient response.

As shown in Fig. 13, the transient response waveform with 50-kHz input step waveform for 150 pF load capacitance is obtained. The phase margin cannot be tested because the output stage and the dynamic-current feedback

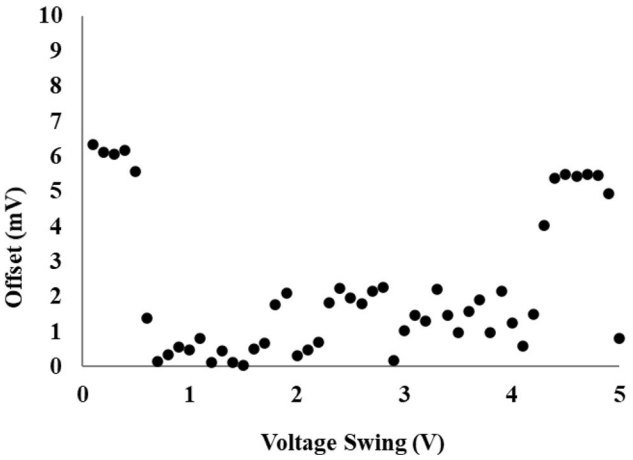


Fig. 9 Post-layout simulation result of offset voltage versus different common-mode input voltages

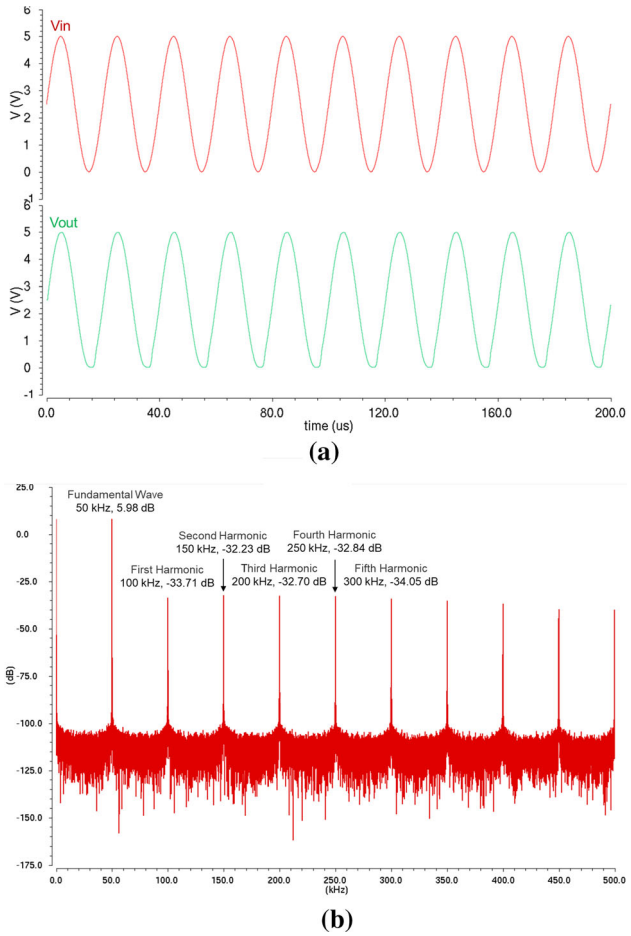


Fig. 10 Simulation results of **a** transient response and **b** spectrum to a 50-kHz 5-V input sinusoid signal

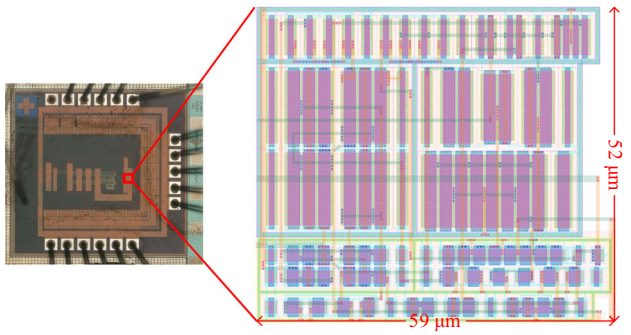


Fig. 11 Microphotograph of the silicon chip and the layout for the dual-output-stage structure buffer

are turned off during the static state. The input-voltage-swing is set to 4 V to better observe the stability, and we evaluate stability from waveform's oscillation during transient. The settling time of the buffer with dual output stage is only 0.32 μs at 99% of the final voltage.

The transient response to the same step-wise input under a large-size capacitive load of 1000 pF, is illustrated in Fig. 14. The proposed buffer with dual output stage

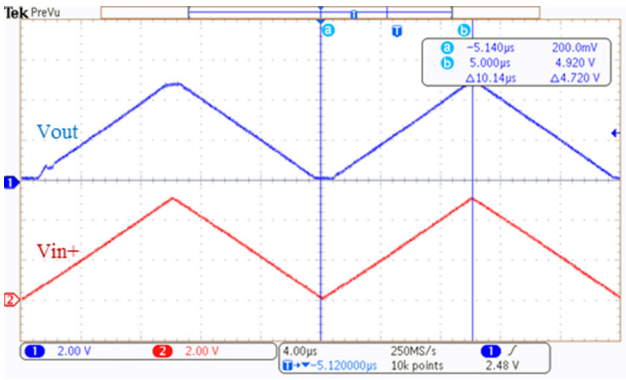


Fig. 12 Measured amplifier transient response to a 50-kHz full-swing input triangular wave

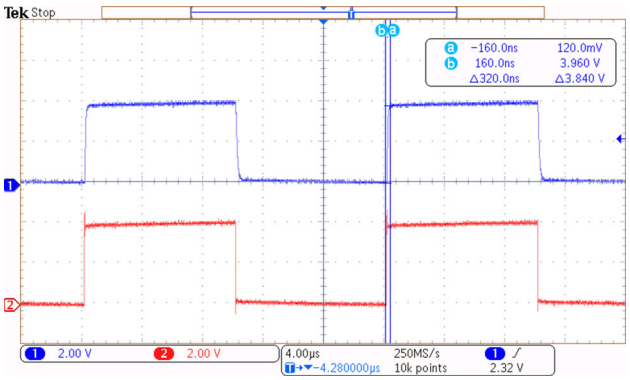


Fig. 13 Measured transient response to a 50-kHz 4-V input step waveform under a 150-pF capacitance of the buffer amplifier with dual output stage

exhibits the settling time of 1.18 µs at 99% of the final voltage, which is only 41% of the single-output-stage structure. For fair comparison, the aspect ratio of the output transistors in the traditional single-output-stage buffer is almost the sum of output-stage transistors in the dual-output-stage buffer. The aspect ratio of the other transistors is also the same, respectively, for both designs.

Finally, for the small-signal performance, Fig. 15 shows the transient response to a 50-kHz 40-mV step-wise input for 1000-pF capacitive load. As can be observed, the output waveform follows the input waveform, and the performance of dual-output-stage buffer is better than the single-output-stage buffer (1.7 µs vs. 2.4 µs).

Table 4 shows the performance comparison. Compared with the state-of-the-art works, this buffer design has better performances in quiescent current, settling time and active area. In Table 2, factors FOM_1 and FOM_2 are used to evaluate the whole buffer performance. FOM_1 is used to compare the performance of buffers by evaluating the tradeoffs between the equivalent capacitor of the OLED panel C_L, the quiescent current I_{DD}, and the settling time T_S. It is defined by

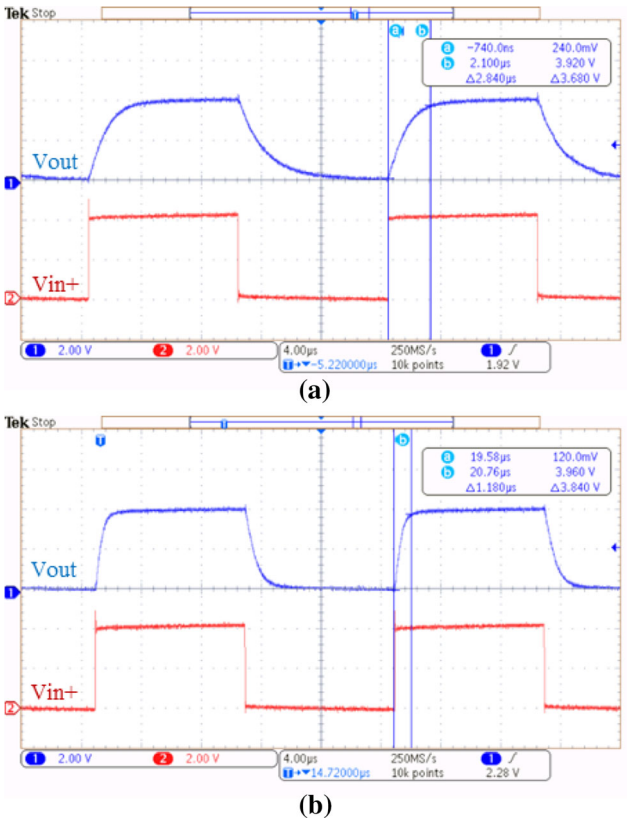


Fig. 14 Measured transient response to a 50-kHz 4-V input step waveform under a 1000-pF capacitance of the buffer amplifier with **a** single output stage and **b** dual output stage

$$FOM_1 = \frac{C_L}{T_S I_{DD}} \tag{24}$$

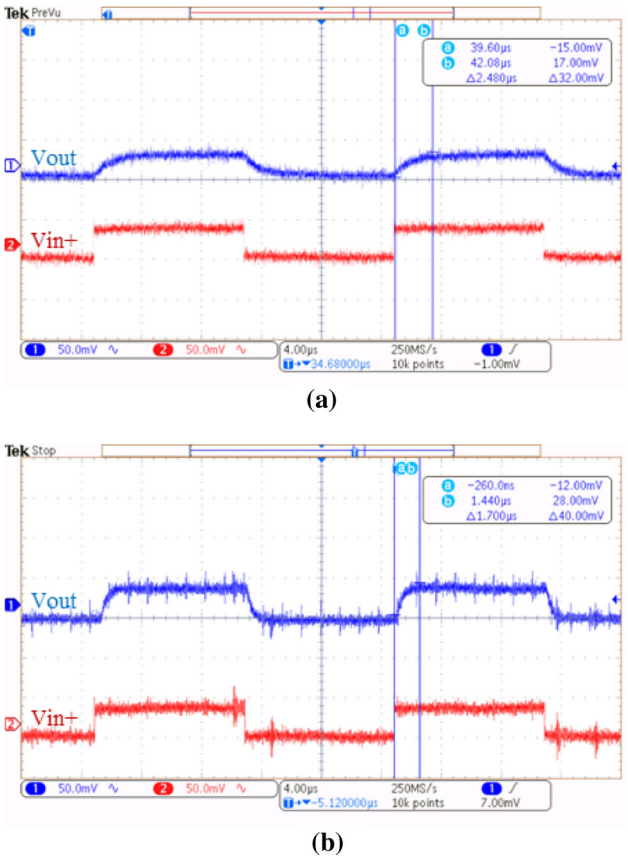
Higher output voltage swing can accommodate higher grey levels of the OLED display. Therefore, V_{swing} has been added in FOM_2. Its basic definition is

$$FOM_2 = \frac{C_L V_{swing}}{T_S I_{DD}} \tag{25}$$

The larger FOM_1 and FOM_2 are, the better performance the output buffer achieves. We use 5 V device in the proposed buffer design (Table 1, VDD-VSS = 5 V), so we don't take the advantage of more advanced CMOS technology (0.18 µm CMOS for 1.8 V core devices). Thus, the process factor is not included into the comparison.

5 Conclusion

We propose a high-speed low-power rail-to-rail output buffer with dynamic-current feedback for OLED display applications. The advantages focus on three aspects: Firstly, we use low-tail-current comparator and cutting off buffer's output stage during the static state to guarantee



(a)

(b)

Fig. 15 Measured transient response to a 50-kHz 40-mV input step waveform under a 1000-pF capacitance of the buffer amplifier with **a** single output stage and **b** dual output stage

low quiescent-power. Secondly, we mitigate the tradeoff between low static-current and fast transient-response by introducing dynamic-current feedback. With a minimized sacrifice of dynamic power during transient, the design allows fast response for buffer's first stage. And it is a way to push away non-dominant pole so as to improve the system stability. Finally, we balance the system stability and large-signal slew-rate flexibly. Using dual-output-stage structure, we can place compensation resistor between them and create one zero to improve phase margin, while the real ON resistance at output terminal is still small enough to guarantee good slew-rate during large-signal transient.

The advantages of the proposed output buffer have been verified based on 0.18 μm process by measuring silicon data. The design shows remarkable performance in quiescent-current (3 μA), settling time (1.18 μs @1 nF capacitive load), and active area (52 μm × 59 μm). Besides, it provides wide range of capacitive load (150 pF to 1 nF). This buffer is suitable for high-resolution, high-refresh-rate, high-precision OLED display applications.

Table 4 Performance summary and comparison

Design	Ref. [5][a]	Ref. [11][a]	Ref. [22][b]	Ref. [25][a]	Ref. [26][a]	Ref. [27][b]	Ref. [28][a]	Ref. [29][b]	Ref. [30][a]	Ref. [15][a]	This work[a]
Technology (μm)	0.35	0.5	0.6	0.6	0.35	0.35	0.35	0.35	0.13	0.35	0.18
V_{DD}(V)	3.3	5	3	5	3.3	3	3.3	3.3	0.7	3	5
Quiescent current (μA)	7	32	3.5	30	6.5	8	3	5	24	1.63	3
Settling time @C_L(μs, pF)	4.1@1000	0.71@1000	1.7@1000	1.3@680	6@40	0.8@1000	1.78@1200	1.5@600	2.6@30,000	1.11@1000	1.18@1000
Output range (V)	0/3.3	0/5	0/3	0.15/4	N.A	0/3	0/3.3	N.A	0/0.7	0/0.7	0/5
Chip size(μm^2)	47 × 57	73 × 91	31 × 30	N.A	33 × 217	25 × 25	54 × 122	2940	2725	5562	52 × 59
FOM_1(pF/(μs*μA))	34.8	44	168	17.4	1	156	225	80	479	553	282
FOM_2 (pF*V/(μs*μA))	115	220	504	67	N.A	468	743	N.A	335	1659	1410

[a]Measurement results
[b]Simulation results

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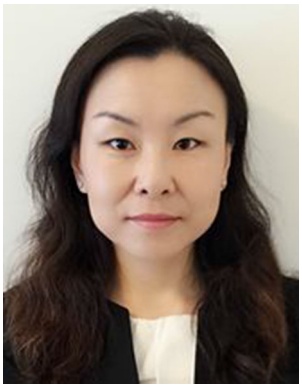

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