Photosensitive polymer reliability for fine pitch RDL applications

Emmanuel Chery, Fabrice F. C. Duval, Michele Stucchi, John Slabbekoorn, Kristof Croes, Eric Beyne

imec Leuven, Belgium emmanuel.chery@imec.be

Abstract—We present the reliability results obtained on a two-metal level copper RDL patterned on a photosensitive polymer with a target pitch below 4 μ m. Our polymer has been submitted to high temperature storage at 150 °C and to temperature humidity stress at 85 °C/85 % RH for 1000 hours. A thermal cycling stress between -50 °C and 125 °C for 1000 cycles was also performed on these samples.

Collected electrical data indicate an increase in the copper wires resistivity and via resistance after 1000 hours at 150 °C. Failure analyses performed on the stressed samples reveal the formation of a copper oxide layer on top of the metal lines and at the bottom of the vias resulting from the presence of water at the interface metal/polymer. The presence of moisture inside the polymer is further confirmed by Fourier-transform infrared spectroscopy (FTIR) measurements. These results emphasize the need of a capping layer on top of the metal lines and reiterate the need of a continuous Ti barrier for a reliable process.

Index Terms—Fine pitch RDL, photosensitive polymer, reliability, high temperature storage, thermal cycling, 3D packaging

I. INTRODUCTION

Interconnects redistribution layers (RDL) are a key enabler for IC heterogeneous integration using advanced packaging technologies. The increasing complexity of integrated systems requires more and more connections to be made between adjacent chips. To achieve this in a minimal number of metal layers, the critical dimensions of the RDL lines must be reduced. [1]-[3]. One promising method uses dual damascene wire patterning of a high resolution photosensitive polymer used as dielectric. In this process, vias and RDL wires are embedded in a barrier inside polymer trenches. Due to the chemical-mechanical polishing (CMP) step of the damascene process, the RDL stack remains flat thus enabling more metal layers to be processed at resolution limit. The requirements on this polymer are high: compatibility with lithography processing, thermal

stability, low moisture uptake and mechanical strength to meet reliability standards. Among them, the moisture uptake is the most critical. H_2O can indeed diffuse easily through the organic matrix of the polymer resulting in the presence of water and hydrated ions at the interface polymer/oxide/metal. In presence of atmospheric oxygen, corrosion of the metal is observed, ultimately leading to polymer delamination [4]–[10].

II. EXPERIMENTAL

A. Technology

This study was performed on patterned samples manufactured on 300 mm silicon wafers. On top of a 200 nm silicon nitride layer, the first layer of polymer is coated, exposed and developed to create the trenches for the first metal layer (M1). Afterwards, a 100 nm Ti layer followed by a 100 nm Cu seed layer are deposited by Physical Vapor Deposition (PVD) processes. The Ti layer is used as an adhesion layer as well as a copper diffusion barrier. A copper electroplating step is subsequently used to grow copper on top of the seed layer to fill the line. After a CMP step to remove the excess copper from the trenches, the second layer of polymer is deposited and the vias are patterned. The third layer of polymer is then added and patterned with the trenches of the second metal layer (M2). The Ti barrier and the Cu seed layers are deposited and copper electroplating is used to fill the via and the M2 trenches at the same time (dual damascene approach). After a CMP step, a final polymer layer is coated and the bond pad areas are exposed. The polymer is removed in these areas, and a protective layer is deposited on top of the copper to prevent corrosion while allowing electrical measurements. Characteristic physical dimensions of this process are presented in Fig.1.

The photosensitive dielectric used in this study is a thermoset phenol-based polymer cured at 200 °C. Its permittivity is 3.7 at 100 kHz and its breakdown field is



Fig. 1: FIB cross-section of the full RDL stack.



Fig. 2: IV characteristics performed on a fork-fork structure at M2 level on two different dice. The distance between the electrodes is around 1 μ m as shown on Fig. 1. The measured breakdown voltage is around 180 volts.

around 1.8 MV/cm as shown on Fig.2. The target pitch of this process is below 4 μ m.

B. Experiments

Using a polymer as a dielectric in an RDL process induces serious reliability challenges such as moisture uptake, polymer aging or mechanical issues. To trigger these mechanisms, our process was submitted to three different reliability stresses. High temperature storage (HTS) at 150 °C was performed for 1000 hours to stimulate the diffusion of copper between the metal lines as well as the aging of the polymer. The impact of humidity trapping was studied using 1000 hours of temperature humidity stress (TH) at 85 °C/85 %RH. Finally, potential mechanical issues in the process were investigated with a thermal cycling stress (TC) consisting of 1000 cycles between -50 °C and +125 °C.

Four read-outs were performed (after 72, 168, 500 and 1000 hours of stress or cycles) to monitor the impact of these stresses on some key device parameters. The monitoring procedure was performed at room temperature and consisted of an optical inspection, followed by wafer-level electrical measurements. The data collected include capacitance values and leakage current of the fork-fork capacitors, as well as resistance values for various metal lines and via structures. Finally, the FTIR spectrum of the polymer was used to trace the moisture uptake in the stack.

III. RESULTS AND DISCUSSION

A. Optical inspection

At each read-out, an inspection of the wafers was performed using an optical microscope. The samples submitted to TH and TC stresses did not reveal any abnormalities. On the contrary, a strong coloration of the metal lines is observed after 1000 hours of HTS stress at 150 °C as shown in Fig. 3. In the literature, metal line coloration is reported after 48 hours [9] and after 200 hours [7] of HAST stress (130 °C & 85 %RH) when a polyimide polymer is used to encapsulate the metal lines. The coloration is subsequently associated with copper corrosion [7]. Oppositely, copper lines surrounded by polyimide do not corrode when exposed to TH stress (85 °C & 85 %RH) for 1000 hours [4].

Furthermore, a darkening of the polymer after HTS is observed on Fig. 3b. This change in coloration most likely results from the oxidation of the polymer at high temperature.

B. Electrical results

The integrity of the polymer was assessed using capacitance and leakage measurements, while the stability of the interconnects was appraised through metal resistivity variation and contact resistance monitoring.

Fig. 4 shows the relative increase with time of the capacitance value for the fork-fork structures. An increase of the capacitance value is observed for the unstressed reference samples exposed only to the natural humidity of the laboratory environment. This effect is presumably



Fig. 3: a) Optical inspection of the fork-fork structures before stress. M1 level is on the left of the pad array. M2 level is on the right. b) The same structures after 1000 hours HTS at 150 °C. Traces of corrosion have been observed on the metal line after the HTS stress.

due to moisture uptake inside the polymer resulting in a change of permittivity. M2 level is less impacted (~ 2.5 %) compared to the M1 level (~ 7.5 %). This difference most likely reflects the dynamic nature of the polymer-air interface, where humidity is easily adsorbed and subsequently diffused in the polymer but also easily desorbed when the relative humidity of the environment is changing. Deeper inside the polymer, at M1 level, the absorbed water is more stable allowing a steady increase of the water content.

In all likelihood, the absorption of water inside the polymer explains the augmentation of capacitance value observed after TH and TC stresses where a humid environment is involved. Indeed during the TC stress, condensation from the residual humidity was observed on the sample. Nevertheless, water absorption cannot occur during HTS where the environment is drying the polymer. In this case, the increase is assumably related to a change in the chemical structural properties of the polymer, resulting in an increase of the permittivity.

The polymer insulation properties have been investigated using current-voltage characteristics performed between 95 and 125 volts on a M2 fork-fork structure with a spacing of 2 μ m between the forks. In this range of voltages, the conduction mechanism is triggered and the leakage current is above the SMUs noise level. As presented in Fig. 5, the leakage current did not increase after the different stresses and stays below 1 pA· μ m⁻¹. Similar results have already been reported for various polymers with thicknesses ranging between 2 and 6 μ m [8], [11], [12].

Via robustness against stress is another important indicator of the overall process quality. Fig. 6 shows the cumulative distributions of the resistance values for various via sizes. The impact of the TH and TC stresses



Fig. 4: Relative evolution of fork-fork structure capacitance values with stress time, measured at M1 and M2 levels for the different stresses.



Fig. 5: Leakage current as a function of the applied voltage for a fork-fork structure at M2 level with a spacing of $2 \mu m$. No increase of the leakage current after the stresses is observed.

is limited and the yield remains above 90 % after these stresses. The TC stress resulted in a small decrease of the via resistance value for the 5 μ m vias, probably due to a copper curing process. On the contrary, an increase of the resistance value by a factor 100 to 1000 is observed after HTS. Smaller vias are more impacted than larger ones, likely resulting from a corrosion process at the interface via-metal 1.

Via reliability was furthermore assessed using interwoven daisy chains containing 450 vias connected in serie. As shown in Fig. 7, interwoven daisy chains yield is above 95 % before stress. After the stress, on the



Fig. 6: Cumulative probability distributions of the via resistance values after 1000 hours or cycles of stress for three different via sizes (3 to 5 μ m). An increase of the resistance value by a factor 100 is observed after the HTS stress. The smaller vias are more impacted than the larger ones.



Fig. 7: Cumulative probability distributions of the via interwoven daisy chain resistance values after 1000 hours or cycles of stress for three different via sizes (3 to 5 μ m). The chains are made of 450 vias in serie.

other hand, the yield is drastically reduced independently of the via size. A clear dependency on the via size is observed for HTS stress with smaller vias being more impacted than larger vias. Again, this is pointing in the direction of a corrosion issue at the interface via-metal 1.

Metal resistivity was measured on meander structures with a metal width varying from 2 to 5 μ m. Fig. 8 presents the relative increase of resistivity after the stresses. An increase of the resistivity below 5 % is



Fig. 8: Relative increase of the metal resistivity after 1000 hours or cycles of stress measured at M1 and M2 level as a function of the line width.



Fig. 9: Impact of the metal width on the corrosion mechanisms active at M1 level. Larger metal lines (on the right) benefit from an "umbrella effect", reducing the atmospheric oxygen presence near the metal surface and thus slowing down the corrosion (in red).

measured after TC and TH stresses. However, after HTS, a resistivity increase around 10 % and 15 % for M1 and M2 respectively is detected. Whereas at M2 level the increase is mostly independent of the metal width, wider lines are less impacted at M1 level. This change in the metal resistivity is likely associated with metal corrosion as discussed in section III-A. As M1 and M2 meanders of the same width are stacked, wide M1 meanders benefit from an "umbrella effect", slowing down the diffusion of atmospheric oxygen toward the metal surface and therefore reducing the corrosion rate (Fig. 9).

C. FTIR

To confirm and monitor the moisture uptake inside the polymer exposed only to ambient atmosphere, Fourier



Fig. 10: Relative variations in the FTIR absorbance at wavenumber 3400 cm⁻¹ for a wafer exposed to ambient atmosphere. Wavenumber 3400 cm⁻¹ reflects the water concentration inside the polymer.

Transform Infrared (FTIR) spectroscopy was used. The absorbance spectrum was acquired at each read-out time between 400 and 4000 cm⁻¹ on a Thermo Scientific Nicolet 6700 FT-IR Spectrometer on a reference wafer. This sample consists of a 3 μ m thick blanket layer of polymer on top of a silicon substrate, stored in the laboratory at ambient atmosphere.

Moisture uptake is characterized at wavenumber 3400 cm⁻¹ after normalization of the data. Results are presented on Fig. 10. A steady increase of the absorbance with time is observed thus confirming the moisture uptake from the atmosphere. These measurements are in good agreement with the electrical results presented in section III-B where the increase of capacitance value for the reference unstressed samples was attributed to moisture uptake (Fig. 4). The increase in the response signal (absorbance or capacitance value) is in the same order of magnitude with both methods.

D. Failure analysis

To understand the failure mechanisms, Focused Ion Beam (FIB) cross-sections have been performed on various stressed devices. Fig. 11 presents the cross-section of a M1 line after 1000 hours of TH stress (Fig. 11a) and after HTS at 150 °C (Fig. 11b). No abnormalities are observed after the TH stress. On the contrary, after HTS, a new layer appeared on top of the line and voids are observed at the interface between this layer and the metal. Energy-dispersive X-ray spectroscopy (EDX) analyses were performed in this area. Results are shown



Fig. 11: FIB cross-section analysis of the metal lines at M1 level. a) After the 1000 hours of temperature humidity stress. b) After 1000 hours of high temperature storage. A thick layer of copper oxide has appeared on top of the line. Voids are noticed at the interface metal oxide.

in Fig. 12. The EDX spectra of copper shows a weak but evident signal at the top of line, whereas the oxygen signal starts exactly at the interface metal-polymer. The new layer on top of the metal line is therefore most likely composed of oxygen and copper, revealing the presence of a copper oxide layer, as suspected after the optical inspection (Section III-A and Fig. 3). Similar results are observed on the M2 lines.

Electrically, a resistivity increase around 10 and 15 % was measured after HTS at M1 and M2 level as presented in Fig. 8. Assuming a line height of 2 μ m and 1.5 μ m (M1 and M2 level respectively), a missing layer of copper around 200 to 225 nm is expected. Fig. 11b reveals that the newly created oxide layer thickness is around 330 nm, resulting in a ratio between the missing copper and the new oxide layer thickness in the vicinity of 1.5 to 1.7. These values are in good agreement with the results from Lee and Yu where a ratio 1.79 was reported for a polyimide on copper system [4].

It is important to note that the diffusion of copper is only observed at the top of the metal lines, where the line is not protected by the Ti barrier. For a reliable RDL process, a capping layer at the top of the metal line will therefore be needed. Indeed, while working on a polyimide, Shoji et al. demonstrated the possibility to mitigate the void creation by enhancing the mechanical properties of the polymer-metal interface [8]. Nevertheless, copper diffusion in the polymer, resulting in the creation of an oxide layer, could not be avoided [8], [9]. To prevent this diffusion, Kudo et al. have proposed an enhanced RDL stack where a bi-layer inorganic dielectric is used as a diffusion barrier between the metal



Fig. 12: EDX spectra of the main atomic species present in the process. The presence of copper oxide at the top of the metal line is revealed by the sharp oxygen signal in this region, associated with a diffuse copper signal.

lines and a photosensitive polyimide. After 200 hours of HAST stress (130 °C & 85 %RH), copper corrosion is not observed [7]. Another solution includes the use of a self aligned copper silicide barrier [13]. In both cases, the authors noticed a positive improvement of the electromigration performances [7], [13].

Cross-section analyses were also performed on the kelvin via structures. Results are presented in Fig. 13. Again, no abnormalities are observed in the via after the TH stress (Fig. 13a). However, strong signs of corrosion are detected in the lower part of the via after the HTS stress at 150 °C (Fig. 13b and Fig. 13c). Furthermore, a continuous copper oxide layer is present between the via and M1. Finally, voids are noticed at the interface viapolymer and on the top of the metal lines. The presence of corrosion at the bottom of the via is the signature of a sub-optimized Ti barrier deposition process in this region, most likely resulting in a discontinuous Ti layer, and allowing the exposure of copper to moisture.

Copper oxide growth is diffusion-driven process where copper atoms have to diffuse through the oxide layer to



Fig. 13: FIB cross-section analysis of a 3 μ m via. a) After 1000 hours of temperature humidity stress. b) After 1000 hours of high temperature storage. A thick layer of copper oxide has appeared on top of the metal lines and at the foot of the via. Voids are noticed at the interface metal oxide. c) Magnified view of the interface via-metal 1. A continuous layer of oxide is present under the via.

get oxidized. As thick oxide layers are slowing down the diffusion, a self-limiting growth process is observed [4], [14]. Consequently, an approximately constant oxide thickness is expected between the via and the metal 1 line when the system is fully oxidized. As such, a constant high contact resistance for the failing vias is foreseen as shown in Fig. 6. Copper oxide formed by thermal oxidation at 150 °C is characterized by a n-type conductivity with an electrical resistivity between $4 \cdot 10^{-2}$ and $10^{-1} \Omega \cdot \text{cm}$ [15], [16]. Fig. 13c reveals a minimal oxide thickness around 80 to 90 nm under the via. Considering an electrically active region around $1 \,\mu\text{m}^2$, this resisitivity range would lead to a contact resistance value in the order of 10 to 100 ohms. These estimations are relatively close to the resistance values measured after HTS shown on Fig. 6. As the oxidation proceeds from the outside of the via toward its center, larger vias may still not be fully oxidized after 1000 hours at 150 °C. In the absence of an oxide layer fully covering the via-metal 1 interface, the contact resistance value increase remains limited until the contact area becomes marginal [17], [18]. This

phenomenon explains the bimodal distributions of the resistance values after HTS stress as shown on Fig. 6 (4 and 5 μ m vias).

IV. CONCLUSION

A dual damascene RDL process with a photosensitive polymer, two metal levels and a target pitch below 4 μ m was submitted to reliability testing. The presence of a polymer in the stack introduces serious challenges highlighted by our studies. In association with high temperatures, atmospheric oxygen diffusing though the polymer matrix enables the corrosion of the metal lines and vias, inducing an increase of their resistance, ultimately resulting in via yield loss. In addition, moisture uptake in the stack was demonstrated through FTIR analyzes and capacitance measurements.

For a reliable RDL architecture with the tested photosensitive polymer, our analyzes emphasize the need of developing a capping solution to protect the metal lines against copper diffusion and corrosion. Ti barrier continuity at the via sidewall is also essential for reliability and requires further process optimization.

ACKNOWLEDGMENT

Data analyzes were performed using R version 3.6.0 [19] in association with the Tidyverse ecosystem [20].

In addition, the authors would like to thank the different teams in imec that have been involved in this study.

REFERENCES

- [1] J. H. Lau, *Fan-Out Wafer-Level Packaging*. Springer Singapore, 2018.
- [2] W. W. Flack, R. Hsieh, H.-A. Nguyen, J. Slabbekoorn, C. Lorant, and A. Miller, "One micron redistribution for fan-out wafer level packaging," in *Electronics Packaging Technology Conference (EPTC)*. IEEE, dec 2017.
- [3] W. W. Flack, R. Hsieh, H.-A. Nguyen, J. Slabbekoorn, S. Suhard, A. Miller, A. Hiro, and R. Ridremont, "One micron damascene redistribution for fan-out wafer level packaging using a photosensitive dielectric material," in *Electronics Packaging Technology Conference (EPTC)*. IEEE, dec 2018.
- [4] H. Lee and J. Yu, "Study on the effects of copper oxide growth on the peel strength of copper/polyimide," *Journal of Electronic Materials*, vol. 37, no. 8, pp. 1102–1110, may 2008.
- [5] R. Posner, O. Ozcan, and G. Grundmeier, "Water and ions at polymer/metal interfaces," in *Advanced Structured Materials*. Springer Berlin Heidelberg, 2013, pp. 21–52.
- [6] H. Noma, K. Okamoto, K. Toriyama, and H. Mori, "HAST failure investigation on ultra-high density lines for 2.1D packages," in *International Conference on Electronic Packaging and iMAPS All Asia Conference (ICEP-IAAC)*. IEEE, apr 2015.
- [7] H. Kudo, R. Kasai, J. Suyama, M. Takeda, Y. Okazaki, H. Iida, D. Kitayama, T. Sasao, K. Sakamoto, H. Sato, S. Yamada, and S. Kuramochi, "Demonstration of high electrical reliability of sub-2 micron cu traces covered with inorganic dielectrics for advanced packaging technologies," in *Electronic Components* and Technology Conference (ECTC). IEEE, may 2017.

- [8] Y. Shoji, H. Araki, Y. Koyama, Y. Masuda, K. Hashimoto, K. Isobe, R. Okuda, and M. Tomikawa, "Higher reliability for low-temperature curable positive-tone photosensitive dielectric materials," in *CPMT Symposium Japan (ICSJ)*. IEEE, nov 2017.
- [9] H. Araki, Y. Shoji, Y. Masuda, K. Hashimoto, K. Matsumura, Y. Koyama, and M. Tomikawa, "Fabrication of redistribution structure using highly reliable photosensitive polyimide for fan out panel level packages," in *International Wafer Level Packaging Conference (IWLPC)*. IEEE, oct 2018.
- [10] S. Moreau, N. Allouti, C. Ribiere, J. Charbonnier, D. Bouchu, J.-P. Michel, N. Buffet, and P. Chausse, "Passivation materials for a reliable fine pitch RDL," in *Electronic Components and Technology Conference (ECTC)*. IEEE, may 2018.
- [11] X. Wei and Y. Shibasaki, "A novel photosensitive dry-film dielectric material for high density package substrate, interposer and wafer level package," in *Electronic Components and Technology Conference (ECTC)*. IEEE, may 2016.
- [12] T. Komine, A. Tanimoto, Y. Aoki, M. Kimura, Y. Hamano, and M. Sasaki, "Low-temperature curable dielectric materials with higher reliability," *Journal of Photopolymer Science and Technology*, vol. 31, no. 5, pp. 625–628, jun 2018.
- [13] K. Chattopadhyay, B. Schravendijk, T. Mountsier, G. Alers, M. Hornbeck, H. Wu, R. Shaviv, G. Harm, D. Vitkavage, E. Apen, Y. Yu, and R. Havemann, "In-situ formation of a copper silicide cap for TDDB and electromigration improvement," in *International Reliability Physics Symposium Proceedings*. IEEE, 2006.
- [14] J. C. Yang, B. Kolasa, J. M. Gibson, and M. Yeadon, "Selflimiting oxidation of copper," *Applied Physics Letters*, vol. 73, no. 19, pp. 2841–2843, nov 1998.
- [15] V. Figueiredo, E. Elangovan, G. Gonçalves, N. Franco, E. Alves, S. Park, R. Martins, and E. Fortunato, "Electrical, structural and optical characterization of copper oxide thin films as a function of post annealing temperature," *physica status solidi (a)*, vol. 206, no. 9, pp. 2143–2148, sep 2009.
- [16] L. D. L. S. Valladares, D. H. Salinas, A. B. Dominguez, D. A. Najarro, S. Khondaker, T. Mitrelias, C. Barnes, J. A. Aguiar, and Y. Majima, "Crystallization and electrical resistivity of Cu₂O and CuO obtained by thermal oxidation of cu thin films on SiO₂/Si substrates," *Thin Solid Films*, vol. 520, no. 20, pp. 6368–6374, aug 2012.
- [17] J. A. Greenwood, "Constriction resistance and the real area of contact," *British Journal of Applied Physics*, vol. 17, no. 12, pp. 1621–1632, dec 1966.
- [18] L. Kogut and K. Komvopoulos, "Electrical contact resistance theory for conductive rough surfaces," *Journal of Applied Physics*, vol. 94, no. 5, pp. 3153–3162, sep 2003.
- [19] R Core Team, R: A Language and Environment for Statistical Computing, R Foundation for Statistical Computing, Vienna, Austria, 2019. [Online]. Available: https://www.R-project.org/
- [20] H. Wickham, M. Averick, J. Bryan, W. Chang, L. McGowan, R. François, G. Grolemund, A. Hayes, L. Henry, J. Hester, M. Kuhn, T. Pedersen, E. Miller, S. Bache, K. Müller, J. Ooms, D. Robinson, D. Seidel, V. Spinu, K. Takahashi, D. Vaughan, C. Wilke, K. Woo, and H. Yutani, "Welcome to the Tidyverse," *Journal of Open Source Software*, vol. 4, no. 43, p. 1686, nov 2019.