High yield and process uniformity for 300 mm integrated WS_2 FETs

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Abstract

We demonstrate an integrated process flow on full 300mm wafers with monolayer WS_2 channel. WS_2 is a 2D semiconductor from the transition metal dichalcogenide family and holds promise for extreme gate length scaling. We report here on integration challenges and optimize process uniformity for a single-device yield higher than 90% across wafer. These transistors and integration flow are shown to be compatible with H_2 anneal of at least 400 C and hence in principle suitable for hybrid integration in the BEOL.

Keywords: WS_2, TMDC, 2D, CVD, 300mm, FET, integration

Introduction

2D materials and in particular transition metal dichalcogenides are identified as promising channel materials for future scaled nodes [1-5]. Typical record-setting devices are fabricated in a lab environment, using fab incompatible techniques like flake transfer and lift off. However, 300mm fab-compatible process modules are needed as the technology is maturing. This paper reports on 300 mm double gated WS_2 FET devices where all used process steps, including 2D growth, damascene contact and gate formation, are fab compatible [2-5]. This paper focusses on integration challenges, yield optimization, and within-wafer (WIW) uniformity.

Integration and basic device operation

Fig.1a,b show a COVENTOR-based process simulation of the double gated WS_2 device, and a schematic of the final device. Details on the used process steps and critical imitations are described elsewhere [2-5]. A 300 mm deposited 750°C CVD WS_2, with smaller grain size is used [3-6]. Many of the process choices are intended to limit mechanical stress, i.e. the absence of a spacer and the related use of a damascene top gate. A TEM of the resulting device with Lg=22 nm is shown in Fig.2a,b.

IV curves for a 22 nm top gate device with back and top gate EOT of ~57 and 3.5 nm with independent back and front gate sweeps are show in Fig.3-4. Ambipolar reconfigurable [7] behavior is observed in both cases, which indicates an unpinned Fermi level. Either the top or the back gate can be used to select the dominant branch. Back gated Id vs/ L_{ch} dependence (Fig.5) indicates a channel-limited n-type current with effective mobility of ~ 0.5 cm^2/Vs and a contact-limited p-type current. Despite the mobility limitations by the small grains in the WS_2 channel [8], the performance allows for the collection of wafer-level properties. Improved device behavior can be expected by replacing the channel by improved material at a later stage.

Wafer yield and effect of H_2 anneal.

To avoid delamination of the WS_2 during active patterning, a Spin on Carbon/Spin on Glass (SoC/SoG) soft mask based active patterning was introduced [3-4]. The yield is 95 % and 91 % for n-type and p-type single transistor operation, respectively (Fig.6). In the context of future hybrid integration, we demonstrate process compatibility for a H_2 anneal with BEOL-integrated WS_2 devices build on top of a different FEOL. Selected wafers are submitted to 30 minutes 10% H_2 anneal at 5 atm in the 200-400°C temperature range after encapsulation by the ILD0 oxide (stage 2 in Fig.1a). Up to 300°C no significant change is observed for the n and p current, while for 400°C there is a minor improvement in Ion and SS that is accompanied by a minor increase in Vt (Fig.7-8). The yield of the wafers is not affected by the H_2 anneal (Fig.9).

We demonstrate that Si defects deeper in the stack can be passivated with the H_2 anneal without degrading the WS_2 channel above. For some devices, the Silicon back gate is implanted with 10^{19} at/cm^3. This implantation causes a Vt shift of +20V (Fig.8) but recovers after H_2 anneal due to Si passivation, without degrading the WS_2 performance. This implies that Si based FEOL under 2D in the BEOL can be passivated.

Within-wafer uniformity improvement

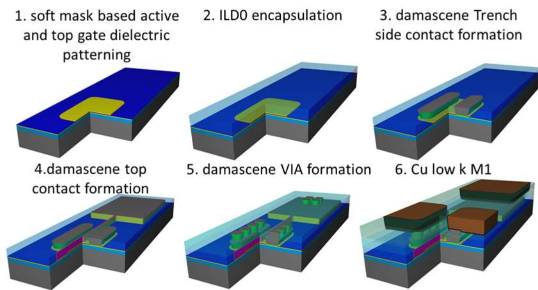
There is significant within-wafer (WiW) nonuniformity in Vt, exceeding the device-to-device variability, when using SiO_2 as a hard mask for the active patterning [4]. The radial Vt distributions in Fig.10a show especially the widest (10µm) devices have a negative Vt shift towards the wafer edge. Using the low stress SoC/SoG soft mask the WiW uniformity improves (Fig.10b) and the channel width dependence reduces. The WiW uniformity improves even more by using an alternative contacting scheme, where the long trench contacts are changed to distributed round contacts (Fig.11,1c). This results in uniform Vt over the wafer and the channel width dependence reduces again (Fig.10c,12). These two observations are likely caused by reduced mechanical stress near the channel region. This is confirmed in Fig.13 where focused ion beam (FIB)-based lamella preparation causes the WS_2 bottom interface to delaminate, and the layers buckle up due to stress relaxation. This does not occur during one-sided FIB cuts, used for within-line inspections. Adhesion loss at the weaker van der Waals interface also occurs as rip out during chemical mechanical polishing (CMP) on gated areas with large lateral extent (Fig.14).

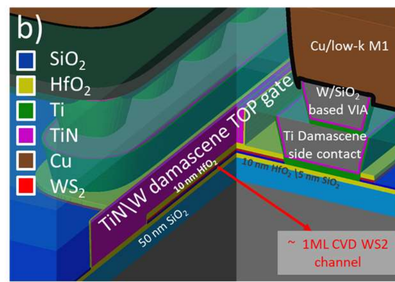
In summary, the observations of (1) less delamination when changing oxide hard mask to soft mask, (2) less delamination during CMP of smaller features, (3) more uniform Vt for distributed round contacts and reduced width dependence, are all consistent with a reduction in built-in stress or better redistribution of stress.

TEM in Fig.2c shows the trench contacts connect to the WS_2 edge (side contacts) while the round contacts connect to the WS_2 top (top contacts), which could hint to a different injection mechanism having an impact on the WiW uniformity.

Conclusions

We demonstrate a damascene top gate and contact, double gated WS_2 transistor flow with a single transistor yield above 90%. The radial uniformity is improved by limiting the mechanical stress of the materials used, and further improved by using distributed top contacts. The resulting devices are compatible with H_2 anneals of at least 400°C, making the devices suitable for hybrid 2D integration in the BEOL.





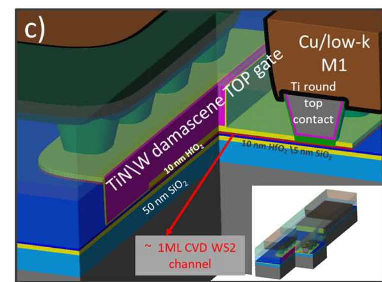
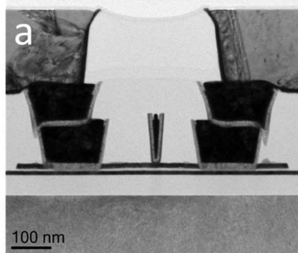
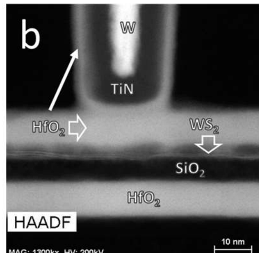


Fig.1: (a) COVENTOR process simulation of the key process modules (b) representation of the obtained double-gated WS_2 device with a damascene TiN top gate and a damascene Ti side contact. The Si wafer is used as back gate. (c) representation of the of obtained alternative double gated WS_2 device with round contacts.





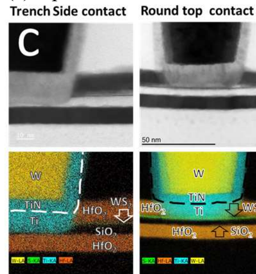


Fig 2: (a) TEM of double gated WS_2 device (W = 1 µm) with trench side contacts, (b) HAADF (contrast proportional to atomic number) zooms of the gate area. The Lg is 22 nm including the 3 nm HfO_2 liner (c) TEM (top row) and EDS maps (bottom row) of the contact area for the devices with side trench contacts and round top contacts. The respective side and top contact can clearly be seen in the EDS maps.

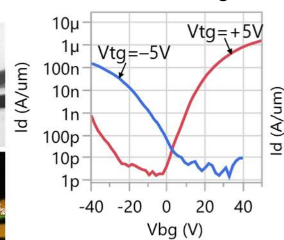


Fig.3: Back gate sweep transfer characteristics show n-type operation for Vtg=+5V and p-type for Vtg=−5V. W_{ch}=1µm, L_{ch}=240nm, L_{tg}=22nm, V_d=1V

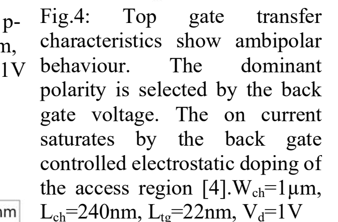


Fig.4: Top gate transfer characteristics show ambipolar behaviour. The dominant polarity is selected by the back gate voltage. The on current saturates by the back gate controlled electrostatic doping of the access region [4].W_{ch}=1µm, L_{ch}=240nm, L_{tg}=22nm, V_d=1V

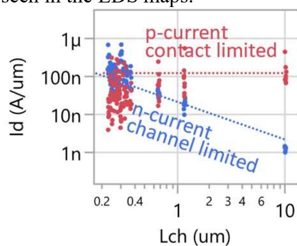


Fig 5: n-current (Vbg=50V, Vtg=3V) scales inversely proportional with channel length and is hence channel mobility limited. P-current (Vbg= −50V, Vtg= −3V) is contact limited.

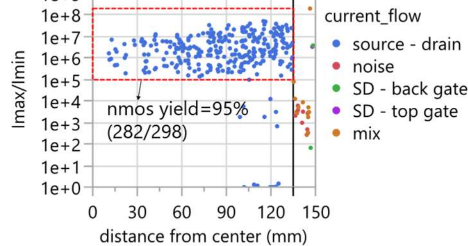


fig.6: The nmos yield is 95%, when excluding the 1.5cm edge where WS_2 is removed to avoid water-intercalation-based bevel and edge delamination. A device is considered yielding if there is a dominant source to drain current with $I_{max}/I_{min} > 10^5$.Wch=1µm, Lch=240nm.

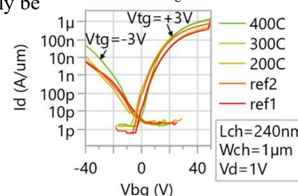


Fig 7: 30 minutes 10% H anneal at 5 atm up to 400 C does not degrade transfer characteristics. Small SS improvement in p- and n-current observed for 400 C anneal.

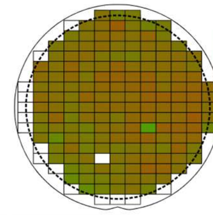


Fig.12: Near-uniform back-gate Vt map for wafer with SoG/SoC patterning and round contacts, shown in Fig.10c. W_{ch}=10µm, L_{ch}=240 nm, L_{tg}=22nm, V_d=1V.

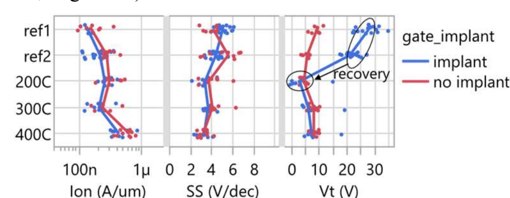


Fig 8: H anneal at 400C gives minor improvement of transistors characteristics. Implanting the Si back gate causes a large Vt shift but is recovered by H anneal, likely passivating traps at the Si/SiO_2 interface.

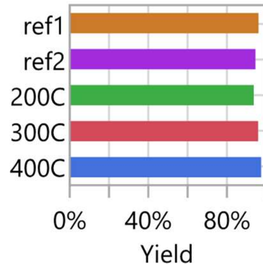


Fig.9: High operational yield is maintained after hydrogen anneal.

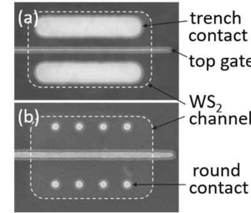


Fig.11: SEM inspection of devices with (a) trench contacts and (b) round contacts after top gate CMP.

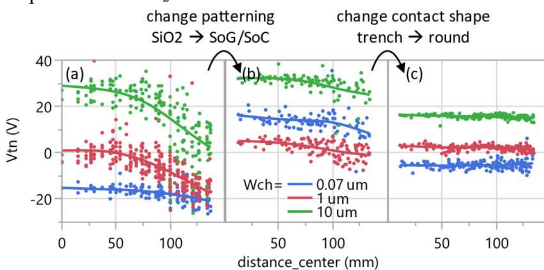


Fig 10: (a) There is a large nonuniformity in back-gate Vtn using oxide hard mask for active patterning [4], especially for wide channels (L_{ch}=240nm, Wch=10µm). (b) This improves by changing to SoC/SoG soft mask (c) and again by changing trench contacts to round contacts (causes longer L_{ch}=406nm). These improvements are most likely related to less built-in stress.

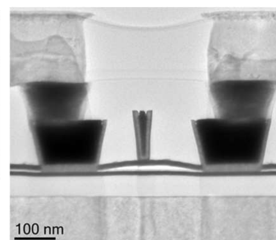


Fig 13: Stress-induced buckling is frequently observed on double sided FIB lamella (TEM preparation W = 10 µm). The WS_2 detaches from the growth surface.

Fig.14: local gate rip out is observed on large gate areas (here 96 um squares). This can be avoided by appropriate design rules.

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