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Jonas Keukelier,[1,a] Karl Opsomer,[2] Wouter Devulder,[2] Sergiu Clima,[2] Ludovic Goux,[2] Gouri Sankar Kar,[2] and Christophe Detavernier[1,b]

AFFILIATIONS

[1]Department of Solid State Sciences, Ghent University, 9000 Ghent, Belgium
[2]Imec, 3001 Leuven, Belgium

[a]**Electronic mail:** jonas.keukelier@ugent.be
[b]**Author to whom correspondence should be addressed:** Christope.Detavernier@ugent.be

ABSTRACT

In order to make 3D crossbar memory architectures viable, selector elements with highly non-linear current–voltage characteristics are required. Ovonic Threshold Switching (OTS) is a highly non-linear phenomenon observed in amorphous chalcogenides, such as GeSe, that shows promise for application in selectors. In this paper, the impact of alloying with metallic (Zr), metalloid (B, Sb), and non-metallic (C, N) elements as a function of their concentration on the thermal stability and switching properties of alloyed GeSe layers is studied. In the case of the thermal stability analysis, the key parameter that is tracked is the crystallization temperature (T_c) of the as-deposited amorphous films since OTS only occurs in amorphous materials. Using a simple metal–insulator–metal type test structure where the bottom electrode is scaled to 6 μm, the OTS properties of the alloyed layers are also compared. The pristine leakage current (I_{pris}), the first fire voltage (V_{FF}), and the threshold voltage (V_{th}) were determined using DC and pulsed (AC) measurements. Results indicate that C alloying in combination with sufficiently high nitrogen incorporation can extend the thermal stability above 600 °C with only low dependence on the C content. Among the metallic and metalloid elements, crystallization temperature is strongly dependent on alloying concentration. In general, larger concentrations are needed to obtain a T_c above 400 °C as compared to CN alloying. Electrical characterization indicates strong dependence of the first fire voltage and the leakage current on the metallicity of the alloying element with only small to moderate concentrations required to influence electrical properties.

I. INTRODUCTION

3D crossbar memory architectures are an increasingly popular way of achieving greater memory densities without the need to further reduce the size of each memory element.[1–5] Such designs instead consist of multiple layers of memory cells sandwiched between opposite rows of parallel wires, stacked on top of each other. By expanding in the third dimension, memory capacity is no longer limited by the available wafer space. Such designs, however, require that at each interconnection, the memory device is accompanied by an additional component, referred to as a selector, which has a highly non-linear current–voltage (IV) characteristic. These selectors are necessary to eliminate the sneak current paths through neighboring cells alongside the energized wires of a particular memory cell selected for reading or writing.[6,7] These neighboring cells experience a part of the applied voltage and may disturb the reading and writing operation by passing additional current.

Certain amorphous chalcogenides have been shown to exhibit non-linear IV behavior, which makes them perfectly suited to act as selector layers. The phenomenon is referred to as Ovonic Threshold Switching (OTS) and was first discovered by Ovshinsky.[8] While the phenomenon has been known for several decades, the exact mechanisms that govern the conduction and switching are still debated. In Fig. 1, typical OTS IV behavior is illustrated. The layer starts out in a state of high resistance referred to as the HRS. The glassy chalcogenide network gives rise to many

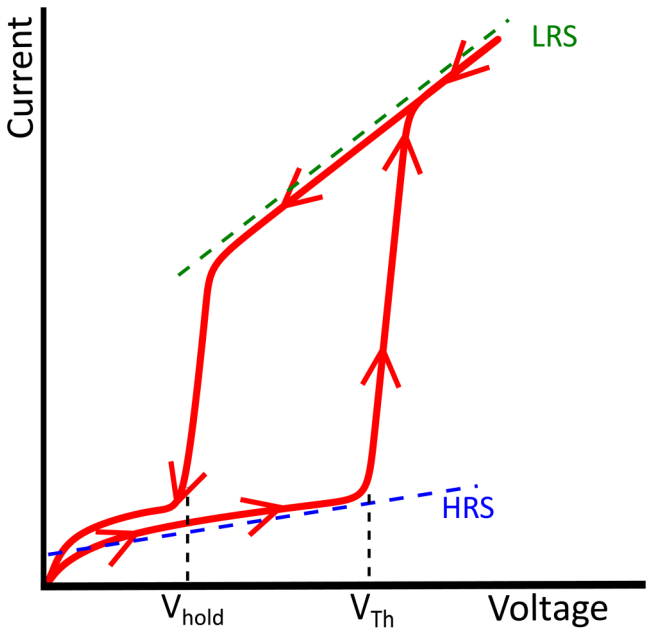
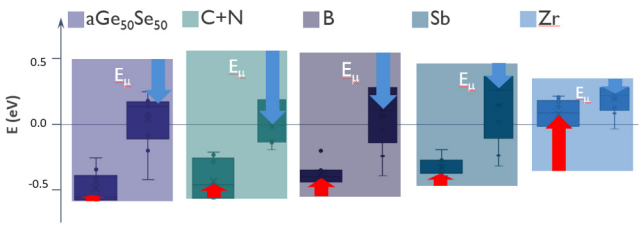


FIG. 1. Illustration showing the typical IV behavior of an OTS switching layer. The threshold voltage (V_{th}) where the layer switches between the high resistive state (HRS) and the low resistive state (LRS) is marked as well as the hold voltage (V_{hold}) where the layer switches back. Arrows indicate the direction of the IV sweep.

localized defects, and conduction in this state is dominated by hopping transport between trap states as well as excitations between localized trap states and the conduction band known as Poole–Frenkel conduction.[9] At a certain threshold voltage, the layer switches to a low resistive state (LRS) with a more ohmic-like conduction. This switching process has long been considered a purely electrical phenomenon due to its speed and reversibility, though other studies suggest that switching may also be accompanied by a local structural change or the formation of a metastable crystalline filament.[10] One model that may explain the switching is the so called percolation model. In this model, localized trap states can switch to a delocalized conducting state as the electric field increases. At a critical value, a conductive percolation path of delocalized defects is formed across the layer.[11–13] When the voltage is lowered again, the delocalized state is retained below the initial threshold voltage until a critical hold voltage (V_{hold}) at which point defects become localized again and the current rapidly drops as the layer reverts to its HRS. In practice, a few defects can remain de-localized for some time after the initial switching, which results in a slightly higher off-state current. Over many cycles, this can cause the current in the LRS to approach that of the HRS. Recent studies have shown that this effect is reversible, however, by applying appropriate recovery voltage pulses.[13]

Ge-containing selenides show promise for use in two-terminal selectors based on OTS,[14,15] but knowledge about the thermal stability of GeSe alloys is still lacking. In order to exhibit volatile switching, the layers must remain amorphous during the selector fabrication process as well as during operation. Considering temperatures exceeding 400 °C are common in back-end-of-line (BEOL) processes, the crystallization temperature (T_c) needs to be at least this high. Additionally, partial crystallization is one of the ways the selector may fail irreversibly (i.e., remain stuck in the LRS state).[13] As such, higher thermal stability is generally preferred. Crystallization may be delayed by alloying with other elements. Alloying can in turn also be used to tune the threshold switching behavior. In this work, we explore the impact of the addition of alloying elements on thermal stability by measuring the crystallization temperature. The impact of alloying elements on the switching behavior is also studied. Several candidate materials were selected based on their varying degree of metallicity. Based on the bulk bandgap of Ge/Sb/Zr/B-selenides, one can predict that Sb and Zr alloying of GeSe will introduce states in the mobility gap since their bulk bandgap is lower, while the opposite holds true for B. This can change the electronic properties of the material such as making it more or less conductive.[16,17] Additionally, previous experiments[18,19] have already shown that C helps to lower the threshold voltage V_{th} at the cost of increasing the off-state leakage, while N achieves the opposite. It was, therefore, decided in this work to combine both elements to examine whether an optimal balance can be achieved. Before experimental work commenced, additional computational analysis was done in an attempt to predict if the chosen elements could yield interesting results, as well as to link some computed material properties to easily experimentally measurable device properties. Density-Functional Theory (DFT) simulations were conducted in CP2K, where a combination of Goedecker, Teter, and Hutter (GTH) pseudo-potentials and localized basis sets with a Perdew, Burke, and Ernzerhof (PBE) functional was used to generate ten different melt-and-quench atomic models. The hybrid exchange-correlation functional (HSE06) was used to investigate the electronic structure. The *ab initio* calculations were part of a separate study,



computed property	GeSe ref	CN	B	Sb	Zr
Ee (eV)	0.4	0.6	0.5	0.2	0.2
Eh (eV)	0	0.1	0.1	0.1	0.5
Eμ (eV)	1.1	1.1	1.1	0.9	0.7

FIG. 2. Impact of alloying on electronic properties of GeSe as determined by density-functional theory simulations. In the simulations, the alloying concentrations were chosen at 14 at. %. The blue and red arrows, respectively, indicate the electron and hole trap depth.[20]

additional details of which can be found in Ref. 20. Simulated properties include the electron and hole trap depths (E_e and E_h, respectively) as well as the mobility gap E_μ, which are related to IV leakage current and non-linearity. The results of these calculations can be found in Fig. 2.

II. EXPERIMENTAL

GeSe thin films were deposited by co-sputtering from a Ge_2Se_3 stoichiometric target in combination with a Ge target using radio frequency (RF) and direct current (DC) sputtering, respectively. Alloying was achieved by co-sputtering from elemental C, B, Sb, and Zr targets. Targets are sourced from reputable distributors and have a high level of purity, the lowest of which is 99.2% for Zr and the highest is 99.99 and 99.999% for, respectively, Ge_2Se_3 and Ge, which make up the base material. In order to incorporate N, reactive sputtering in a partial N_2 atmosphere was performed. High purity (6.0) sputter gases are used. Compositions were determined using a combination of Elastic Recoil Detection (ERD) for C, N, and B alloying and Rutherford Backscattering Spectrometry (RBS) for the heavier elements (Ge, Se, Zr, and Sb). The setup for ERD analysis consists of a 6SDH tandem accelerator from National Electrostatics Corporation and a ToF–E telescope detection system from the University of Jyvaskyla, Finland. For RBS analysis, the accelerator is a 6SDH Pelletron accelerator from the same supplier, and the scattering chamber was developed at the Jülich Research Center. Layer thickness is verified using X-ray Reflectivity (XRR) measurements. For X-Ray Diffraction (XRD) analysis, 50 nm GeSe-X films are deposited onto a $TiN/SiO_2/Si$ substrate and capped *in situ* with a 20 nm TiN layer to prevent material loss due to sublimation and prevent oxidation. To study the crystallization behavior, an *in situ* XRD approach is used. Samples are loaded individually into a vacuum chamber, which is then purged with He to create an inert atmosphere. Using a Cu K-α source and a linear Bruker VANTEC detector, a fixed 2θ-window of 20° is monitored, with two separate measurements done centered around 20° and 40°. The sample is then heated up to 600 °C at a heating rate of 0.2 °C/s. This way, the crystallization temperature can be accurately determined. For a selection of samples, the surface smoothness was also measured using a Bruker Dimension Edge Atomic Force Microscope (AFM). The sample layer structure is illustrated in Fig. 3(a).

For electrical characterization experiments, separate samples were prepared with 5 or 20 nm thin films deposited in metal–insulator–metal type test structures where the bottom electrode is scaled to 6 μm. A schematic of the test structures can be found in Fig. 3(b). A patterned substrate is used consisting of a 75 nm SiO_2 insulating layer on top of a 50 nm TiN bottom electrode layer. Then, 6 μm diameter vias are patterned and etched in the SiO_2 down to the bottom TiN. The switching and top electrode layers are sputtered through a 580 μm shadow mask aligned with the bottom electrode vias in the substrate. This results in cells with a top electrode of 580 μm for easy contacting but an effective switching area of only 6 μm in diameter. A single sample deposited this way will contain 81 cells of a given size. This structure allows for fast screening of multiple compositions and gives good results when focusing on relative effects but evidently lacks certain aspects of more complicated test structures (e.g., a built-in series resistor to limit operating current). During electrical measurements, a positive voltage is applied to the top electrode, while the backside of the sample is grounded. Using a Keithley 2601 Source-Measurement Unit, a slow voltage ramp is performed to obtain the switching voltage when applying a normal DC voltage. This procedure will often result in a leaky cell and, therefore, is not used for detailed threshold voltage analysis. Leakage current measurements are also done using DC conditions. To characterize the threshold switching behavior, first, the leakage current of a set of pristine devices is measured at 2 V. Using a Keysight 81150A pulse generator in combination with a Keysight MSOX3104T mixed oscilloscope, short triangular voltage pulses with a rise and fall time of 2.5 μs are then

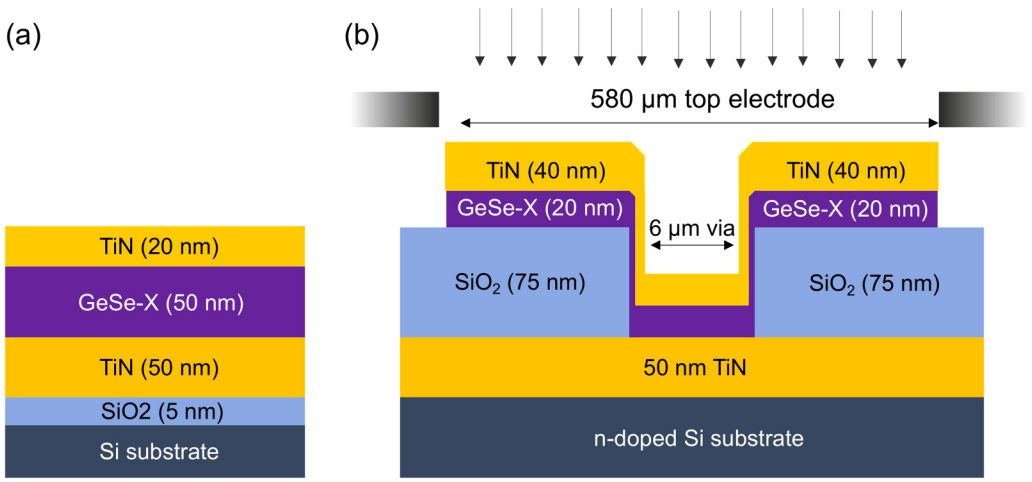


FIG. 3. (a) Schematic representation of the sample used for XRD and AFM analysis. (b) Schematic representation of the samples used for IV analysis. Note that these samples are prepared by sputtering of the switching layer and the top electrode onto a patterned test structure.

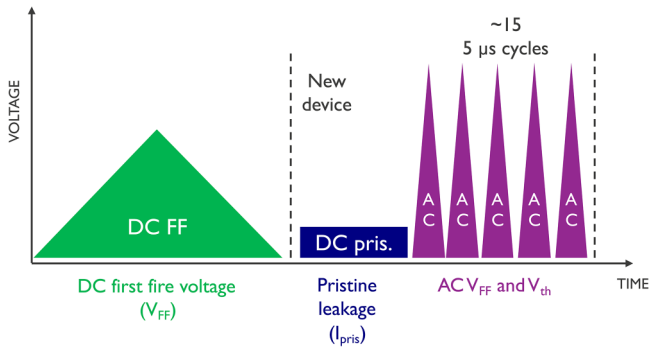


FIG. 4. Schematic representation of the sequence of measurements performed for IV characterization.

used to obtain values for the first fire and threshold voltage (AC V_{FF} and AC V_{th}). The short duration of the pulses ensures that the switching remains volatile. One channel of the oscilloscope measures the voltage drop across the sample, while the second channel is used to measure the voltage drop over the 50 Ω input impedance to determine the current flowing through the cell. Switching parameters obtained using this method are prefixed by the letters AC to distinguish them from the DC switching voltages. This measurement approach is graphically represented in Fig. 4. From the data collected during these measurements, the key parameters are then extracted using an automated python script. To increase accuracy, multiple cells are measured for each composition, and the results are reported in the form of box plots.

III. RESULTS AND DISCUSSION

A. Determining crystallization temperature of a GeSe thin film

Figure 5 shows the *in situ* XRD pattern of an unalloyed GeSe layer. The lack of peaks at room temperature suggests an as-deposited amorphous layer. As the temperature is raised, crystallization first occurs at 350 °C, as peaks relating to orthorhombic GeSe[21] appear in both windows of the XRD measurement. As the temperature is raised above 570 °C, both peaks disappear again, suggesting that the phase has melted. This temperature is comparable to the eutectic temperature of bulk 43 at. % Ge Ge_xSe_{1-x} of 578 °C reported by Ross and Bourgon.[22] In addition to melting, at elevated temperatures, the layer also experiences some sublimation. Both visual and energy dispersive x-ray (EDX) analysis show that the layer has largely evaporated after anneal to 600 °C. However, when annealed to a temperature beyond the crystallization point but below the point at which the layer melts, EDX analysis shows that the composition of the layer remains unchanged. This is shown in Fig. S1 of the supplementary material for a GeSe layer. This demonstrates that the TiN capping layer is effective in eliminating material sublimation up until at least the crystallization temperature. An *ex situ* locked couple θ–2θ XRD scan was also performed on a second sample that was annealed to 450 °C and subsequently quenched in order to study the peaks in more detail.

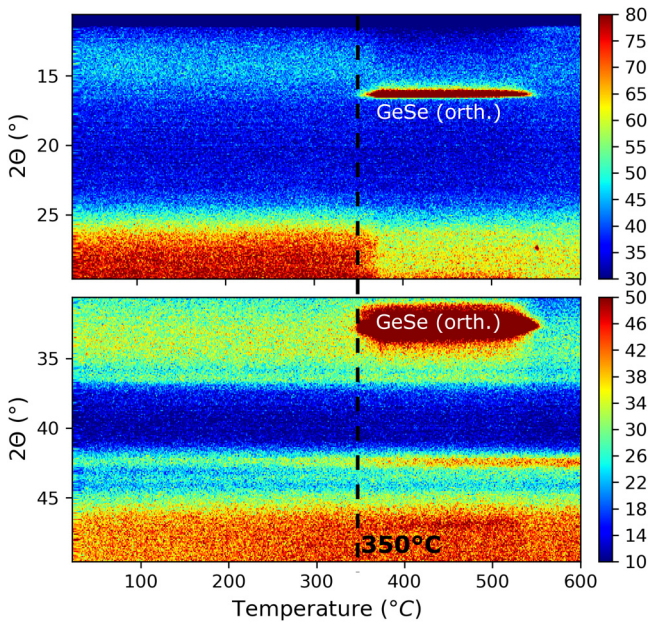


FIG. 5. *In situ* XRD patterns of GeSe, taken with a line detector centered at 20° and at 40°. Crystallization first occurs at 350 °C with the appearance of peaks related to orthorhombic GeSe.[21]

This result can be found in Fig. 6. The *ex situ* scans confirm the amorphous nature of the as-deposited layer. The only peaks to appear in the as-deposited layer also appear in the annealed layer and can be attributed to a face-centered TiN crystal structure found in the substrate or capping layer. In addition to the peaks at 16° and 33° that were also visible in the *in situ* scans, some additional peaks relating to orthorhombic GeSe can be seen here, including a shoulder peak to the 33° peak, explaining the broad nature of that peak in the *in situ* scan.

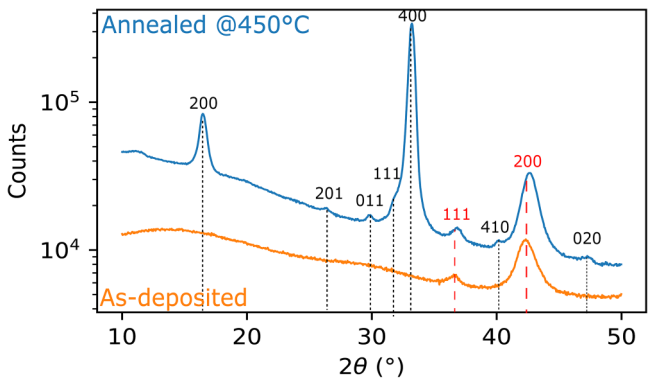


FIG. 6. Locked couple θ–2θ XRD scan of an as-deposited and annealed GeSe layer. Peaks relating to orthorhombic GeSe[21] are marked in black. The peaks marked in red are related to a face-centered TiN crystal structure.[23]

B. Impact of alloying on crystallization temperature and morphology

To increase the thermal stability, i.e., increase the crystallization temperature, alloying elements were added. For all elements, a systematic set of different concentration levels were targeted. However, the sputter parameters can pose a practical limitation. In the case of B, the RF sputter rates are fairly low compared to that of Ge_2Se_3 and Ge. With the power limited to 80W in order to not overheat the target, only a concentration of at most 2 at. % could be achieved. Conversely, the high DC sputter rate of Sb results in very efficient incorporation even at low power. The lower limit to the concentration in this case is the stability of the plasma at very low sputter power. For all materials and concentrations, XRD samples were prepared and measured as described in Sec. III A. An overview of all the *in situ* XRD measurements is provided in the supplementary material. Crystallization temperature has been defined in this paper as the temperature at which the first, non-substrate related, diffraction peak appears during a ramp anneal at 0.2 °C/s. In the case of Sb alloying, it is the alloying element that first crystallizes in the still amorphous GeSe matrix in which case this is taken as the crystallization temperature. The crystallization temperatures for the different alloying elements are summarized in Fig. 7.

In the case of B, even for a modest alloying concentration, a decrease in T_c is observed. Insufficient data are available to accurately judge the impact of B at higher concentrations though. For the case of Zr, the initial effect of alloying with a small amount is to decrease the crystallization temperature similar to the effects of B. When increasing the Zr content, the T_c quickly rises, surpassing that of unalloyed GeSe at a concentration of 5 at. %. In the case of Sb, a non-monotonic trend is observed. For all measured concentrations, the impact of Sb is to increase the crystallization temperature, though it is unclear what happens in the case of very low concentrations of alloying materials. The highest T_c is reached for an alloying element concentration of 26 at. %, after which the crystallization temperature drops again. A possible explanation for the non-monotonic trend in T_c could be the transition from a solid solution where Sb is homogeneously present throughout the as-deposited amorphous GeSe matrix to a more phase segregated state where Sb is present in small clusters either amorphous or of a size below that of the XRD detection limit. This hypothesis is supported by the fact that at lower Sb content, it is the GeSe that crystallizes first, whereas at higher concentrations, the dominant peaks are those of Sb and Sb based compounds. It is not possible to distinguish between the two states with only XRD. Other techniques such as scanning transmission electron microscopy would be able to distinguish a solid solution from a phase segregated state but are incompatible with a large material screening as performed in this paper.

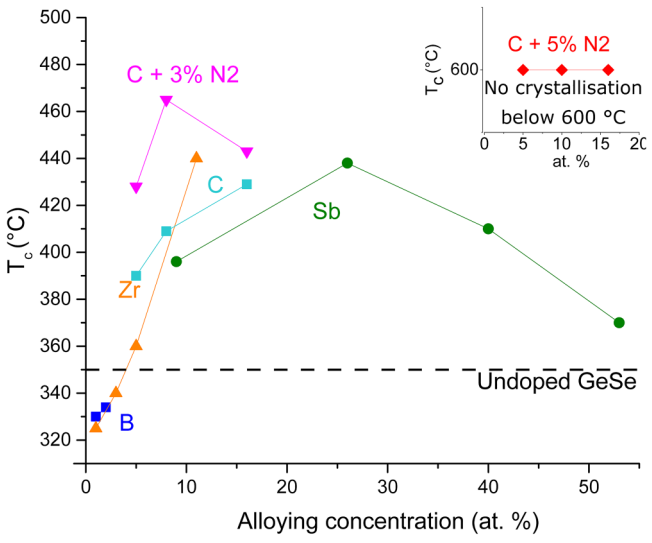


FIG. 7. Crystallization temperature T_c for alloyed GeSe as a function of alloying concentration in at. %. In the case of N incorporation, the percentage of N_2 in the sputter gas is listed. The inset represents the collection of CN alloyed samples where the N_2 concentration was 5%. For these samples, no crystallization is observed up until the maximum temperature of 600 °C. The dashed line represents the crystallization temperature of a 50 nm GeSe reference layer.

In the case of C alloying, a significant increase in the crystallization temperature across all alloying levels is observed. At an alloying level of 8 at. %, the T_c already exceeds 400 °C, with further increases of C content resulting in even higher T_c. When reactively sputtering in a 3% N_2 atmosphere, the thermal stability can be improved further, though the impact of N_2 becomes less significant at higher levels of C. The non-monotonic trend in T_c may possibly be attributed to slight variations in N_2 partial pressure between depositions. If the partial pressure of N_2 is increased up to 5%, a significant improvement of the thermal stability is observed. In this case, no crystallization is found in the measured temperature range for all of the C concentrations. As the C content has not changed significantly, it can be concluded that more efficient N incorporation due to the higher N_2 partial pressure is responsible for the increase in the crystallization temperature.

For a selected number of compositions, AFM measurements were performed. These measurements are shown in Fig. 8. In the case of CN alloying, the layers are very smooth, with the occasional particle observed. In the case of B alloying, the layers tend to be smooth, but particles/clusters are more common. In the case of Sb and Zr, no particles are observed, and the layers are generally smooth. This suggests decent intermixing of the alloying element and GeSe.

C. Electrical properties of alloyed GeSe layers

In addition to the impact on crystallization temperature, the alloyed layers were also compared electrically. For this purpose, alloying levels were chosen with relatively similar atomic concentrations. The selected concentrations are listed in Table I. In the case of separate C and N alloying, this has already been explored in earlier works[18,19,24] where it was found that C tends to increase the leakage current and switching voltages, while N tends to do the opposite to both. In this paper, we have, therefore, looked only at co-alloying with C and N. In Fig. 9, an example of a DC IV sweep and a pulsed IV sweep for the 20 nm CN alloyed sample is shown. In the case of the DC measurements, pristine leakage current prior

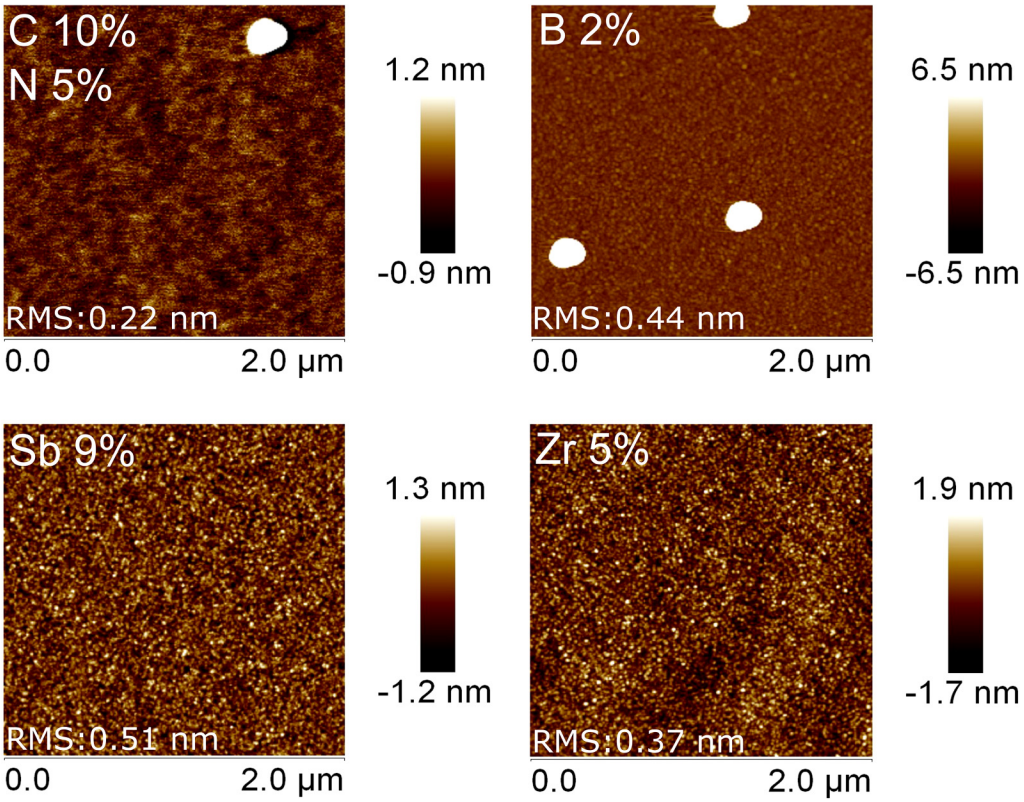


FIG. 8. Atomic force microscopy images of a selection of as-deposited alloyed GeSe samples. Alloying concentrations depicted are the same as those used in the IV characterization in the next paragraph. The RMS roughness calculated from a $2 \times 2 \mu m^2$ is listed in each image.

to switching can be determined accurately. In this study, we have chosen to measure the pristine leakage current at 2 V except in the case of the 5 nm CN alloyed layer, where the leakage current was measured at 1 V so as to not exceed the first fire voltage. The first fire voltage (V_{FF}) refers to the voltage at which a pristine cell switches from a high resistive to a low resistive cell. The DC V_{FF} can be accurately determined as the point at which the current suddenly reaches the compliance current. In the case of pulsed measurements, current value measurements do not have the same level of precision but can still be used to accurately determine the switching voltage. Both the first fire voltage and subsequent threshold switching voltages are determined by observing at which time during the pulse the current undergoes the sharpest increase. In Fig. 10, the results are summarized in the form of boxplots. To obtain these boxplots, a single sample is deposited for each alloying material. A single sample contains 81 cells of a given size (6 μm cells were used for this analysis). For each dataset, multiple cells are selected for measurement from different areas on the sample. This approach averages out any thickness variation that can occur along the sample. Other sources of spread in the data can be due to inconsistent etching of the vias on the substrate, which is done through a chemical process. Second, the quality of the top electrode of the cell can vary somewhat depending on the location of the sample as shadow effects from the mask are more pronounced during the static top electrode deposition. These are additional sources of variation that should be taken into account on top of the inherent variation of the physical process. A dashed line in each of the subplots represents the median value as obtained for an unalloyed 20 nm GeSe reference sample. It should be noted, however, that for this reference sample, the substrate design deviated slightly, though the via surface area and layer stacks were kept the same.

TABLE I. Selected alloying concentrations for IV analysis.

Label	CN5	CN20	B	Sb	Zr
Thickness	5 nm	20 nm	20 nm	20 nm	20 nm
Atomic percentage	10 at. % C, 5% N_2	10 at. % C, 5% N_2	2 at. % B	9 at. % Sb	5 at. % Zr

1. Threshold voltage analysis

Figure 10(a) shows the DC V_{FF} obtained from a single DC IV sweep on least eight function cells. A clear trend can be observed

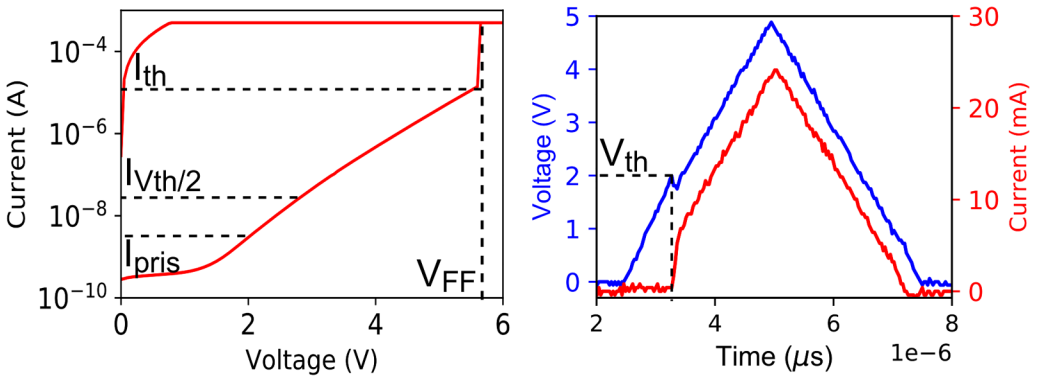


FIG. 9. (left) Example of a DC IV sweep on a CN alloyed sample. (right) Example of a pulsed IV sweep on a CN alloyed sample. The blue curve represents the applied voltage and the red curve the measured current. Several parameters have been indicated.

when going from the non-metallic elements to the more metallic ones with lower first fire voltages observed for the more metallic elements such as Sb and Zr. Interesting to note as well is the difference between the first fire voltage of the 20 nm CN alloyed sample (CN20) and the 5 nm CN alloyed sample (CN5). A factor of nearly four difference is observed in the first fire voltage, which coincides with the factor of four difference in layer thickness. This can be understood as the critical electric field required for first fire switching being the same in both layers.

The first fire voltage as obtained using pulsed measurement (b) follows a very similar trend. The AC V_{FF} (obtained from at least 15 functional cells) is in all cases systematically higher than the DC case, though the difference decreases for the more metallic elements. The main difference between the DC and AC sweeps is the vastly slower sweep rate (0.5 V/s vs 2×10^6 V/s), which suggests slight sweep rate dependence. Such sweep rate dependence has already been observed in the case of faster sweep rates between 5×10^3 V/s and 5×10^6 V/s and is related to the voltage dependence of the switching probability.[25] The V_{FF} is a measure of how difficult the material is to switch; as such, it can be inferred that metallic alloying elements facilitate switching, but non-metallic elements may inhibit switching.

The threshold voltage V_{th} (c) is recorded from ± 20 subsequent switching cycles. Only the data of those cells that exhibited volatile switching for all 20 cycles were included. The threshold voltages of at least six function cells for each alloying element are included in the boxplot. All layers show a threshold voltage significantly lower than that of the first fire case, and the outliers at higher threshold voltages often represent the first several cycles after the initial first fire. This indicates that the material goes through a certain forming step prior to settling in a more stable regime. This forming step is in line with the hypothesis that after first fire, some defect trap states will remain delocalized and facilitate switching during subsequent cycles. Alternatively, it is possible that during the first few cycles, some material segregation or partial crystallization is taking place, which stabilizes after a few cycles. Recently, other studies have shown that it may be possible to recover the pristine state by applying appropriate recovery pulses using a reverse bias.[13] Crucially, recovery is only possible so long as no material segregation or crystallization has yet occurred. In the case of the threshold voltage as compared to the first fire voltage, differences in-between alloying elements are far less noticeable. Compared to the 20 nm CN alloyed sample, B, Sb, or Zr alloying all result in a slightly lower threshold voltage. A surprising result is obtained from the 5 nm CN layer, as despite having a factor of nearly 4 difference in the first fire voltage and a factor of 4 difference in the thickness, after first fire, the threshold voltage differs only by 25%. A possible explanation for this is that the first fire makes a percolative path of defects that facilitate OTS switching at lower voltages.[26] A thicker layer may have a longer path length but still exhibit a comparable switching voltage. No comparison to the unalloyed reference was made here as it is likely that the difference in the substrate is most prominent for repeated cycling (for instance, differences in contact resistances).

2. Leakage current analysis

The pristine leakage I_{pris} (d) is determined using a DC measurement at 2 V (or 1 V in the case of the 5 nm CN alloyed sample as 2 V is above the DC FF voltage of this sample). The data in this plot are obtained from a number of cells reserved for pristine leakage measurements as well as the same IV sweeps that are used to obtain the data in subfigure (a). In total, the set contains at least 15 functional cells. A clear inverse relation to that of the first fire voltage can be observed with more metallic elements resulting in a significantly higher pristine leakage current even for modest concentrations like in the case of Zr. Compared to the reference, the non-metallic alloying elements tend to decrease the leakage current. CN alloying, in particular, results in low leakage current even for a 5 nm layer. A notable correlation can be observed with the calculated electron trap depths (E_e) in Fig. 2. The alloys with a lower trend E_e show a higher leakage current at the same voltage/electric field. If the conduction is dominated by Poole–Frenkel conduction, involving hopping of electrons between trapped states and the conduction band, a lower trap depth would result in a higher

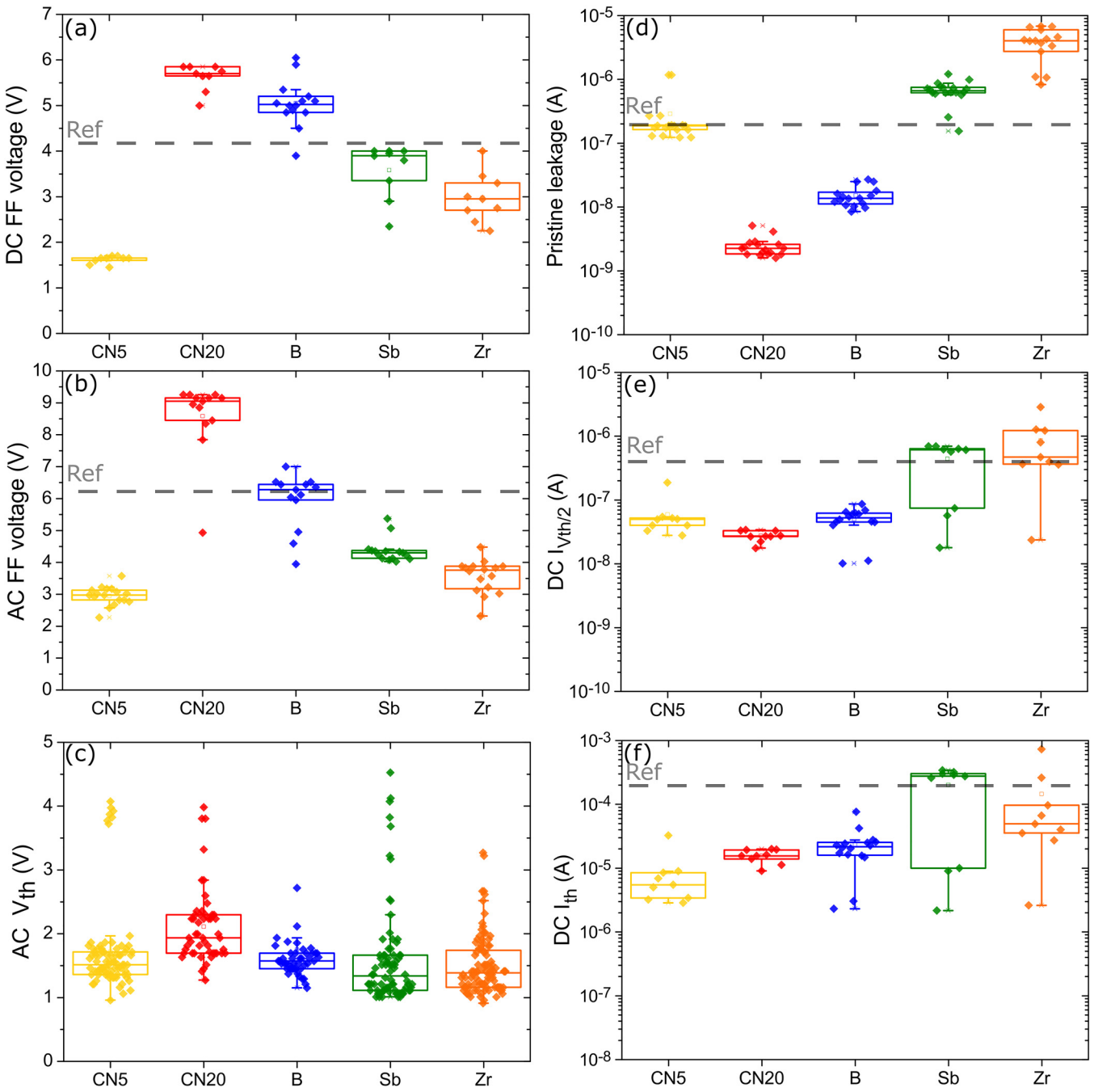


FIG. 10. Summarized electrical characteristics for alloyed GeSe layers. A dashed line in each subplot represents the median value obtained for an unalloyed GeSe reference. (a) First fire voltage obtained from a slow DC voltage sweep. (b) First fire voltage determined using a short triangular pulse. (c) Threshold voltage obtained from multiple subsequent cycles of triangular pulses. (d) Pristine leakage at 1 V/2 V. (e) Current at half of the DC first fire voltage. (f) Current at the DC first fire voltage.

current at the same electric field,[9] which would appear to be the trend observed here.

A second common approach for measuring leakage current is to measure the leakage current at half the threshold voltage ($I_{Vth/2}$), with the ratio between I_{on} and $I_{1/2}$ being the selectivity (non-linearity) factor of the device. As the purpose of a selector cell is to limit the leakage current through half-selected cells, $I_{Vth/2}$ is crucial in judging the viability of the device. This is done in Fig. 10(e).

These boxplots contain the current measured at half the DC V_{FF} reported in Fig. 10(a) for every individual first fire cycle. While the pristine leakage at fixed and first fire voltages can differ greatly between alloying elements, the differences in leakage current when measured this way are more subtle. This further illustrates that V_{FF} and I_{pris} are intimately related and decreases in one often come at the cost of increases in the other. This is particularly true for the CN films and shows that varying the thicknesses can achieve a desired pristine leakage or switching voltage, but varying the thickness does not change the non-linearity of the material. In the case of the Zr and Sb, leakage at a half-threshold voltage is higher as opposed to the other alloying elements. Once again, a correlation can be seen between this trend and the mobility gaps obtained from the DFT calculations. The mobility gap decreases when going from B to Sb to Zr, which is reflected by the increase in the leakage current observed for these materials in addition to their decrease in the first fire voltage. It should be stressed though that while these observations may point toward a certain conduction mechanism, they are not enough in itself to make a conclusion. The correlations pointed out here serve mostly to illustrate that DFT analysis of material characteristics may help in predicting trends in device characteristics.

Finally, Fig. 10(f) contains the DC threshold current. This is the current measured just prior to the first fire event. It is notable that despite the much more significant variation in V_{FF} and I_{pris}, differences here are more modest, though spread in the data, especially in the case of metallic elements, makes accurate determination difficult. As the ON current through a selector is often determined by the adjacent resistive elements, a lower current prior to switching increases the effective resistive window of the selector cell and as such is preferable.

The last two parameters were also obtained from the DC IV sweeps used in subfigure (a) and thus contain the same number of datapoints. From these parameters, we may conclude that in the case of the CN alloyed samples, even though at a fixed voltage, a thinner layer has a higher leakage current, considering the leakage at a half-threshold voltage remains the same and the resistive window is higher, a thinner layer may be more effective at eliminating sneak path currents in a crossbar device. When compared to separate alloying with just N or C,[19] it seems that combining C and N achieves comparable reductions in leakage current, while the presence of C limits the increases in first fire and threshold voltages. A separate study on $GeSe_2$ has already shown that homopolar Ge bonds as well as Ge clustering are mainly responsible for the leakage current.[27] Nitrogen was shown to drastically reduce Ge homopolar bond presence and leakage current, but co-alloying with a more conductive element (Sb in the case of the study) was also required to facilitate switching and to lower the first fire voltage. As such, we can summarize that N incorporation is an effective tool to reduce the leakage current in $GeSe_x$-chalcogenides by eliminating undesired bonds after which co-alloying with a more conductive element (C, Sb, Zr) allows for tuning of the first fire and threshold voltage to the desired level.

IV. CONCLUSIONS

In this paper, we have demonstrated that the crystallization temperature of GeSe can be effectively increased with the addition of alloying elements through (reactive) co-sputtering across a wide range of concentrations. However, note that the sputter efficiency of the alloying elements may impose practical limits as to what is achievable without the use of alloyed GeSe-X targets. For the metallic alloying elements Sb and Zr, concentrations above 10 at. % are required to increase the crystallization temperature above 400 °C. At very low concentration (<3 at. %), however, the presence of a metallic or metalloid element can have a lowering effect on the crystallization temperature. In the case of non-metallic alloying elements such as C, even at small alloying concentrations, increases in crystallization temperature are observed. In the case of just C alloying, a crystallization temperature above 400 °C can be achieved with alloying concentrations of 8 at. % C. When reactively sputtering in a 3% N_2 atmosphere, this level of thermal stability can already be reached with a concentration as low as 5 at. %. When increasing the N_2 partial pressure to 5%, the amorphous state is retained beyond 600 °C.

Alloyed layers were also compared electrically. It was found that even at limited concentrations, significant impact on electrical characteristics can be observed. A clear trend is noticeable toward lower first voltage and increased leakage current when going from non-metallic to metallic elements, which holds even if the alloying concentration of the more metallic element is lower than that of the less metallic one. As evident from the half-threshold leakage current measurement, this trade-off between the first fire voltage and the leakage current at a fixed bias appears to be universal across all alloying elements. The threshold voltage is less sensitive to alloying with only a reduction observed in the case of metallic alloying. In the case of CN alloying, low leakage currents are observed. The V_{FF} and V_{th} are higher than in the case of other elements, but it has been shown that this can be tuned by changing the thickness, while still retaining a low leakage at a half-threshold voltage. Combined with their high thermal stability across compositions, CN alloyed GeSe was shown to be the most viable candidate for selector applications. Improved performance overall is obtained compared to layers with only C, which suffer from high leakage currents or only N, which suffer from high threshold voltages.[18,19] Finally, we aimed to demonstrate that DFT analysis may be a helpful tool in predicting trends in device characteristics based on calculated material characteristics.

SUPPLEMENTARY MATERIAL

See the supplementary material for an overview of all *in situ* XRD patterns used for the thermal stability analysis in this paper as well as EDX measurements prior to and after annealing of a GeSe reference layer.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available within the article and its supplementary material.

REFERENCES

[1]S. Barraud, M. Ezzadeen, D. Bosch, T. Dubreuil, N. Castellani, V. Meli, J. M. Hartmann, M. Mouhdach, B. Previtali, B. Giraud, J. P. Noël, G. Molas, J. M. Portal, E. Nowak, and F. Andrieu, "3D RRAMs with gate-all-around stacked nanosheet transistors for in-memory-computing," in *2020 IEEE International Electron Devices Meeting (IEDM)* (IEEE, 2020), pp. 29.5.1–29.5.4.

[2]B. R. Fernando, Y. Qi, C. Yakopcic, and T. M. Taha, "3D memristor crossbar architecture for a multicore neuromorphic system," in *2020 International Joint Conference on Neural Networks (IJCNN)* (IEEE, 2020), pp. 1–8.

[3]G. W. Burr, M. J. Brightsky, A. Sebastian, H. Cheng, J. Wu, S. Kim, N. E. Sosa, N. Papandreou, H. Lung, H. Pozidis, E. Eleftheriou, and C. H. Lam, "Recent progress in phase-change memory technology," IEEE J. Emerg. Sel. Top. Circuits Syst. **6**, 146–162 (2016).

[4]P. Narayanan, G. W. Burr, K. Virwani, and B. Kurdi, "Circuit-level benchmarking of access devices for resistive nonvolatile memory arrays," IEEE J. Emerg. Sel. Top. Circuits Syst. **6**, 330–338 (2016).

[5]C. Kügeler, M. Meier, R. Rosezin, S. Gilles, and R. Waser, "High density 3D memory architecture based on the resistive switching effect," Solid State Electron. **53**, 1287–1292 (2009).

[6]B. Govoreanu, L. Zhang, and M. Jurczak, "Selectors for high density crosspoint memory arrays: Design considerations, device implementations and some challenges ahead," in *2015 International Conference on IC Design & Technology (ICICDT)* (IEEE, 2015), pp. 1–4.

[7]G. W. Burr, R. S. Shenoy, K. Virwani, P. Narayanan, A. Padilla, B. Kurdi, and H. Hwang, "Access devices for 3D crosspoint memory," J. Vac. Sci. Technol. B **32**, 040802 (2014).

[8]S. R. Ovshinsky, "Reversible electrical switching phenomena in disordered structures," Phys. Rev. Lett. **21**, 1450 (1968).

[9]D. Ielmini, "Threshold switching mechanism by high-field energy gain in the hopping transport of chalcogenide glasses," Phys. Rev. B **78**, 035308 (2008).

[10]P. Noé, A. Verdy, F. d'Acapito, J.-B. Dory, M. Bernard, G. Navarro, J.-B. Jager, J. Gaudin, and J.-Y. Raty, "Toward ultimate nonvolatile resistive memories: The mechanism behind ovonic threshold switching revealed," Sci. Adv. **6**, eaay2830 (2020).

[11]D. Garbin, W. Devulder, R. Degraeve, G. Donadio, S. Clima, K. Opsomer, A. Fantini, D. Cellier, W. Kim, M. Pakala *et al.*, "Composition optimization and device understanding of Si-Ge-As-Te ovonic threshold switch selector with excellent endurance," in *2019 IEEE International Electron Devices Meeting (IEDM)* (IEEE, 2019), pp. 35.1.1–35.1.4.

[12]S. Kabuyanagi, D. Garbin, A. Fantini, S. Clima, R. Degraeve, G. Donadio, W. Devulder, R. Delhougne, D. Cellier, A. Cockburn *et al.*, "Understanding of tunable selector performance in Si-Ge-As-Se OTS devices by extended percolation cluster model considering operation scheme and material design," in *2020 IEEE Symposium on VLSI Technology* (IEEE, 2020), pp. 1–2.

[13]F. Hatem, Z. Chai, W. Zhang, A. Fantini, R. Degraeve, S. Clima, D. Garbin, J. Robertson, Y. Guo, J. Zhang *et al.*, "Endurance improvement of more than five orders in Ge_xSe_{1-x} OTS selectors by using a novel refreshing program scheme," in *2019 IEEE International Electron Devices Meeting (IEDM)* (IEEE, 2019), pp. 35.2.1–35.2.4.

[14]H.-W. Ahn, D. Seok Jeong, B.-K. Cheong, H. Lee, H. Lee, S.-D. Kim, S.-Y. Shin, D. Kim, and S. Lee, "Effect of density of localized states on the ovonic threshold switching characteristics of the amorphous GeSe films," Appl. Phys. Lett. **103**, 042908 (2013).

[15]B. Govoreanu, G. L. Donadio, K. Opsomer, W. Devulder, V. Afanas' ev, T. Witters, S. Clima, N. S. Avasarala, A. Redolfi, S. Kundu *et al.*, "Thermally stable integrated Se-based OTS selectors with ¿20 mA/cm^2 current drive, >3.10 3 half-bias nonlinearity, tunable threshold voltage and excellent endurance," in *2017 Symposium on VLSI Technology* (IEEE, 2017), pp. T92–T93.

[16]A. Jain, S. P. Ong, G. Hautier, W. Chen, W. D. Richards, S. Dacek, S. Cholia, D. Gunter, D. Skinner, G. Ceder, and K. A. Persson, "The materials project: A materials genome approach to accelerating materials innovation," APL Mater. **1**, 011002 (2013).

[17]S.-Y. Shin, J. Choi, J. Seo, H.-W. Ahn, Y. G. Choi, B.-K. Cheong, and S. Lee, "The effect of doping Sb on the electronic structure and the device characteristics of ovonic threshold switches based on Ge-Se," Sci. Rep. **4**, 7099 (2014).

[18]N. S. Avasarala, G. Donadio, T. Witters, K. Opsomer, B. Govoreanu, A. Fantini, S. Clima, H. Oh, S. Kundu, W. Devulder *et al.*, "Half-threshold bias I off reduction down to nA range of thermally and electrically stable high-performance integrated OTS selector, obtained by Se enrichment and N-doping of thin GeSe layers," in *2018 IEEE Symposium on VLSI Technology* (IEEE, 2018), pp. 209–210.

[19]N. S. Avasarala, B. Govoreanu, K. Opsomer, W. Devulder, S. Clima, C. Detavernier, M. van der Veen, J. Van Houdt, M. Henys, L. Goux *et al.*, "Doped GeSe materials for selector applications," in *2017 47th European Solid-State Device Research Conference (ESSDERC)* (IEEE, 2017), pp. 168–171.

[20]S. Clima, B. Govoreanu, K. Opsomer, A. Velea, N. S. Avasarala, W. Devulder, I. Shlyakhov, G. L. Donadio, T. Witters, S. Kundu *et al.*, "Atomistic investigation of the electronic structure, thermal properties and conduction defects in Ge-rich Ge_xSe_{1-x} materials for selector applications," in *2017 IEEE International Electron Devices Meeting (IEDM)* (IEEE, 2017), pp. 4.1.1–4.1.4.

[21]D. Grier, G. McCarthy, D. Seidler, and P. Boudjouk, "JCPDS pattern 00-048-1226," ICDD Grant-in-Aid, 1987.

[22]L. Ross and M. Bourgon, "The germanium–selenium phase diagram," Can. J. Chem. **47**, 2555–2559 (1969).

[23]W. Wong-Ng, H. McMurdie, B. Paretzkin, C. Hubbard, and A. Dragoo, "JCPDS pattern 00-038-1420," ICDD Grant-in-Aid, 1987.

[24]S. Clima, D. Garbin, K. Opsomer, N. S. Avasarala, W. Devulder, I. Shlyakhov, J. Keukelier, G. L. Donadio, T. Witters, S. Kundu *et al.*, "Ovonic threshold-switching Ge_xSe_y chalcogenide materials: Stoichiometry, trap nature, and material relaxation from first principles," Phys. Status Solidi RRL **14**, 1900672 (2020).

[25]Z. Chai, W. Zhang, R. Degraeve, S. Clima, F. Hatem, J. F. Zhang, P. Freitas, J. Marsland, A. Fantini, D. Garbin *et al.*, "Dependence of switching probability on operation conditions in Ge_xSe_{1-x} ovonic threshold switching selectors," IEEE Electron Device Lett. **40**, 1269–1272 (2019).

[26]Z. Chai, W. Zhang, R. Degraeve, J. F. Zhang, J. Marsland, A. Fantini, D. Garbin, S. Clima, L. Goux, and G. S. Kar, "RTN in Ge_xSe_{1-x} OTS selector devices," Microelectron. Eng. **215**, 110990 (2019).

[27]J. Keukelier, K. Opsomer, T. Nuytten, S. Sergeant, W. Devulder, S. Clima, L. Goux, G. S. Kar, and C. Detavernier, "Impact of changes in bond structure on ovonic threshold switching behaviour in $GeSe_2$," J. Mater. Chem. C **9**, 117–126 (2021).