Monolithic Integration of Thin Film Photodiode with CMOS Technology for Infrared Imaging Applications

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Abstract

Monolithic integration of thin film photodiode with CMOS wafer is promising for various emerging infrared image sensing applications such as AR/VR and automotive electronics. Compared to the III-V infrared image sensor chip process using 3D assembly technology, the advantage of thin film photodiode sensors is versatility and cost. However, there are several process challenges to overcome before volume production can be implemented in a CMOS fab. In this paper, we discuss the process flow of thin film photodiode integration and update the status of the process development at imec.

Keywords—monolithic integration; infrared; thin film photodiode; TFPD; image sensor; quantum dot

Introduction

Si-based CMOS image sensor technology has been well established since the first Si CMOS image sensor chip was developed in 1993 and has achieved high resolution, high efficiency, and low cost [1, 2]. However, the application of Si CMOS image sensor is limited to visible and near-infrared wavelength range due to the inherent bandgap property of Si. For image sensing in the infrared wavelength range, a photo-active layer material with smaller bandgap, i.e. non-Si material, integrated with CMOS readout is needed. III-V materials have been the main material for such infrared application during the past decades. Due to the difficulty of epi growth of high quality III-V materials on Si substrate, III-V based infrared image sensor chips or tiles are integrated with CMOS wafer using 3D assembly technology [3]. The pixel pitch and the manufacturing cost of III-V based infrared image sensor is lagging that of Si CMOS image sensors.

Compared to III-V chip/tile integration with CMOS wafer using 3D assembly technology, thin film photodiode (TFPD) is showing competitiveness in process versatility and manufacturing cost [4]. By spin-coating or evaporation, thin film stacks with organic photodiode or quantum-dot photodiode can be deposited and processed on top of the standard CMOS readout integrated circuit (RoIC) wafers in a CMOS fab. Various thin-film-based imager devices have been demonstrated and different thin-film materials have been explored to cover the imaging application in the wavelength range of visible to IR [5, 6, 7]. However, the integration of such thin-film materials using a standard CMOS process flow with volume manufacturing compatibility is still a challenge.

In this work, we discuss the monolithic integration flow of a quantum-dot photodiode thin film on standard CMOS RoIC wafers and report the latest development status [8].

Thin Film Photodiode Process on CMOS Readout Wafer

The schematic cross-section of a fully integrated TFPD image sensor chip is as shown in Fig.1. After the standard CMOS process, the following four major modules are needed to develop the fully integrated thin film image sensor on top of CMOS wafer: RoIC-TFPD interface module, TFPD stack module, TFPD patterning module, and passivation and connection module.

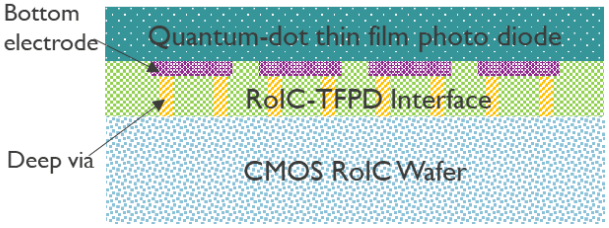

Fig.1. Schematics of monolithically integrated quantum-dot thin film photo diode with standard CMOS readout wafer.

A. RoIC-TFPD interface module

This interface module consists of the bottom electrode of the thin film photodiode and the deep vias which connect the bottom electrode to the circuitry in CMOS wafer. The bottom electrode is a critical component for the imaging devices, as the material and the process need to be optimized to get balanced electrical and optical performances.

B. TFPD stack module

In the TFPD stack module, the functional layers in the thin-film photodiode need to be deposited on top of the CMOS wafer after the interface module process. The sequence of the stack deposition depends on the polarity of the devices, either e2RoIC (Fig. 2) or h2RoIC (reading out electrons or holes, respectively).

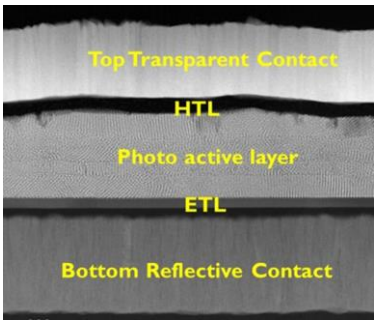

Fig.2. TEM cross-section of the fully processed TFPD stack (e2RoIC) on full wafer where ETL is electron transport layer and HTL is hole transport layer

Among these layers, the defectivity of the photo-active layer is critical for the imager device performance and needs strict process control. As shown in Fig.3, the defectivity of a quantum-dot layer can be significantly improved after the deposition process optimization.

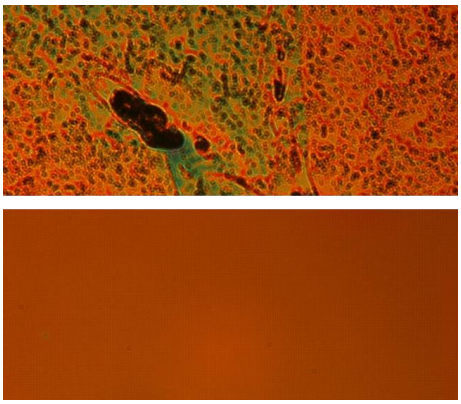

Fig.3. Demonstration of the quantum-dot layer defectivity before (top) and after (bottom) the deposition process optimization

D. TFPD stack patterning module

The thin film patterning on wafer level is another challenge for a CMOS fab. Firstly, the functional thin film imposes a lower thermal budget limitation on all the following process steps in the integration flow. A strict temperature control is needed to avoid yield loss induced by thin-film outgassing. Secondly, the patterning process needs to follow the contamination control in a CMOS fab during the patterning process of the complex thin film stack. Some wafer level patterning result is shown in Fig. 4.

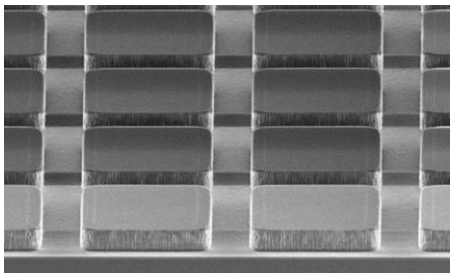

Fig.4. SEM inspection of TFPD pixel array patterning process on full wafer

Fig. 5 illustrates a proof-of-concept image sensor realized on die level using PbS quantum-dot stack monolithically integrated with a 5-um pixel pitch readout chip (768x512 px)

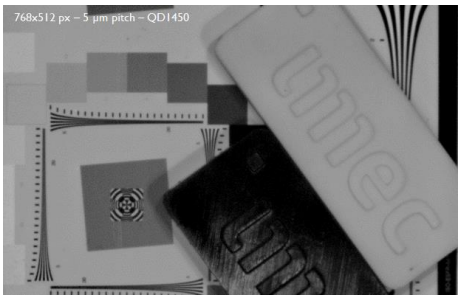

Fig.5. Test image acquired by quantum-dot based sensor processed on die-level.

Conclusion

There are various potential applications for thin-film based infrared image sensor technology. To implement such technology in volume manufacturing, monolithic integration of thin-film photodiode on standard CMOS wafers is essential. In this paper, we have discussed several integration process challenges and shown the latest integration process development results at wafer level.

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