AlON gate dielectric and gate trench cleaning for improved reliability of vertical GaN MOSFET

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Abstract

A wide range of applications in power electronics have been increasingly adopting in recent years the use of wide bandgap semiconductor materials due to their unprecedent compromise between maximum reverse blocking voltage (Vr) and ON-state resistance (Ron) [1]. A promising technology for extending the maximum Vr of GaN-based devices to 1200V and beyond is the Vertical GaN MOSFET. The semi-vertical architecture on 200mm GaN-on-Si wafer is used as a test vehicle to develop optimal process modules, such as the gate stack, for later implementation in a vertical device architecture [2]. An important region of this device is the gate insulator since the quality of the dielectric material and of the interface with the semiconductor play key roles in defining its threshold voltage (Vt), Vt hysteresis and reliability. Recent works have proposed the use of the high-κ dielectric AlON as the gate insulator in lateral AlGaN/GaN MOS-Heterojunction FET technologies due to the resulting reduced Vt hysteresis [3][4] and the possibility of using higher temperatures in the process steps following the dielectric deposition due to the stable amorphous structure of AlON [5]. This work discusses for the first time the use of an AlON dielectric in a trench-gate GaN device as an interface dielectric between the GaN channel region and a SiO_2 insulator in a bilayer gate stack. This analysis is performed by means of Vt hysteresis, Positive Bias Temperature Instability (PBTI) and Time Dependent Dielectric Breakdown (TDDB) measurements on wafers with three different AlON depositions: AlO cycle first (lower and higher nitrogen content) and AlN cycle first (lower nitrogen content), which are then compared to the commonly used Al_2O_3. The effect of two different cleanings of the gate trench prior to the dielectric deposition and of the SiO_2 thickness on device reliability are also addressed by TDDB analysis.

Fig. 1 depicts the cross section of the semi vertical GaN-on-Si MOSFET. The stress compensation layers and the GaN n+ drain/n- drift/p body/n+ source regions are epitaxially grown on 200mm Si (111) substrates by MOCVD. The gate trench is opened by dry etch and its surface is smoothed by Atomic Layer Etching (ALE) cycles before being treated with an optimized chemical cleaning. A 2.5nm thick interface dielectric, either Al_2O_3 or AlON, is grown by Atomic Layer Deposition (ALD) before the PECVD deposition of 50nm of SiO_2. Fig.2 shows the transfer characteristics and extracted Vt of devices with Al_2O_3 or AlON interface dielectric The Al_2O_3 dielectric results in the highest median Vt (7.4V), while both AlON wafers with AlO deposited first present the lowest median Vt (3.9V). This is most likely related to dangling bonds, which create positive charges that lower Vt in the devices with AlON-AlO first dielectrics, in accordance with what has been previously reported for AlGaN/GaN-HFETs [3]. The reason for this effect to be less pronounced when depositing AlN first is still not fully understood, but this is likely due to the different quality of the interface and of the dielectric. Fig. 3 depicts the Vt hysteresis after a Vgs double sweep between 0V and Vt+4V. The wafers with Al_2O_3 and AlON-AlN first present similar Vt hysteresis (with a median of 0.64V and 0.56V, respectively), even though the values are more dispersed for the Al_2O_3 wafer. Both wafers with AlON-AlO first present the lowest hysteresis with a median of 0.25V as a result of the better interface with the semiconductor, which has also been reported for AlGaN/GaN devices [3][4]. The results for the PBTI measurements are shown in fig.4, in which the gate stack was submitted to a continuous stress voltage by applying an overdrive voltage of around 13V to the gate. Following the trend observed for the Vt hysteresis, both wafers with AlON dielectric-AlO first present the least Vt shift over time (0.95V after $1{\cdot}10^4$ s) possibly due to the better interface quality. The Al_2O_3 dielectric results in the highest Vt shift (1.8V after $1{\cdot}10^4$ s), which is higher than the obtained value for the AlON-AlN first dielectric (1.2V for $1{\cdot}10^4$ s). The TDDB analysis was performed by stressing devices at high temperature and plotting the time to failure on a Weibull plot, so that the gate voltage for an 1% failure rate in 10 years can be extrapolated. Fig. 5 shows that when comparing the devices with Al_2O_3 and AlO-AlN first interface dielectrics, the same Vgs of 33V for a 1% failure rate over 10 years is obtained, which suggests that the dielectric wear-out happens in the thicker SiO_2 dielectric and is thus not affected by the high-κ layer. To demonstrate the impact of the optimized chemical cleaning employed in these devices on device reliability, TDDB analysis is conducted on devices with a 2.5nm Al_2O_3 + 65nm SiO_2 dielectric stack and different gate trench cleanings before the dielectric deposition. Fig. 6 shows that cleaning 2 can improve the maximum electric field (approximated as Vgs over SiO_2 thickness) sustained by the gate stack for a 1% of failure rate over 10 years in about 10% (and the maximum Vgs from 39V to 42V) when compared to clean 1. We hypothesize that cleaning 2 has a positive impact on the presence of weak spots in the dielectric stack and on their statistical distribution over devices by removing more efficiently organic residues. Increasing the SiO_2 thickness does not affect the maximum electric field for the same failure rate and operation time, however a thicker SiO_2 increases the maximum Vgs, since the electric field over the gate is reduced.

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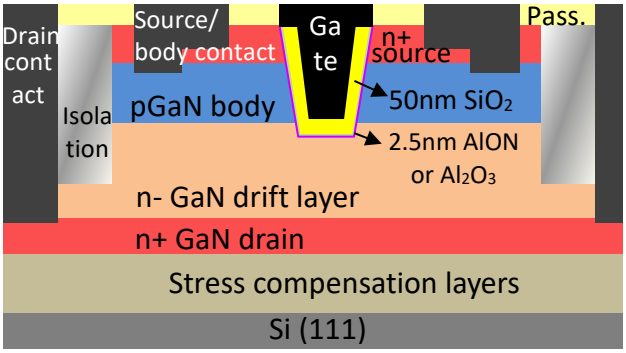

Figure 1 - Schematic cross section of the GaN-on-Si semi vertical MOSFET

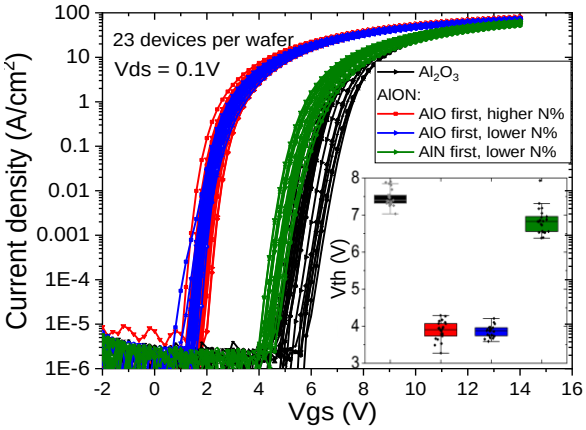

Figure 2 - Current density as a functions of the gate voltage for different AlON depositions and Al_2O_3. Inset: threshold voltage.

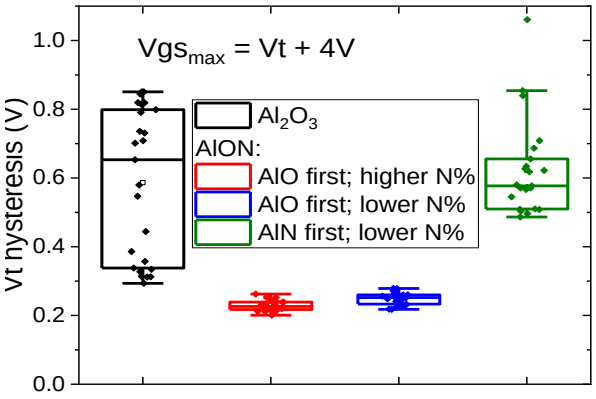

Figure 3 - Threshold voltage hysteresis after forward and back sweeping Vgs between 0V and Vt + 4V for wfaers with AlON and Al_2O_3 gate dielectric

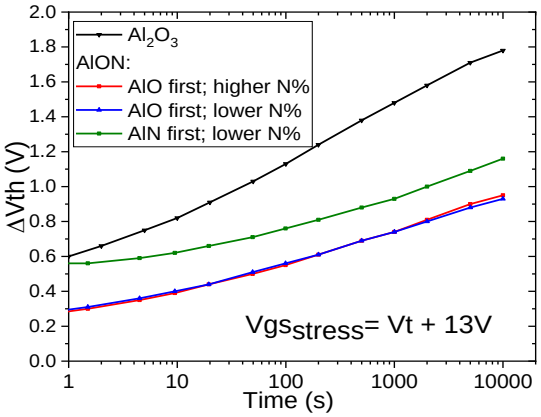

Figure 4 - Threshold voltage shift over time with gate overdrive voltage around 13V for wfaers with AlON and Al_2O_3 gate dielectric.

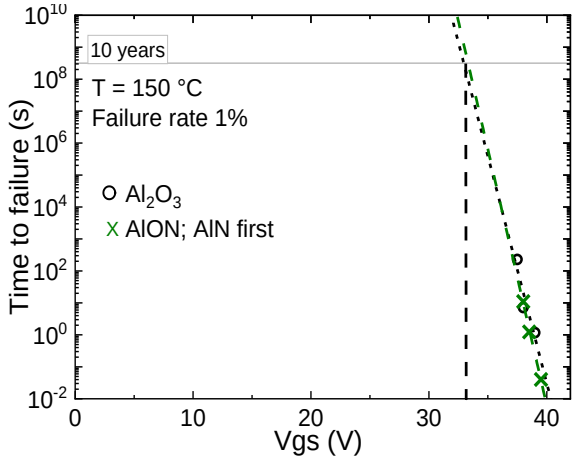

Figure 5 - Time to failure (failure rate 1%) over gate voltage and 10 years lifetime extrapolation for AlON and Al_2O_3 wafers

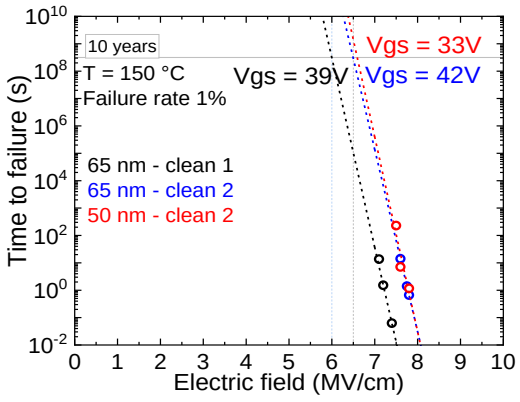

Figure 6 - 1% rate time to failure over electric field and 10 years lifetime extrapolation for clean 1 and 2 and for 50nm and 65nm of SiO_2. Vgs for 10 years of operation, 1% failure rate is also indicated.