A 3.3GS/s 6b Fully Dynamic Pipelined ADC with Linearized Dynamic Amplifier

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***Abstract*—This paper presents a single-channel 3.3 GS/s 6b pipelined ADC which features a post-amplification residue generation (PARG) scheme, linearized dynamic amplifier and on-chip calibration to achieve a high-speed, low-power, and compact prototype. The PARG scheme allows the quantization and amplification to run in parallel for a fast pipelining operation. The 6b ADC consists of 6 pipelined stages with 6 comparators and 5 amplifiers in total. Such small number of hardware reduces the overhead from the calibration and enables fully on-chip implementation. By further sharing the calibration hardware between the offset and gain calibration, the ADC with on-chip calibration only occupies 0.0166 mm^2 in 28 nm CMOS. With a linearized dynamic amplifier for the residue amplification, the ADC achieves 34 dB SNDR with a Nyquist input with 3.3 GS/s, consuming 5.5 mW and yielding a 40.02 fJ/conversion-step Walden FoM.**

***Index Terms*—Analog-digital conversion, Calibration, Pipelined ADC, Linearization Technique, Dynamic Amplifier**

I. Introduction

MULTI-GS/s and modest-resolution analog-to-digital converters (ADCs) with low power are the key blocks for digital communications systems, such as ADC-based serial links. The SAR ADC offers a high power efficiency while its sampling rate is limited below 1.5GHz per channel, even with the multi-bit [1]-[3], two-step [4], alternative comparator [5], or the loop unroll technique [6]. Time-interleaved SAR ADCs [7]-[9] keep the efficiency but suffer from the offset and gain mismatch as well as the timing artifact among channels [10]. Such impairments often require hardware-hungry calibration and complex input-buffering front-end to resolve. Flash ADCs are well-known for their superior speed performance with minimal latency, it however brings along high power, large input capacitance and kickback. Even with folding [11] or interpolation techniques [12], either the power and/or the calibration efforts are still significant, and those calibrations are often accomplished off-chip.

The pipelined architecture is typically adopted for ADCs with 9~12-bit resolution and a moderate sampling rate around 2 GS/s per channel [13][14]. Each stage (except the last) of the pipeline accomplishes three major operations: sampling, quantization, and residue amplification. Previous art [15] demonstrated this operation sequence can be avoided by generating the residue with the reference-embedded dynamic pre-amplifiers. However, as the reference is realized by unbalancing the loading capacitance of the pre-amplifier's outputs, its accuracy relies on its tuning step, limiting the comparator's regeneration speed and overall sampling rate of the 6b ADC to only 550 MHz.

Another concern is the linearity of the residue amplifiers. Reference [15] avoids this issue by activating different dynamic pre-amplifiers for each ADC threshold and calibrating the threshold to the desired value. This however limits the implementation into a tree structure with additional hardware and calibration overhead. Conventional closed-loop amplifiers call for high gain and suffer from stability issues, and they are also power-hungry. Dynamic amplifiers (DAs) can improve the power efficiency as well as the speed, but the linearity is relatively poor due to the input-dependent common current, especially under a large input swing. While calibration [16] requires a high order post-distortion extraction procedure that is hardware hungry, the time-domain linearization technique [17] limits the amplification speed significantly with the common-mode (CM) detector.

In this work, we revisit the classical operation sequence in the pipeline architecture. Rather than executing the sampling, quantization and amplification in series, we propose a post-amplification residue generation scheme that allows the quantization and amplification to happen simultaneously [18]. Each stage's residue is generated by a capacitive DAC and amplified by the DA for high speed and low power operation. The linearity of the amplifier is ensured by an auxiliary compensation technique which only induces a mild penalty on the amplification speed. The proposed architecture enables a simple and low-hardware implementation that eases the calibration hardware and effort, enabling a fully-on-chip calibration design. The ADC prototype runs at 3.3 GS/s and consumes 5.5 mW under a 0.9 V supply. It achieves 34 dB SNDR and 45 dB SFDR with a Nyquist input and an ERBW greater than 6 GHz. The total area including on-chip calibration is only 0.0166 mm^2.

Section II describes the ADC with the proposed architecture and techniques. Section III introduces the linearization technique for the high-speed DA. Section IV illustrates the calibration details. Sections IV and V include the CM Propagation in the Pipeline and Calibration, respectively.

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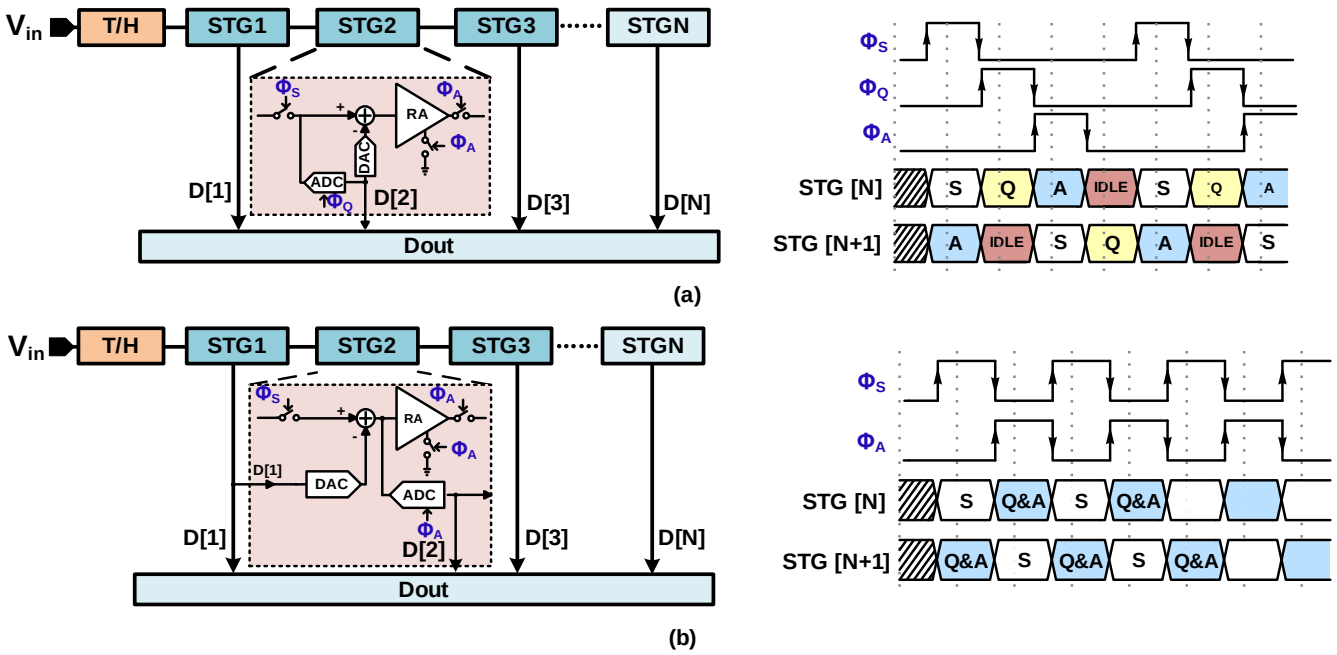

Fig. 1 (a) Conventional pipelined ADC architecture and timing diagram, (b) pipelined ADC with proposed PARG scheme.

Section VI presents the overall ADC architecture while Section VII exhibits the measurement results. Finally, Section VIII draws the conclusions.

II. Review of Pipeline ADC and Proposed Modification

A. *Review of pipelined ADCs*

Fig. 1 (a) shows the conventional pipelined ADC structure and its timing diagram. It can achieve high-speed thanks to the pipelining operation and the fast flash sub-quantizer, with extended resolution obtained by cascading multiple low-resolution stages. Each stage (except the last) generally consists of a sampler, a sub-quantizer, and a multiplying digital-to-analog converter (MDAC). The operation of this conventional pipelined ADC with open-loop amplifier can be described as follows. First, the input signal (V_{in}) is sampled during the Φ_S and is quantized afterwards with the sub-quantizer during Φ_Q. Then, the residue voltage is generated by the DAC according to the quantization results, which is further amplified during Φ_A and passed to the subsequent stages for further quantization. Under a low-to-moderate resolution target, the time required for the sampling, quantization and amplification is similar, which leaves out an idle time slot. This classical arrangement accomplishes serially three major operations, including sampling, quantization, and residue amplification. The amplification (Φ_A) thereby must wait for the completion of the quantization as well as the DAC feedback (Φ_Q), leading to an inefficient time allocation with idle time in each pipelined stage.

B. *Post-amplification Residue Generation Pipelined architecture*

In contrast to the conventional sub-stage operation, Fig.1 (b) illustrates a post-amplification residue generation (PARG) pipeline architecture [18]. While each pipelined stage shares the same hardware as conventional pipeline ADC, its operation is rearranged to avoid idle time. First, the input signal (V_{in}) is sampled during the Φ_S and is quantized by the sub-quantizer during Φ_A. Simultaneously, the sampled input is also amplified by the RA within Φ_A and passes the result to the subsequent stages for residue generation and further quantization. Instead of amplifying the residue, now the RA amplifies the full sampled input, and the residue is generated afterward by adding/subtracting the proper reference voltage from its output. The residue generation thus happens after the amplification which allows the comparator and the RA to work in parallel. The parallelized operation accelerates the overall speed by allowing each stage to accommodate only two basic operations: sampling and conversion/amplification, effectively eliminating the idle time.

C. *Conventional and PARG Pipeline ADC*

Under the same target resolution, the required time for sampling (T_{SAM}), amplification (T_{AMP}) and comparison (T_{comp}) can be unified when comparing the conventional pipeline and the PARG scheme. The smallest possible clock period of the conventional pipelined ADC is:

$$T_{CLK} = T_{SAM} + T_{setup} + T_{pre} + T_{comp} + T_{AMP} + T_{DAC} \quad (1)$$

where T_{setup}, T_{pre} and T_{comp} are the setup time of the sampled input/residue voltage, pre-discharge time and regeneration time of the comparator, respectively. The T_{DAC} is the DAC logic delay. In the conventional setup, each stage (except the last) must conclude sampling, comparison, and amplification where certain timing overheads, such as setup time and pre-discharge time of the comparator, are inevitable due to the serial operation in each stage. While with the post-residue amplification scheme, the shortest clocking period can decrease down to:

$$T_{CLK} = T_{SAM} + T_{setup} + T_{pre} + T_{comp} \quad (2)$$

Noted that T_{AMP} is saved, and T_{DAC} and T_{setup} can be merged as the amplification and comparison now happen at the same time. Here, we assume $T_{pre} + T_{comp} > T_{AMP}$, since the regeneration time of the comparator is often more critical than the amplification time in high-speed scenarios. The PARG can provide a 1.5-fold improvement in conversion speed compared to the conventional pipelined ADC for a low-to-moderate resolution target. Or in other words, it gives an additional 1/3 of regeneration time for the comparator, thus improving the metastability error rate of the ADC. It is also worth noting that the optimum timing of Fig. 1 (a) requires a clock pulse-width modification, shortening the sampling time from half period, which is sensitive to PVT variations. While the half-period setup in the proposed PARG is more robust, the actual saving or speed enhancement is higher than the discussed value above.

III. Linearized Dynamic Amplifier

An open-loop type MDAC provides a convenient and a high-speed way to facilitate the PARG since the amplified voltage is held on the succeeding stage's capacitor, it places a higher pressure on the linearity requirement of the residue amplifiers as they interface with larger signal swings, especially at the initial stages. In this design, the dynamic residue amplifier is adopted due to its outstanding energy efficiency and fully-dynamic power property. While the speed-limiting CM detection is removed and its gain accuracy is ensured by the calibration as detailed in Section V later, a linearization technique is necessary to reach a reasonable SFDR performance even for a low-to-moderate resolution target.

A. *Linearity of Dynamic Amplifiers*

The circuit schematic of the conventional DA [19] and its transient waveforms are depicted in Fig. 2. Its basic working principle is discharging the supply-pre-charged load capacitors through an input-controlled current source. While the pre-charging process happens during the reset phase Φ_{RST} and the capacitive loads (C_L) are reset to VDD , the amplification takes place at the amplification phase Φ_{Amp}. During Φ_{Amp}, the DA is similar to a classic differential trans-conductance amplifier, where the differential pair discharges the output nodes (V_O / V_{O+}) from the pre-charged value (VDD) to ground. The discharge process terminates when Φ_{Amp} goes low again. Based on this operating principle, the voltage gain A_V of the DA becomes:

$$A_V = \frac{G_m}{C_L} \cdot T_{amp} \approx \frac{g_{m1}+g_{m2}}{2} \cdot \frac{1}{C_L} \cdot T_{amp} \qquad (3)$$

where g_m, C_L and T_{amp} are the trans-conductance of the input transistors, the load capacitance, and the amplification time, respectively. Regarding the integrating nature of the discharging process, it is desirable that the output differential current ($I_{D2} - I_{D2}$) are linearly related to the input voltage and consistent throughout time. However, the drain-source current of the MOSFET is 2nd order dependent on its overdrive voltage according to the square-law model, and thereby it fails to linearly follow the input, originating nonlinearity in the amplification. The nonlinearity induced by the differential input pair can be obtained by exploring the relationship between the

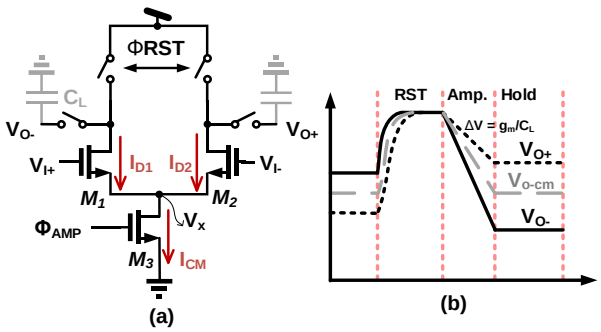

Fig. 2. (a) Schematic and (b) signal behavior of the conventional differential dynamic amplifier.

differential drain current of an input pair and its differential input voltage based on the square-law equation [20]:

$$I_{D1} - I_{D2} = \frac{1}{2} k (V_{I+} - V_{I-}) \sqrt{\frac{4I_{CM}}{k} - (V_{I+} - V_{I-})^2} \qquad (4)$$

where I_{D1} and I_{D2} are the drain currents generated by M1 and M2 in the amplification phase for the inputs V_{I+} and V_{I-} , respectively. I_{CM} represents the common-mode current, and $k = \mu C_{ox} \frac{W}{L}$, which are the geometry and process parameters of the MOSFETs. The nonlinearity originated by the I_{CM} term can be suppressed through a careful sizing of M_3, which reduces the channel length modulation effect. Consequently, I_{CM} is mainly controlled by the gate-source voltage of M_3 and is relatively constant within the amplification. On the other hand, the input pair originates a second-order input-dependent term $(V_{I+} - V_{I-})^2$ inside the square-root part in (4), imposing that the differential output current fails to follow the input linearly. This leads to a compressing type of nonlinearity as the square-root term decreases when the input difference grew. Such type of nonlinearity is the major bottleneck and becomes severe with the large input swing in the first initial pipelined stages.

B. *Linearization of High-speed Dynamic Amplifiers*

Despite there are various techniques to linearize the DA in the literature, they are seldom applicable to high-speed scenarios or robust enough over PVT. Next, we will introduce a linearization technique, which results in a mild effect on the speed of the DA.

1) *Proposed Linearization Technique*

As described in (4), the input-pair-induced nonlinearity is related to the 2nd-order dependency of the MOSFET drain current on the input ($(V_{I+} - V_{I-})^2$ term). The presented idea alleviates its impact by making the term under the square-root part in (4), $\sqrt{\frac{4I_{CM}}{k} - (V_{I+} - V_{I-})^2}$, approach to a constant value. Fig. 3 displays the proposed DA with an auxiliary path for linearization. On top of the conventional DA structure, an auxiliary pseudo-differential input pair M_4-M_5 with clock-controlled through M_6-M_7 is added. They share the same main clock signal Φ_{Amp} with the DA and provide compensation currents I_{D1Aux} and I_{D2Aux} . The sum of the compensation current is:

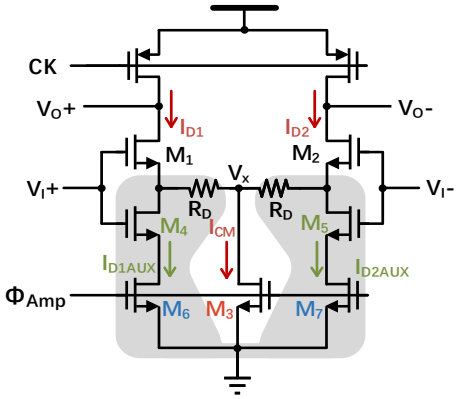

Fig. 3. Dynamic Amplifier with proposed linearization technique.

$$I_{sum,Aux} = I_{D1Aux} + I_{D2Aux} = c + \frac{1}{2}k_1(V_{I+}^2 + V_{I-}^2) \quad (5)$$

where $k_1 = \mu C_{ox}\frac{W}{L}$ is the geometry and process parameters of M_4 / M_5, and the variable c is:

$$c = 2k_1(V_{th-Aux}^2 - 2V_{th-Aux}V_{CM}) \quad (6)$$

where V_{th-Aux} is the threshold voltage of the auxiliary pair. As $I_{sum,Aux}$ in (5) is in parallel with I_{CM}, the 2nd-order input-dependent term $(V_{I+}^2 + V_{I-}^2)$ in (5) compensates the nonlinearity from $(V_{I+} - V_{I-})^2$ in (4). After including the compensation, equation (4) becomes:

$$I_{D1} - I_{D2} = \frac{1}{2}k(V_{I+} - V_{I-})\sqrt{\beta} \quad (7)$$

where:

$$\beta = \frac{4I_{CM}}{k} + \frac{4k_1}{k}\left(V_{CM} - V_{th,AUX}\right)^2 + \left(\frac{k_1}{k} - 1\right)(V_{I+} - V_{I-})^2 \quad (8)$$

It can be noticed from (8) that the perfect compensation happens when $k_1 / k = 1$ in which the differential current in (4) becomes:

$$I_{D1} - I_{D2} = \frac{1}{2}k(V_{I+} - V_{I-})\sqrt{\frac{4I_{CM}}{k} + 4\left(V_{CM} - V_{th,AUX}\right)^2} \quad (9)$$

Comparing (4) with (9), the 2nd-order terms, V_{I+}^2 and V_{I-}^2, are canceled by introducing auxiliary paths, while β in (8) depends only on constant values: V_{CM}, V_{th-Aux}, μ, C_{ox} and transistor geometries as well as I_{CM}.

2) Source Degeneration

DAs are based on the differential pair configured in the common-source fashion, and thus the source-degeneration technique is also effective for its transconductance (g_m) linearization. By adding a degeneration resistor R_D, a negative feedback is induced, which suppresses the gain variation of the DA. With the major portion of g_m nonlinearity suppressed by the previously discussed auxiliary path, the degeneration mainly alleviates the input dependency of I_{CM} for better overall linearity. The nonlinearity from I_{CM} is also significant since the drain-source voltage of M_3 (V_x) is also dependent on the input, which eventually affects β in (8) even when $k_1 / k = 1$. However, the degeneration also turns the effective G_m of the input pair that become $\frac{g_m}{1+g_m R_D}$, thus reducing the overall gain of the DA.

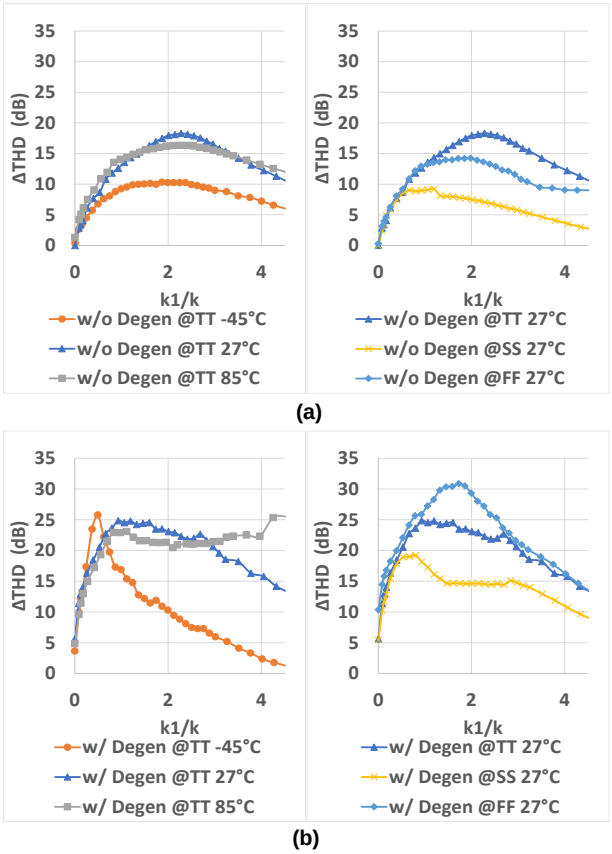

Fig. 4. Dynamic Amplifier with proposed linearization technique (a) THD improvement vs k_1/k with aux. pair only (b) THD improvement versus k_1/k with degeneration.

Such loss is partially compensated by the proposed linearization technique as its gain is superior to the conventional design (see Appendix I). Simulation results show that degeneration resistors provide an extra 6 dB linearity improvement on top of the proposed linearization technique under typical conditions; the overall THD improvement with both linearization techniques is no less than 16 dB across different corners and temperatures.

3) Design Considerations and PVT Simulations

A special attention is necessary to be paid on M_4 and M_5 to achieve the linearization goal. M_4 and M_5 share the same gate voltage as M_1 and M_2, but a lower source voltage, leading to a higher V_{GS}. Thus, the threshold voltage of M_4 and M_5 needs to be higher than that of M_1 and M_2 to maintain a reasonably small overdrive voltage for a sufficient V_{dsat} headroom. Therefore, M_1 and M_2 are implemented with LVT devices while M_4 and M_5 are HVT devices to comply the overdrive constraint. Fig. 4 plots the simulated THD improvement for different k_1/k ratios across several process and temperatures for various linearization options. To obtain these results, the tail current is fixed and the biasing condition of M_3, and the g_m of the main input pair M_1 and M_2 are also fixed for a fair comparison. Besides, the differential gain and the input swing are carefully adjusted to a similar level in all simulations. Fig. 4 (a) shows that the auxiliary pair gives about 10 dB linearity improvement with $k_1/k = 1$. Such ratio is set by the physical properties of the

main and auxiliary NMOS input pairs, where the only source of variations on the k_1/k ratio is the mismatch and therefore it is expected to be immune to the PVT variations. However, the proposed linearization technique compensates only the g_m-induced nonlinearity of the input pair and there are remaining nonlinearities originated from g_{ds} as well as high order terms which are PVT sensitive. As a result, the overall improvement varies across different PVT conditions, and the best compensation moves away from k_1/k=1. While the overall improvement stays above 16 dB for k_1/k within 0.25 to 1.25 as shown in Fig. 4 (b), a proper choice of k_1/k and the degeneration resistance allows the proposed DA to tolerate a certain range of temperature variation. We choose k_1/k =0.7 in this design to ensure a sufficient THD performance over PVT. we choose k_1/k=0.7 in this design to ensure a satisfactory performance over PVT.

IV. Common-Mode Propagation in Pipelined ADC

In order to achieve a high-speed amplification, the CM detector in the conventional DA is omitted in our design. While the calibration ensures the gain accuracy, the DA output CM can experience a significant variation under process corners. Improper common-mode voltage can dramatically degrade the performance of the DAs and induce errors in the residue propagation through the pipeline, causing failure in the overall ADC conversion. The total output CM variation of the DA in the proposed pipelined ADC originates from two primary sources: 1) the common-mode gain inherent from the DA; 2) the differential gain variation from the DA that needs an adaptive output CM for compensation. Next, we will analyze the CM variation of the conventional and proposed linearized DA and discuss their design considerations.

A. Common-Mode Analysis of Dynamic Amplifiers

1) Conventional Dynamic Amplifier

For a given desired gain (A_v), the output CM voltage of the conventional DA is:

$$V_{CM,O} = VDD - \frac{A_V}{2}\frac{I_{CM}}{g_m} \tag{10}$$

where I_{CM} is the CM tail current. The $V_{CM,O}$ of the conventional DA is ideally independent of the input CM voltage ($V_{CM,I}$) as indicated in (10). However, the drain voltage of the tail transistor indeed is related to the $V_{CM,I}$ and therefore affect I_{CM}. This relationship can be depicted as:

$$2I_{D0} = k\left(V_{CM,I} - V_x - V_{TH}\right)^2 = I_{CMo} + g_{ds,M3}V_x = I_{CM} \tag{11}$$

where I_{D0} is the CM drain current and I_{CMo} is the nominal CM tail current. g_{ds} is the drain-source transconductance of the tail transistor. From (11), M_3 provides an additional current ($g_{ds}V_x$) when the $V_{CM,I}$ changes (as well as V_x), eventually altering the output CM voltage of the DA. Then, we can rewrite (10) as:

$$V_{CM,O,conv} = VDD - \frac{A_V}{2}\left(\frac{I_{CM0}}{g_m} + \frac{g_{ds,M3}V_x}{g_m}\right) \tag{12}$$

The CM gain can be evaluated by taking the derivative of $V_{CM,O,conv}$ with respect to $V_{CM,I}$, leading to:

$$A_{CM,conv} = -A_V\frac{g_{ds,M3}}{2g_m} \tag{13}$$

Since the common-mode gain of DA is desired to be small for a robust pipeline operation, we design the clock-controlled tail current source M_3 with a minimized channel-length modulation effect, and the input pair M_1 and M_2 for maximum transconductance g_m. A small A_V and a reasonable choice of $g_{ds,M3}$ and g_m bring $A_{CM,conv}$ down to ~ -30 dB, which constitutes a negligible CM gain. Eventually, the overall CM from (12) remains to $VDD - A_V\left(\frac{I_{CM0}}{2g_m}\right)$. Across process corners, A_V experiences a ~30% variation which leads to a ~15.4 mV output CM variation for a proper gain after calibration.

2) Proposed Linearized Dynamic Amplifier

The above analysis can be applied to the proposed linearized DA. The CM drain current becomes:

$$I_{D0,lin} = I_{CM0} + g_{ds,M3}V_x + 2I_{D0,Aux} \tag{14}$$

where $I_{D0,Aux}$ is the CM drain current of the auxiliary pair. The overall CM variation of the linearized DA is:

$$V_{CM,O,lin} = VDD - \frac{A_V}{2}\left(\frac{I_{CM0}}{g_m} + \frac{g_{ds,M3}V_x + 2g_{m,Aux}V_{CM,I}}{g_m}\right) \tag{15}$$

and the CM gain therefore is equal to:

$$A_{CM,lin} = -A_V\frac{g_{ds,M3} + 2g_{m,Aux}}{2g_m} \tag{16}$$

where $g_{m,Aux}$ is the transconductance of the auxiliary pair. Unlike the conventional DA, the CM gain of the linearized DA can be higher than 1, especially in the optimal linearization condition. When $k_1=k$, the overdrive voltage of the auxiliary pair is larger than that of the main input pair due to the tailless configuration. Therefore, the auxiliary pair M_3 and M_4 should be carefully designed to guarantee $g_{m,Aux} \ll g_m$. The CM gain combined with the CM variation caused by the differential gain variation potentially induces a too large/small CM voltage at the later stages of the pipeline, leading to a hard conversion error.

B. Failure Condition and Common-Mode Voltage Design Consideration

The CM voltage propagation up to specific stage (N-th stage) in the entire pipeline can be obtained through the CM voltage propagation property of DAs presented before. The general form of a single stage will be:

$$V_{CM,O} = VDD - A_V\frac{I_{CM0}}{2g_m} + A_{CM}V_{CM,I} \tag{17}$$

and the propagation of N cascading stages is:

$$V_{CM,O[N]} = V_{CM,O} + \Delta V_{CM,I}\prod_{m=1}^{N}A_{CM,O[m]} \tag{18}$$

where $A_{CM,O[N]}$ is the output CM gain of the N-th stage. Since the CM voltage is strongly correlated to the DA's gain (A_V), it eventually reaches an adaptive value after the gain calibration. Nevertheless, even with a proper gain, the DAs can still induce severe nonlinearity with inappropriate CM voltage. $V_{CM,O}$ should be accommodated into a range that leaves enough

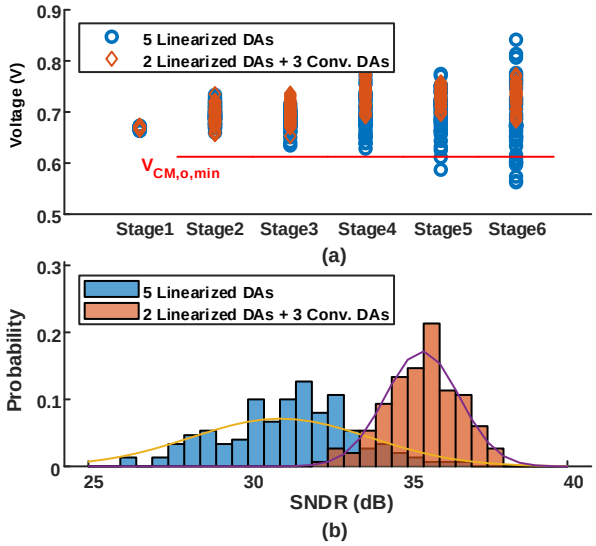

Fig. 5. 200-iteration Monte-Carlo simulation results of (a) output common-mode voltage of each stage (b) overall ADC SNDR.

margin (large V_{DS}) of the input and tail transistors to saturate, setting its lower bound value as:

$$V_{CM,o,min} > V_{dsat,MAIN} + V_{dsat,AUX} + A_V \frac{(V_{i+}-V_{i-})}{2} \quad (19)$$

Based on (18) and with the criteria indicated in (19), it is desirable to have A_{CM} smaller than 1. While as discussed previously with (16), the A_{CM} of the proposed linearized DA can be larger than 1 when $k_1/k = 1$. Fig. 5 (a) illustrates the output common-mode voltage with different DA arrangements in a 200-run Monte Claro simulation of the proposed pipelined ADC. It can be observed that the variance is relatively large and exceeds $V_{CM,o,min}$ in the 4th stage when solely adopting the linearized DAs in all the stages. That leads to a dramatic performance drop as indicated in Fig. 5 (b). To meet the stringent linearity requirement and ensure a proper accumulated common-mode voltage in the final stages of the pipeline, we only adopt the linearized DA in the first two stages thereby keeping the output common-mode variation in each stage within $V_{CM,o,min}$ and the overall SNDR centered at ~35dB with a one-sigma variation of ~1dB.

V. Calibration

Similar to the conventional architecture, the proposed pipelined ADC is sensitive to inter-stage offset and gain-error impairments. In addition, due to the stringent linearity requirement, the gain mismatch between the signal paths of the DA is also critical. Originated from mismatch and process variations, the offset of the comparators and dynamics amplifiers as well as the inter-stage gain error from the residue amplifier significantly limit the overall performance of the ADC. While redundancy among stages is often introduced in the conventional approach to mimic the offset error, it however complicates the quantizer design as it necessitates multiple reference voltages and comparators in each stage. Besides, it cannot correct the nonlinearity caused by the gain mismatch between the signal paths of the DA. Instead, in this design, both

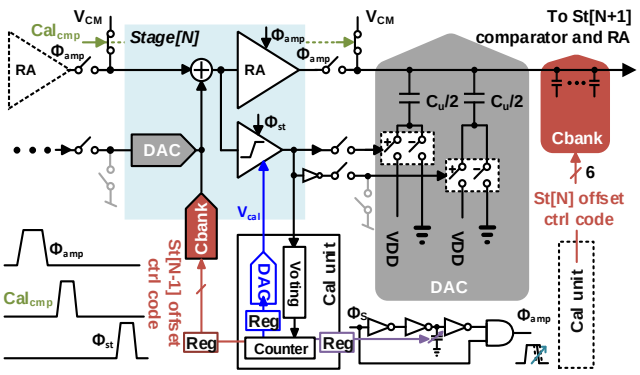

Fig. 6. Detailed block diagram of the offset and gain calibrations.

offset and gain impairments are suppressed through a hardware-sharable and low-cost foreground calibration. The calibrations run sequentially, starting with comparator offset, amplifier signal-path gain mismatch, and then followed by the amplifier gain. Their block diagram is depicted in Fig. 6 with each calibration detailed next.

A. Comparator Offset Calibration

The offset calibration of the comparators starts from the 1st stage and each stage accomplishes in sequence. During the calibration, the ADC works as normal, but the bottom plate of the DAC keeps resetting and disconnecting from the comparator control. The differential inputs of each stage are shorted together after amplification, which generates the corresponding common-mode voltage for the offset calibration. The comparator gives a decision during Φ_{ST}, indicating the offset polarity. The decision passes through an 8-time majority voting logic and controls the counter. The counter value further employs a 6b R-2R DAC which provides a calibration voltage V_{cal} to adjust the offset of the comparator through an additional input calibration pair. The step size of V_{cal} is 7 mV and the ratio between the input pair and the calibration pair is 1: 0.2, that covers 3-sigma ±30 mV offset.

B. Dynamic Amplifier Offset and Signal-path Gain Mismatch Calibration

The offset and the signal-path gain mismatch of the DA are calibrated together. While the offset error can saturate the succeeding stage, the signal-path gain mismatch causes severe nonlinearity. Given that both signal paths experience the same nonlinearity, their gain therefore undergoes the same characteristic and does not worsen the linearity performance. Nevertheless, due to the mismatch between the signal paths, their transfer characteristics can shift and scale, worsening the differential gain nonlinearity. Fig. 7 (a) illustrates the analytical model of the DA and its single-ended outputs is:

$$Vo +/-= V_{DD} - \frac{\frac{I_{D0}}{2} - \Delta V_{IN} \cdot g_{m,+/-}}{C_L} T_{AMP} \quad (20)$$

where I_{D0} is the common-mode current, g_m is the transconductance of the input transistor, T_{AMP} is the amplification time and C_L is the loading capacitance of the DA.

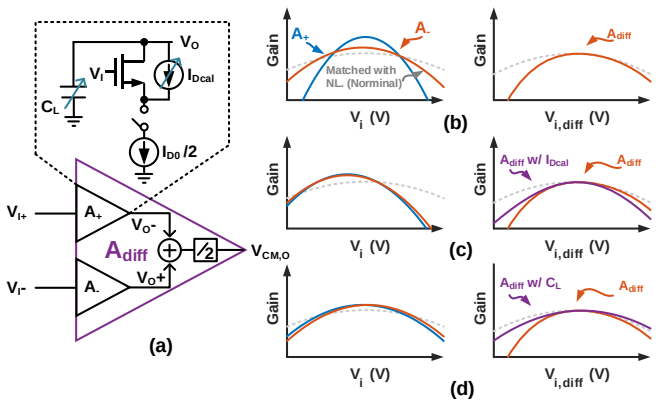

Fig. 7. (a) The analytical diff-path mismatch model of the DA (b) offset and diff-path gain mismatch as well as overall nonlinearity. (c) calibration characteristic with I_{Dcal} (d) calibration characteristic with C_L.

Based on (20), the offset can be compensated by adjusting I_{D0}. However, such compensation only aligns the center point of the deviated gain curves rather than the overall gain characteristic as $\frac{g_m}{C_L}$ remains unchanged. With offset and signal-path (A_+ / A_-) gain mismatch as presented in Fig. 7 (b), the overall nonlinearity of the differential gain A_{diff} becomes worse. With adjustment accomplished through I_{Dcal}, the offset can be well compensated, but it does not repair the nonlinearity (Fig. 7 (c)).

Instead of trimming I_{D0} with an extra pair, we manage to trim the loading capacitors (C_L) of the differential outputs which compensates both the offset and the differential gain error at the same time. It is worth noting that both errors can be suppressed simultaneously as C_L appears in the denominator of (20). While I_{D0} and g_m may not experience the same amount of variation under mismatch, the calibration thereby potentially leaves a residual error as depicted in Fig. 7 (d). As both gain curves experience almost the same nonlinearity, it does not introduce much extra nonlinearity to the differential gain. Different from the comparator offset calibration, the differential outputs of the calibrating DA stage do not connect together. It therefore can stimulate the I_{D0} mismatch who can be sensed by the subsequent comparator. Based on the I_{D0}mismatch between the differential paths,C_L is adjusted accordingly, which at the same time in the 1st-order corrects the $\frac{g_m}{C_L}$ mismatch for better linearity. Based on the 500-iteration Monte-Carlo post-simulation result of the proposed design in Fig. 8, the 3-sigma THD of the DA after calibration stays within -45 dB centered at -52 dB which fulfills the 6b requirement. It also confirms that adjusting the current with an extra input pair gives rise to additional nonlinearity even with offset successfully removed. The tunable load C_{Bank} is 6-bit with a tuning step of 0.15 fF, covering 30% variation of the DA. The calibration logic is similar to the comparator offset calibration as introduced in the previous section, and therefore most of the hardware can be shared for compactness.

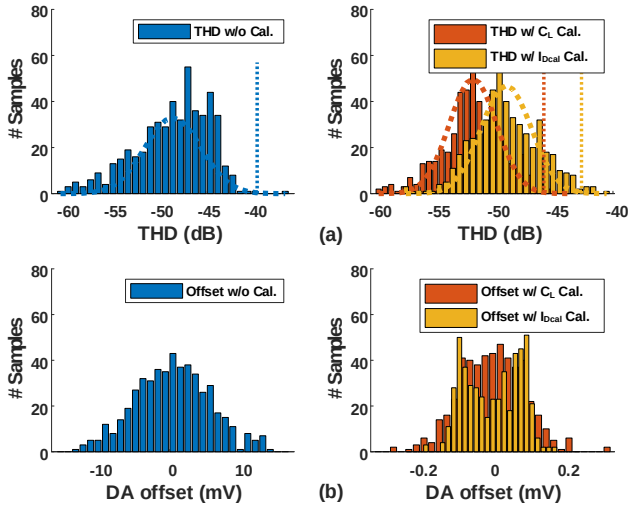

Fig. 8. 500-iteration Monte-Carlo Simulation of (a) DA's THD with and without calibration (b) DA's offset with and without calibration.

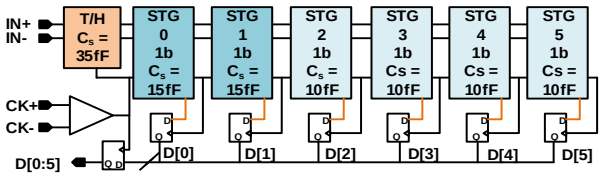

Fig. 9. Overall Architecture.

C. *Amplifier differential gain*

The inter-stage gain error is calibrated from the last to the first stage. To detect the gain error of stage N (with nulled offsets in the comparator and amplifier), a half-LSB voltage is generated in the DAC of stage N through $\frac{C_u}{2}$ while others keep reset. Then, it is amplified and quantized by the current and/or subsequent stages. The quantization result D[N:5] is ideally $2^{(6-N)}$ -1, which is the full-scale of stage N to stage 5. The calibration starts with a minimum gain configuration and increases the gain until D[N:5] approaches its ideal value. As the output common-mode of the DA has a strong correlation with the gain, such calibration also ensures proper inter-stage CM voltages. The gain adjustment is accomplished by varying the amplification time. It can achieve a linear tuning step and at the same time does not affect the offset and differential-path gain error of the DA as the differential-path impairments are calibrated out through $\frac{g_m}{C_L}$. An 8-bit digital-controlled delay line is utilized to adjust the amplification time where each step is 117 fs resulting in a 0.0015 gain step. The fore-ground calibrated gain holds sufficiently good for our target resolution as the amplification time (T_{amp}) also varies accordingly with temperature. The post-layout simulation result shows that the gain variation is within ±1% from -20 to +85 ˚C, which has a neglectable effect on the ADC performance. Again, most of the logic can be shared with other calibrations and enables a compact design.

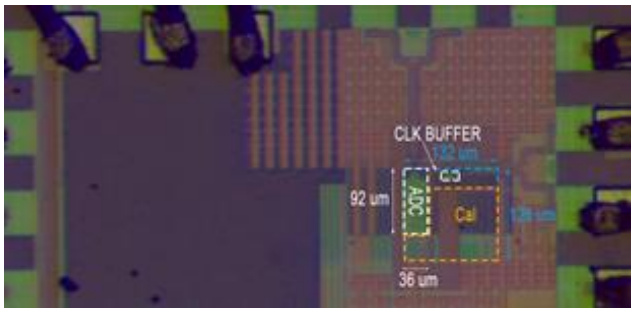

Fig. 10. Die photo.

VI. Overall ADC Implementation

The overall ADC consists of six 1b stages which aggregate 6-bit resolution as depicted in Fig. 9. No redundancy is inserted among stages to obtain the best efficiency and avoid the need of multiple reference voltages, while the gain and offset error are calibrated in the foreground as discussed in Section V. The PARG scheme introduced in Section II is adopted which allows the quantization and amplification to run in parallel for high speed. The inter-stage gain is around 1.5x, keeping a balance between the first few stages' linearity and later stages' noise/accuracy requirement. The low 1.5x gain is due to the stringent linearity requirement which is a drawback of the PARG scheme. However, with the 6b target in this design, such small gain does not lead to a large tradeoff between noise and power, and therefore, the PARG scheme is well suitable to high- speed and low-resolution designs. Only the DAs in the first two stages utilize the proposed linearization technique and the rest stages maintain the conventional DA to ensure a proper common-mode range through the pipe. The Auxiliary path in the proposed DA brings a faster dropping VCM compared to conventional architecture, which degrades its maximum achievable amplification time and noise performance. However, our design is not noise-limited, and the bottleneck is the linearity. Such noise performance degradation has no impact on the overall ADC energy efficiency. The sampling capacitances of the first, second and third stage stage are 35 fF, 15 fF and 15 fF, respectively, and 10 fF for the remaining stages. Such small capacitance ensures a high speed and low power operation. Split monotonic switching is adopted to generate the residue in each stage, which avoids an additional CM voltage. The outputs of each stage are aligned with the D-flip-flop.

VII. Measurement Results

The ADC is fabricated in 28 nm CMOS, with ~40 fF input capacitance (excluding ESD) and occupies an active area of 0.0166 mm^2 (132 µm x 126 µm), including on-chip calibration circuits as shown in Fig. 10. The input swing of the prototype is $400mV_{pp\text{-}diff}$ to adopt the PARG scheme. During measurements, the on-chip calibration is performed at the foreground and the calibration counter values are frozen throughout all conditions. Fig. 11 (a) illustrates the measured output spectrum (decimated by 225) at 3.3 GS/s for an input near Nyquist (1.649 GHz), with and without calibration. Before the calibration, the 2nd and 3rd harmonic dominate the SFDR and

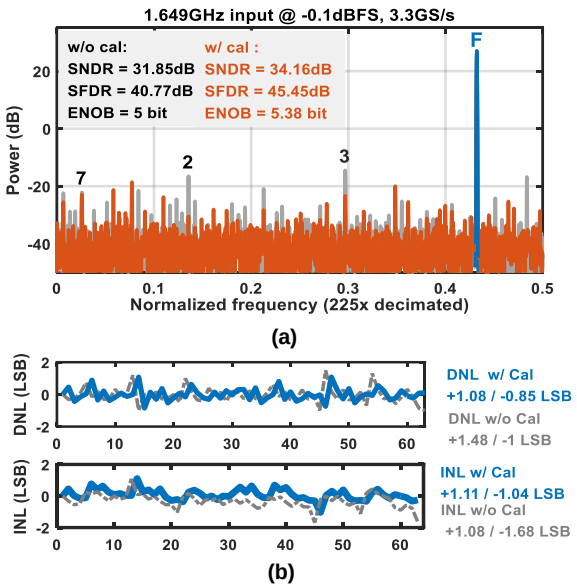

Fig. 11. Measured ADC (a) spectrum at near Nyquist input and (b) DNL/INL before and after calibration.

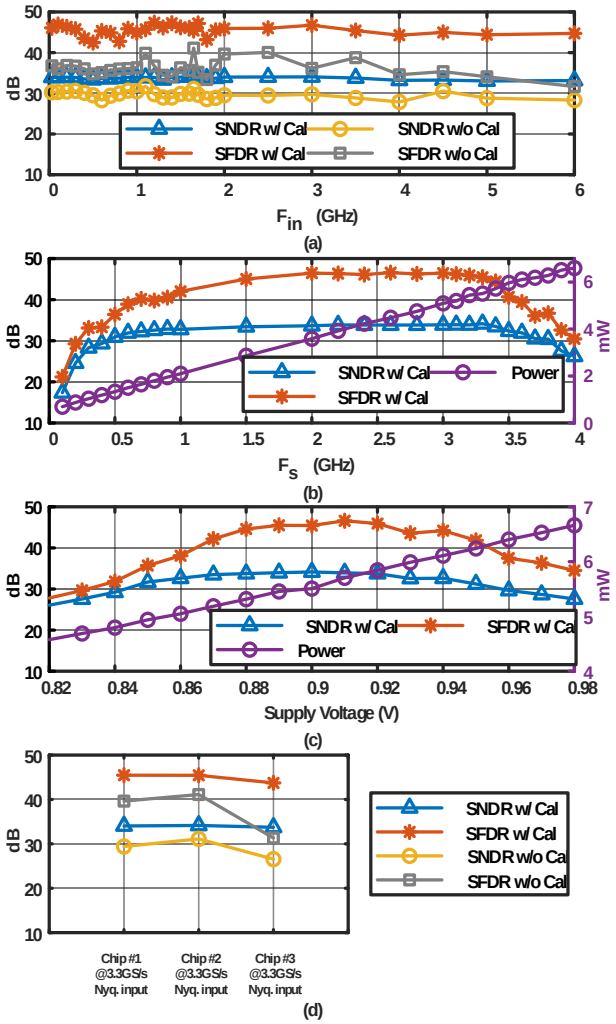

Fig. 12. ADC performance sweeps (a) versus F_{in}. (b) versus F_s. (c) versus supply voltage (d) versus randomly selected samples

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART

	This work	Verbruggen [15] JSSC'10	Chen[21] VLSI'13	Shu[22] VLSI'12	Oh [12] JSSC'19
Architecture	Fully Dynamic Pipeline	Fully Dynamic Pipeline	Flash	Flash	Flash
Technology	28nm	40nm	32nm SOI	40nm	65nm
Supply (V)	0.9	1.1	0.85	1.1	0.85
Power (mW)	5.5	2.6	8.5	11	7.5
ERBW (GHz)	>6	2	2.43	1.5	3.1
Resolution (bit)	6	6	6	6	6
f_s (GS/s)	3.3	2.2	5	3	2.5
SFDR@Nyq.(dB)	45.45	41.5	37.48	38	45.07
SNDR@NYQ.(dB)	34.16	31.1	30.9	33.1	33.8
FoM@Nyq (fJ/conv.-step)	40.02	40.3	59.4	99.3	74.7
Active Area(mm^2)	0.0166	0.03	0.02	0.021	0.12
Calibration	On-chip	Off-chip	Off-chip	Off-chip	On-chip

greatly limit the achievable SNDR. The mismatches between differential circuits cause mainly the second harmonic, while the offset and gain error results in the third harmonic. These harmonics are reduced once the calibration is done, and the SFDR is improved by 5 dB. Moreover, as depicted in Fig. 11 (b), the measured DNL and INL before calibration are +1.48 / -1 LSB and +1.08 / -1.68 LSB, and after calibration are +1.08 / -0.85 LSB and +1.11 / -1.044 LSB respectively.

Fig. 12 (a) plots the measured SFDR/SNDR across input frequencies from DC to 6 GHz. The SNDR and SFDR maintained at ~33 dB and 45 dB thanks to the small input capacitance and bootstrapped sampling front-end. Fig. 12 (b) exhibits the SNDR and SFDR as well as the power consumption versus sampling frequencies from 1 GS/s to 4 GS/s with a fixed input at ~1.6 GHz. The performance has a significant drop beyond 3.4 GS/s due to the insufficient conversion time. At sampling rates below 300MS/s the performance degrades due to leakage on the residue holding capacitors. Their switches are sized for lowest R_{on} due to the high-speed target. Besides, it clearly shows the power consumption scales linearity versus sampling frequency with a slope of 1.5 μW/MHz, which confirms the fully dynamic characteristic of the proposed prototype. With a fixed calibration set obtained at a 0.9-V supply and no re-calibration, the SNDR degrades less than 3 dB for a ±5% supply change, as illustrated in Fig. 12 (c). Moreover, three randomly selected samples demonstrate a similar performance which further proves the effectiveness of the calibrations as depicted in Fig. 12 (d). Table I summarizes the major ADC specifications and compares them with state-of-the-art designs. The proposed prototype achieves competitive energy efficiency and SNDR in a compact area even including on-chip calibration circuitry.

VIII. CONCLUSIONS

This paper presented a 0.9 V 6-bit 3.3 GS/s pipelined ADC. The proposed post-amplification residue generation pipelined architecture effectively increases the achievable conversion rate. In order to guarantee the linearity under such high speed, an auxiliary pseudo-differential input pair is added to the conventional DA structure. A total 16-dB linearity improvement is achieved along with source degeneration. The on-chip calibration corrects the offsets, diff-path gains, and inter-stage gain errors with mostly sharable hardware, thus leading to a compact area. Compared to the state-of-the-art, the single-channel prototype ADC obtains a high speed (3.3GS/s) and decent SFDR and SNDR with competitive Walden FoM.

APPENDIX I.
GAIN OF DYNAMIC AMPLIFIERS

The differential gain of the DA can be generalized in the following equation based on the differential current (I_{diff}) and input (V_I) derivative:

$$A_{V,diff} = \frac{\partial I_{diff}}{\partial V_I} \cdot \frac{1}{C_L} \cdot T_{amp} \tag{21}$$

where I_{diff} is given by (4) and (9) for the conventional DA and proposed DA, respectively. By substituting (4) into (21), the gain of the conventional DA therefore becomes:

$$A_{V,conv} = \frac{T_{amp}}{C_L} \cdot \frac{\partial}{\partial V_I}\left(\frac{k}{2} V_I \sqrt{\frac{4I_{CM}}{k} - V_I^2}\right) \tag{22}$$

The derivative with square-root term in (22) can be approximated by a Taylor series and further simplified to only consider the first-order term, thus (22) becomes:

$$A_{V,conv} \approx \frac{T_{amp}}{C_L} \cdot \left(\sqrt{kI_{CM}}\right) \tag{23}$$

Similarly, the gain of the proposed linearized DA can be expressed as:

$$A_{V,linear} \approx \frac{T_{amp}}{C_L} \cdot \left(\sqrt{k(I_{CM} + k_1\gamma)}\right) \tag{24}$$

where $\gamma = \left(V_{CM} - V_{th,AUX}\right)^2$. As discussed in Section III, $k_1 = k$ is important for best linearization, $\sqrt{(kI_{CM} + k\gamma)}$ is obviously larger than $\sqrt{kI_{CM}}$ as γ is a positive value. It therefore can be concluded the gain of the proposed DA is superior to the conventional.

REFERENCES

[1] C. Chan, Y. Zhu, W. Zhang, S. U and R. P. Martins, "A Two-Way Interleaved 7-b 2.4-GS/s 1-Then-2 b/Cycle SAR ADC With Background Offset Calibration," in *IEEE Journal of Solid-State Circuits*, vol. 53, no. 3, pp. 850-860, Mar. 2018.

[2] C. Chan, Y. Zhu, S. Sin, S. Ben U and R. P. Martins, "A 6 b 5 GS/s 4 Interleaved 3 b/Cycle SAR ADC," in *IEEE Journal of Solid-State Circuits*, vol. 51, no. 2, pp. 365-377, Feb. 2016.

[3] D. Li, Z. Zhu, J. Liu, H. Zhuang, Y. Yang and N. Sun, "A 7-bit 900-MS/s 2-Then-3-bit/cycle SAR ADC With Background Offset Calibration," in *IEEE Journal of Solid-State Circuits*, vol. 55, no. 11, pp. 3051-3063, Nov. 2020.

[4] H. Chen, X. Zhou, Q. Yu, F. Zhang and Q. Li, "A >3GHz ERBW 1.1GS/S 8B Two-Step SAR ADC with Recursive-Weight DAC," in Proc. of 2018 IEEE *Symposium on VLSI Circuits*, pp. 97-98. Jun, 2018.

[5] L. Kull et al., "A 3.1 mW 8b 1.2 GS/s Single-Channel Asynchronous SAR ADC With Alternate Comparators for Enhanced Speed in 32 nm Digital SOI CMOS," in IEEE Journal of Solid-State Circuits, vol. 48, no. 12, pp. 3049-3058, Dec. 2013.

[6] T. Jiang, W. Liu, F. Y. Zhong, C. Zhong, K. Hu and P. Y. Chiang, "A Single-Channel, 1.25-GS/s, 6-bit, 6.08-mW Asynchronous Successive-Approximation ADC With Improved Feedback Delay in 40-nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 47, no. 10, pp. 2444-2453, Oct. 2012.

[7] L. Kull et al., "Implementation of Low-Power 6–8 b 30–90 GS/s Time-Interleaved ADCs With Optimized Input Bandwidth in 32 nm CMOS," in *IEEE Journal of Solid-State Circuits*, vol. 51, no. 3, pp. 636-648, Mar. 2016.

[8] S. Le Tual, P. N. Singh, C. Curis and P. Dautriche, "22.3 A 20GHz-BW 6b 10GS/s 32mW time-interleaved SAR ADC with Master T&H in 28nm UTBB FDSOI technology," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pp. 382-383. Feb, 2014.

[9] V. H. -. Chen and L. Pileggi, "A 69.5 mW 20 GS/s 6b Time-Interleaved ADC With Embedded Time-to-Digital Calibration in 32 nm CMOS SOI," in *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 2891-2901, Dec. 2014.

[10] B. Razavi, "Design Considerations for Interleaved ADCs," in *IEEE Journal of Solid-State Circuits*, vol. 48, no. 8, pp. 1806-1817, Aug. 2013.

[11] M. Miyahara, I. Mano, M. Nakayama, K. Okada and A. Matsuzawa, "22.6 A 2.2GS/s 7b 27.4mW time-based folding-flash ADC with resistively averaged voltage-to-time amplifiers," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pp. 388-389, Feb. 2014.

[12] D. Oh, J. Kim, D. Jo, W. Kim, D. Chang and S. Ryu, "A 65-nm CMOS 6-bit 2.5-GS/s 7.5-mW 8 $\times$ Time-Domain Interpolating Flash ADC With Sequential Slope-Matching Offset Calibration," in *IEEE Journal of Solid-State Circuits*, vol. 54, no. 1, pp. 288-297, Jan. 2019.

[13] S. Devarajan et al., "A 12-b 10-GS/s Interleaved Pipeline ADC in 28-nm CMOS Technology," in *IEEE Journal of Solid-State Circuits*, vol. 52, no. 12, pp. 3204-3218, Dec. 2017.

[14] A. M. A. Ali et al., "A 12-b 18-GS/s RF Sampling ADC With an Integrated Wideband Track-and-Hold Amplifier and Background Calibration," in *IEEE Journal of Solid-State Circuits*, vol. 55, no. 12, pp. 3210-3224, Dec. 2020.

[15] B. Verbruggen, J. Craninckx, M. Kuijk, P. Wambacq and G. Van der Plas, "A 2.6 mW 6 bit 2.2 GS/s Fully Dynamic Pipeline ADC in 40 nm Digital CMOS," in IEEE Journal of Solid-State Circuits, vol. 45, no. 10, pp. 2080-2090, Oct. 2010.

[16] R. Sehgal, F. Van Der Goes and K. Bult, "A 13-mW 64-dB SNDR 280-MS/s Pipelined ADC Using Linearized Integrating Amplifiers," in *IEEE Journal of Solid-State Circuits*, vol. 53, no. 7, pp. 1878-1888, July 2018.

[17] L. Yu, M. Miyahara and A. Matsuzawa, "A 9-bit 500-MS/s 6.0-mW dynamic pipelined ADC using time-domain linearized dynamic amplifiers," in *Proc. of IEEE Asian Solid-State Circuits Conference (A-SSCC)*, pp. 65-68, Nov. 2016.

[18] Z. Zheng et al., "16.3 A Single-Channel 5.5mW 3.3GS/s 6b Fully Dynamic Pipelined ADC with Post-Amplification Residue Generation," in *IEEE International Solid- State Circuits Conference Digest of Technical Papers* (ISSCC), pp. 254-256, Feb. 2020.

[19] J. Lin, M. Miyahara and A. Matsuzawa, "A 15.5 dB, wide signal swing, dynamic amplifier using a common-mode voltage detection technique," in *Proc. of IEEE International Symposium of Circuits and Systems (ISCAS)*, pp. 21-24, Apr. 2011.

[20] M. S. Akter, R. Sehgal, F. van der Goes, K. A. A. Makinwa and K. Bult, "A 66-dB SNDR Pipelined Split-ADC in 40-nm CMOS Using a Class-AB Residue Amplifier," *in IEEE Journal of Solid-State Circuits*, vol. 53, no. 10, pp. 2939-2950, Oct. 2018.

[21] V. H. -. Chen and L. Pileggi, "An 8.5mW 5GS/s 6b flash ADC with dynamic offset calibration in 32nm CMOS SOI," in *Proc. of IEEE Symposium on VLSI Circuits (VLSIC)*, pp. C264-C265, Jun. 2013.

[22] Y. Shu, "A 6b 3GS/s 11mW fully dynamic flash ADC in 40nm CMOS with reduced number of comparators," in *Proc. of IEEE Symposium on VLSI Circuits (VLSIC)*, pp. 26-27, Jun. 2012.

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Since Oct. 1992, has been on leave from U. of Lisbon and with the DECE, Faculty of Science and Technology (FST), University of

Macau (UM), Macao, China, where he is a Chair-Professor since Aug. 2013. In FST, he was Dean (1994-1997), and has been UM's Vice-Rector since Sep. 1997. From Sep. 2008 to Aug. 2018, Vice-Rector (Research) and from Sep. 2018 to Aug. 2023, Vice-Rector (Global Affairs). Within the scope of his teaching and research activities he has taught 21 bachelor and master courses and, in UM, has supervised (or co-supervised) 47 theses, Ph.D. (26) and Masters (21). Authored or Co-authored: 8 books and 12 book chapters; 48 Patents, USA (38), Taiwan (3) & China (7); 628 papers, in scientific journals (263) and in conference proceedings (365); as well as other 69 academic works, in a total of 765 publications. He created in 2003 the *Analog and Mixed-Signal VLSI Research Laboratory* of UM, elevated in January 2011 to State Key Laboratory (SKLAB) of China (the 1st in Engineering in Macao), being its Founding Director. He was the Founding Chair of UMTEC (UM company) from January 2009 to March 2019, supporting the incubation and creation in 2018 of *Digifluidic*, the first UM Spin-Off, whose CEO is a SKLAB PhD graduate. He was also a co-founder of Chipidea Microelectronics (Macao) [later Synopsys-Macao] in 2001/2002.

Prof. Rui Martins is an *IEEE Fellow*, was Founding Chair of IEEE Macau Section (2003-2005) and IEEE Macau Joint-Chapter on Circuits And Systems (CAS) / Communications (COM) (2005-2008) [*2009 World Chapter of the Year* of *IEEE CAS Society (CASS)*], General Chair IEEE Asia-Pacific Conference on CAS – *APCCAS'2008*, Vice-President (VP) Region 10 (Asia, Australia and Pacific) (2009-2011) and VP-World Regional Activities and Membership of *IEEE CASS* (2012-2013), Associate-Editor of *IEEE Transactions on CAS II: Express Briefs* (2010-2013), nominated *Best Associate Editor* (2012-2013). He was also member of: *IEEE CASS* Fellow Evaluation Committee (2013, 2014, 2018 – Chair, 2019, 2021 & 2022 – Vice-Chair); *IEEE* Nominating Committee of Division I Director (CASS/EDS/SSCS) (2014); and *IEEE CASS* Nominations Committee (2016-2017). Plus, he was General Chair of ACM/IEEE Asia South Pacific Design Automation Conference – *ASP-DAC'2016*, receiving the *IEEE Council on Electronic Design Automation (CEDA) Outstanding Service Award in 2016*, and also General Chair of the IEEE Asian Solid-State Circuits Conference – *A-SSCC 2019*. He was also Vice-President (2005-2014) and President (2014-2017) of the *Association of Portuguese Speaking Universities (AULP)*, and received 2 Macao Government decorations: the Medal of Professional Merit (Portuguese-1999); and the Honorary Title of Value (Chinese-2001). In July 2010 was elected, unanimously, as Corresponding Member of the Lisbon Academy of Sciences, being the only Portuguese Academician working and living in Asia.