Research Article Vol. 8, No. 12 / December 2021 / Optica 1573

OPTICA

Enabling VCSEL-on-silicon nitride photonic integrated circuits with micro-transfer-printing

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Received 31 August 2021; revised 31 October 2021; accepted 1 November 2021; published 9 December 2021

New wavelength domains have become accessible for photonic integrated circuits (PICs) with the development of silicon nitride PICs. In particular, the visible and near-infrared wavelength range is of interest for a range of sensing and communication applications. The integration of energy-efficient III-V lasers, such as vertical-cavity surface-emitting lasers (VCSELs), is important for expanding the application portfolio of such PICs. However, most of the demonstrated integration approaches are not easily scalable towards low-cost and large-volume production. In this work, we demonstrate the micro-transfer-printing of bottom-emitting VCSELs on silicon nitride PICs as a path to achieve this. The demonstrated 850 nm lasers show waveguide-coupled powers exceeding 100 μW, with sub-mA lasing thresholds and mW-level power consumption. A single-mode laser with a side-mode suppression ratio over 45 dB and a tuning range of 5 nm is demonstrated. Combining micro-transfer-printing integration with the extended-cavity VCSEL design developed in this work provides the silicon nitride PIC industry with a great tool to integrate energy-efficient VCSELs onto silicon nitride PICs.

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https://doi.org/10.1364/OPTICA.441636

1. INTRODUCTION

Over the past two decades, the field of silicon photonics has steadily been gaining momentum. As for all silicon photonics applications, the lack of integrated sources impedes the roll-out and applicability of photonic integrated circuits (PICs) in a range of applications. Thus far, a lot of effort has gone into integrating edge-emitting III-V devices, such as Fabry–Pérot (FP) lasers, semiconductor optical amplifiers (SOAs), distributed feedback (DFB) lasers, and widely tunable external cavity lasers, onto planar PICs. Demonstrations include chip-level integration of edge-coupled gain chips and lasers [1] and wafer-level integration via bonding [2], flip-chipping [3], micro-optical benches [4], and micro-transfer-printing [5]. With silicon nitride photonics, low-loss propagation and new wavelength bands became accessible for PICs. Consequently, there have been similar efforts in chip-level integration [6], and wafer-level integration of gain chips and laser diodes [7,8]. All these lasers share planar cavities with planar emission and have cavity lengths ranging from a few hundred micrometers to a few millimeters. Associated with the larger cavity length are relatively high threshold currents, in the range of 10–100 mA.

Within the field of data communication, the issue of power consumption, expressed in energy per bit of information sent, is a key figure of merit that is addressed with vertical-cavity surface-emitting lasers (VCSELs), especially for short-reach optical communication. VCSELs have several advantages, such as high-throughput wafer-level testing, an easy interface with optical fibers, and most importantly, a sub-mA lasing threshold and high slope efficiency (SE) that drastically reduces power consumption. Thus far, these properties have not adequately been translated to the world of planar PICs.

Several approaches for VCSEL-to-PIC integration have already been evaluated. Some approaches utilize active alignment, but the additional complexity of the assembly does not make it attractive for larger volumes, in either throughput or cost [9]. To leverage the high-throughput manufacturing capability of silicon photonics, a passive alignment integration approach should be pursued. Given the surface-normal emission property of VCSELs, diffraction grating couplers (GCs) are most often used to couple light to a waveguide (WG) circuit. GCs are preferably illuminated at an angle from the surface normal. This off-normal angle improves the coupling efficiency (CE) and reduces the optical feedback from the grating into the VCSEL cavity, to avoid feedback-induced instability [10]. This off-normal angle can be introduced on the

VCSEL side [11], on the grating side for silicon-based PICs [12], or by using an intermediary prism to refract the light in between the VCSEL and the grating [13]. The angled flip-chip approach currently lacks stability of the processes. The prism-based approach and the micro-electro-mechanical-system (MEMS)-based release of a silicon diffraction grating to form a tilted GC are interesting, but require processes not directly available in a volume silicon nitride photonics technology. This is also true for the use of, e.g., 45° mirrors for end-fire coupling to a WG, as is sometimes used on silicon photonics platforms by exploiting the anisotropic etching of silicon [14].

Other approaches use hybrid cavity designs for VCSEL integration. A III-V half-VCSEL, which consists of a single III-V distributed Bragg refflector (DBR) and III-V active region, is used along with either a high-index-contrast grating (HCG) that acts as both the reflector and the WG-coupling diffraction grating [15], or the combination of a dielectric DBR for reflection and a low-index-contrast intra-cavity diffraction grating (ICG) for coupling the light into the WG [16]. The latter is the most promising approach in terms of component performance, as combining the functionality of coupling and reflection into a single HCG has proven to be difficult, especially using lower-index-contrast SiN_x WG structures. However, the DBR with an intra-cavity grating approach uses non-standard substrates to form the dielectric DBR, which adds significantly to the overall cost and, as such, makes it less viable from a commercial point of view.

The most straightforward approach is flip-chipping an off-the-shelf VCSEL onto a custom diffraction GC [17]. With that approach, an external cavity laser is formed, as part of the light that is not coupled into the PIC can reflect back into the VCSEL cavity, which, when not accounted for, can lead to laser instability [18]. Moreover, the flip-chip approach uses bumps of several micrometer height, many times larger than the emission wavelength of the laser. Next to the lower CE due to the VCSEL beam divergence in the free space path from the VCSEL aperture to the GC, variations in the solder bump height lead to different feedback phases of the external cavity formed between the VCSEL and the diffraction grating, resulting in higher variability of performance.

In this work, we demonstrate the micro-transfer-printing integration of bottom-emitting VCSELs on SiN_x PICs. This approach has been proven for integrating different edge-emitting InP laser diodes on silicon and silicon nitride PICs [8,19]. The technique offers several benefits, including wafer-scale high-throughput integration, improved usage of III-V material, separation of III-V processing from PIC processing, and a well-controlled separation between the PIC and the III-V laser. This work focuses on integrating 850 nm GaAs VCSELs on silicon nitride PICs. This wavelength range is of great interest in optical biosensing due to the low water absorption. It can also leverage the III-V design and fabrication processes from the large market of data communication VCSELs at 850 nm.

Figure 1(a) shows a cross-section schematic of the designed and fabricated device. The layer thicknesses in the cross section are all well controlled, leading to a lower integration variability when scaling to larger volumes. The illustrated VCSEL is a GaAs-based bottom-emitting VCSEL with two III-V semiconductor DBRs and a gain section that is micro-transfer-printed on a SiN_x PIC. The diffraction grating of the PIC provides polarization-dependent and mode-selective feedback, resulting in an extended cavity laser defined by the top oxide thickness of the cladding above

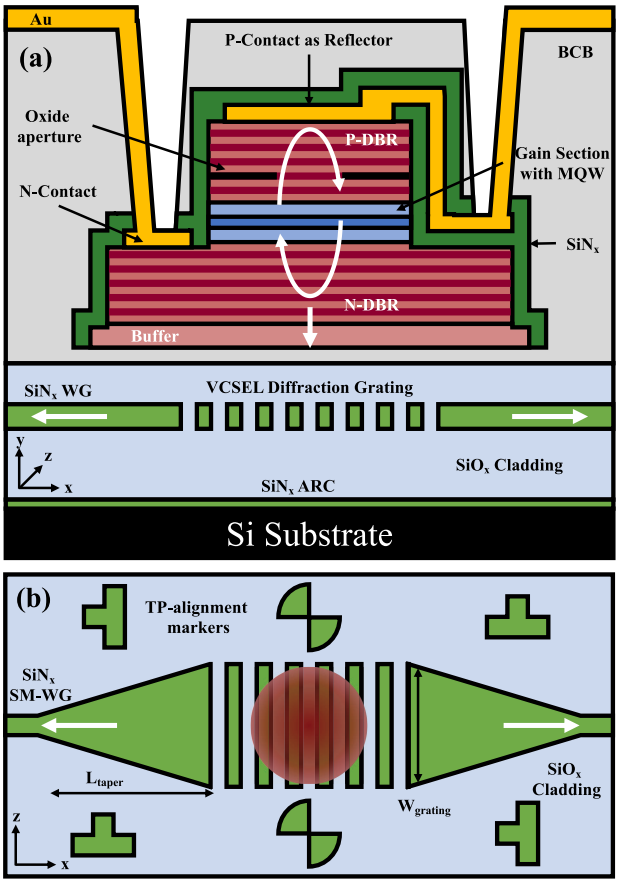

Fig. 1. (a) Cross-section schematic of the micro-transfer-printed vertical-cavity-SiN_x-integrated laser (VCSIL) on a SiN_x bidirectional grating coupler; (b) top-down view of the SiN_x bidirectional diffraction grating coupler design.

the WG. The polarization-selective feedback lowers the TE threshold gain to a value smaller than the TM threshold gain. As a result, the VCSEL prefers to lase in TE polarization and out-couples the light laterally into the SiN_x WG, as shown in Fig. 1(b), to form vertical-cavity silicon-nitride-integrated lasers (VCSILs).

2. DESIGN

The III-V VCSEL is designed for bottom emission and feedback-dependent polarization pinning. Starting from the top, the VCSEL consists of a Ti/Pt/Au (bottom to top order) disk-shaped p-contact that serves as an electrical injection contact and as a top reflector. The top DBR is p-doped and consists of 29 mirror pairs of $Al_{0.12}Ga_{0.88}As/Al_{0.90}Ga_{0.10}As$. At the bottom of the p-DBR, in the layer closest to the separate confinement heterostructue (SCH), a 30 nm $Al_{0.98}Ga_{0.02}As$ layer is included for the formation of an oxide aperture through selective wet oxidation. This laterally confines both the current and the optical mode to the center of the circular VCSEL structure. The active area of the laser is located below the oxidation layer and consists of a $1-\lambda$ thick SCH and a multi-quantum-well (MQW) design containing five 4 nm thick $In_{0.10}Ga_{0.90}As/Al_{0.37}Ga_{0.63}As$ QWs. The bottom DBR is n-doped and composed of 23 mirror pairs of $Al_{0.12}Ga_{0.88}As/Al_{0.90}Ga_{0.10}As$. A Ni/Ge/Au n-contact is positioned a few DBR mirror pair layers below the active area. At the bottom of the n-DBR, a 527 nm

$Al_{0.12}Ga_{0.88}As$ layer (buffer) is present to tune the extended cavity length between the bottom DBR and the diffraction grating. Underneath this layer, 4 nm GaAs serves as an etch stop layer with respect to an $In_{0.49}Ga_{0.51}P$ sacrificial layer, as needed for the micro-transfer-printing process, as will be discussed below. The thin GaAs layer absorbs light at 850 nm, although the impact is minimized because the etch stop layer is placed outside of the III-V cavity, and the standing wave pattern is at a node in the thin GaAs layer.

The VCSEL is designed for bottom emission at a wavelength of 845 nm, with a partial top surface leakage of 5% of the total optical output power for the devices. This allows for a partial characterization of the VCSELs on the native GaAs substrate, prior to the micro-transfer-printing process. Therefore, not all VCSEL devices on the source substrate have a filled circular p-contact. Some test devices are designed with a more standard ring-shaped (annulus) p-contact. The layers of the VCSEL were optimized using a 1D-wave transfer matrix method (TMM) model in MATLAB. Co-design of the WG/GC structure with the VCSEL is necessary, as the reflection from the GC is significant. Since this reflection is polarization dependent, the GC is also used to select the desired polarization state of the VCSEL. TMM calculations use an artificial interface with the same reflectivity properties as the structure beneath the VCSEL. This is obtained from 2D finite-difference-time-domain (FDTD) simulations using Lumerical software.

The diffraction grating on the SiN_x PIC (imec BioPIX300) comprises a 300 nm thick silicon nitride WG, surrounded by SiO_2 cladding [20]. There is an anti-reflection coating (ARC) between the bottom oxide cladding and the substrate, which is part of the standard platform offering. The ARC is a 100 nm thick plasma-enhanced chemical vapor deposited (PECVD) nitride layer, which helps to reduce the feedback from the second external cavity, formed between the VCSEL and the silicon substrate. The ARC suppresses the reflection at this interface from 21.6% down to 3.7%. As a result, the optical feedback from the substrate is less than 10% of the feedback originating from just the diffraction grating. It is therefore why the discussion of the design is focused on the diffraction grating itself and the thickness of the top oxide cladding that lays within the primary extended cavity. As a result, the ARC also reduces the variability in performance between devices, as the influence of the larger variations in the thicker bottom oxide thickness is minimized.

The core of the single-mode (SM) SiN_x WG is 550 nm wide and laterally tapered upwards over 250 μm (L_{taper}), to create a wider ($W_{grating}$) WG/GC to match the mode of the GC to the VCSEL aperture. The top oxide thickness is engineered to achieve resonance in the extended cavity with the diffraction grating. The minimum thickness of the top oxide cladding of the WG needs to exceed 500 nm to avoid a high SiN_x WG leakage loss to the III-V material after coupling into the WG. A representation of the standing wave pattern of the extended cavity VCSEL can be seen in Fig. 2(a). As the VCSEL can operate independently of the diffraction grating, the standing wave pattern is relatively standard. The grating design, optimized in simulations for maximum CE, has a 549 nm pitch, 60% fill factor, and fully etched SiN_x core (300 nm etch depth). At a wavelength of 845 nm, the power reflectivity is 15% for TE polarized light (E-field parallel to the

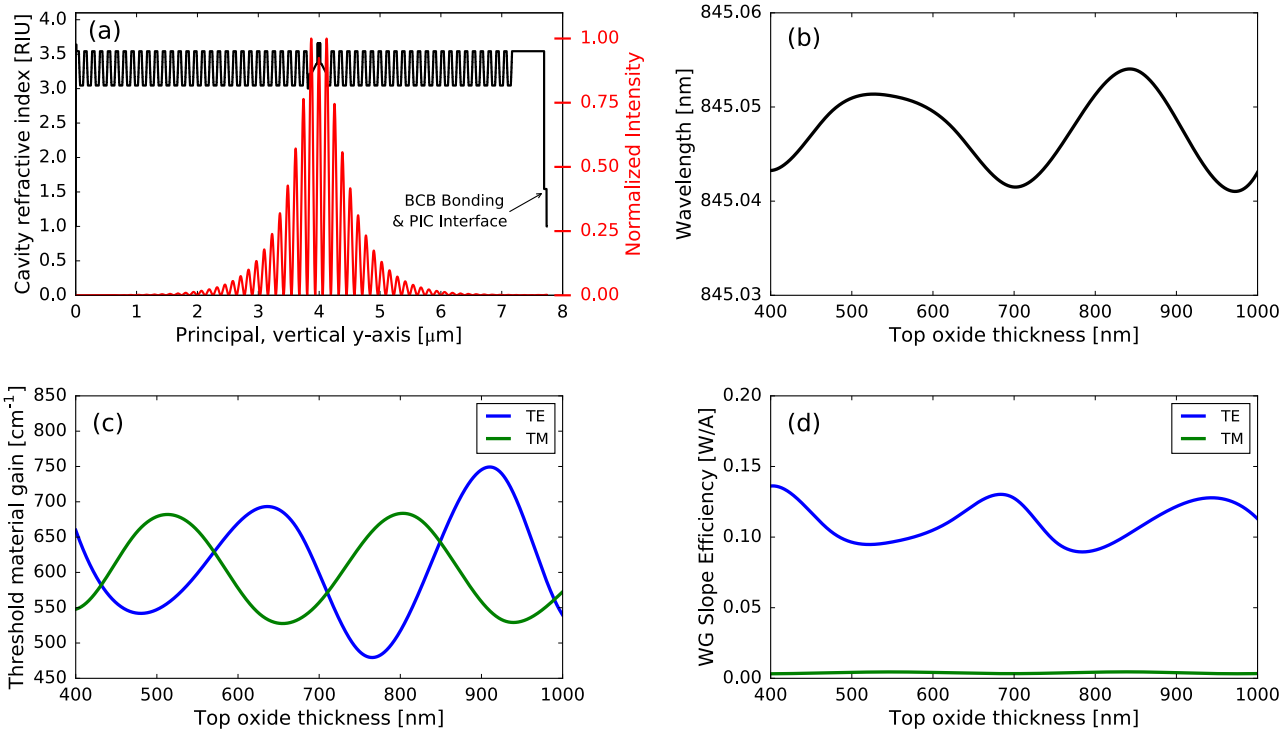

Fig. 2. FDTD-TMM simulated values of the extended cavity design: (a) in red, the standing wave pattern inside the III-V cavity and extending to the PIC diffraction grating with the cavity refractive index design in black; (b) stability of the extended cavity design with the resonance wavelength changing only minimally for different values of the top oxide thickness above the diffraction grating; (c) difference in threshold gain for both polarizations as a function of the top oxide thickness; (d) waveguide-coupled slope efficiency for both polarizations. As the diffraction grating is designed for TE polarization, there is strong suppresion of TM polarization. The simulations are carried out for a fully etched (300 nm etch depth) SiN_x grating with a 549 nm pitch, 60% fill factor, and 7 μm grating length. The simulated mode field diameter of the VCSEL is 5 μm.

grating lines), while it is <5% for TM polarized light (E-field perpendicular to the grating lines). The reflection is calculated based on the field overlap integral as shown in Eq. (1), where $E_{\mathrm{diffr}-z,x}$ is the electric field reflected from the grating when launching a power-normalized Gaussian beam onto the diffraction grating [21], and $\phi_{\mathrm{diffr}-z,x}$ is the parabolic fitted phase front of $E_{\mathrm{diffr}-z,x}$, for the respective TE and TM polarizations along z and x axes. The power-normalized Gaussian beam is defined as $\int G(x)^2 dx = 1$:

$$R_{\mathrm{TE,TM}} = \left| \int E_{\mathrm{diffr}-z,x}(x) e^{j\phi_{\mathrm{diffr}-z,x}(x)} G(x) \mathrm{d}x \right|^2. \quad (1)$$

Varying the top oxide thickness has a negligible effect on the output wavelength, as showcased in Fig. 2(b). The thickness of the cladding was then fine-tuned with the FDTD simulations to minimize the VCSEL threshold for TE polarization, as the grating provides a stronger reflection for this polarization state, as can be seen in Fig. 2(c). At a top oxide thickness of approximately 760 nm, this results in a threshold gain for TM polarization that is more than 150 cm^{-1} higher than for TE polarization, thereby suppressing lasing of TM polarization. The SE for the WG-coupled VCSEL is simulated by combining the CE of the grating from the FDTD simulation, with the vertical slope emission from the transfer matrix model, and shown in Fig. 2(d). The numerically derived values of the extended cavity parameters for TE and TM polarization states can be seen in Table 1, for a VCSEL with an oxide aperture of 5 μm. λ_{res} is cavity resonant wavelength; Q_{cavity} is the cavity quality factor, defined as the ratio between the stored and dissipated energy in the optical cavity, and g_{th} is the gain threshold. The SEs are defined for the relevant substrate configurations, with TOP for the top-emitting test structures on the GaAs source substrate, BOT for the bottom-emitting VCSELs printed on the sapphire substrate, and WG for the WG-coupled VCSILs printed on the WG circuit. The TE single-sided SE in the WG is simulated at 0.09 W/A, derived from the FDTD simulation of the TE single-sided lateral WG CE (WG-CE) for a top oxide thickness of 760 nm.

The micro-transfer-printing technology is validated with an alignment accuracy of up 1 μm, 3 sigma. The influence of this misalignment along the principal grating axis (x axis) is simulated in the FDTD model, as showcased in Fig. 3, to study how the polarization-sensitive feedback might change due to a perpendicular shift with respect to the grating teeth. The misalignment has an impact on the WG-CE, as is to be expected when using diffraction gratings. The total diffraction grating length is designed such that the sum of the CEs of both WGs is maximized. As a result, the maximum coupling of each WG occurs slightly off-center of the diffraction grating. The influence of the misalignment on the threshold gain is derived from the phase and reflectivity response

Table 1. Simulated Properties of VCSELs for Different Substrates, with Top Oxide Thickness of 750 nm for PICs

Properties	GaAs	Sapphire	PIC (TE)	PIC TM
λ_{res} [nm]	845.061	845.060	845.045	845.051
Q_{cavity} [-]	8311.54	12901.06	15762.85	12320.24
g_{th} [1/cm]	934.33	600.96	491.89	629.43
Photon lifetime [ps]	3.729	5.79	7.071	5.527
SE–TOP [W/A]	0.039	—	—	—
SE–BOT [W/A]	—	0.45	—	—
SE–WG [W/A]	—	—	0.0938	0.0037

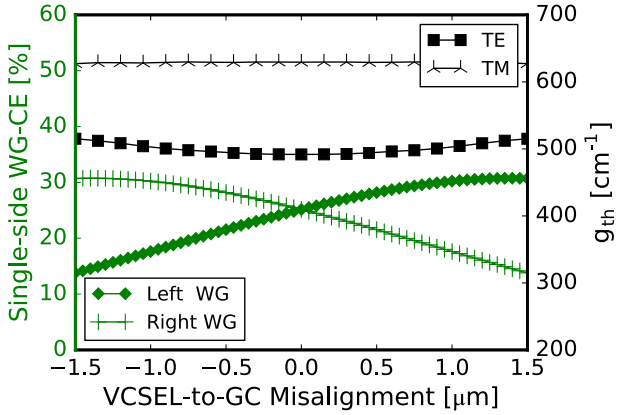

Fig. 3. Influence of the VCSEL-to-GC misalignment along the x axis on both waveguide coupling efficiency (green) and III-V material threshold gain (black), simulated and plotted over a ±1.5 μm range.

of the diffraction grating, as detailed in Eq. (1). The response of either parameter is fairly stable, leading to only minor variations in the TE-threshold gain. To compensate for a z misalignment, the grating width W_{grating} was slightly oversized with respect to the beam width. As a result, the polarization feedback remains stable under a z misalignment. A lateral mismatch between grating mode and VCSEL mode has an approximate 1 dB coupling loss for a z shift corresponding to ∼ one quarter size of the beam width. Over the entire range of expected misalignment values, the VCSEL remains clearly TE polarized.

3. FABRICATION

The process flow for the fabrication can be seen in Fig. 4, showing the advantage of micro-transfer-printing where the complex III-V processing is limited to the III-V substrate. The fabrication starts with a 20 nm Ti, 50 nm Pt, and 100 nm Au (bottom to top order) p-type contact being deposited using electron beam evaporation on top of the VCSEL epitaxial structure. Usually, for top-emitting VCSELs, these contacts are shaped like an annulus to enable top emission. However, for a bottom-emitting design, these p-contacts can be disks, as top emission is not required. The exception is a few test devices for on-source characterization purposes, as shown in Fig. 5(a). In addition to serving as an electrical injection contact and an additional reflector, the disk-shaped contact also protects the top layer of the epitaxial structure. Unintentional etching during the fabrication process could change the VCSEL properties, resulting in a skewed top/bottom emission ratio.

After the contact deposition, the top mesa is formed using a chlorine-based dry etch, followed by the deposition of a SiN_x layer to protect the epitaxial structure from unintentional oxidation. This SiN_x layer is opened up around the mesa edges to enable selective wet oxidation of the $Al_{0.98}Ga_{0.02}As$ layer. The diameter of this oxide-free aperture is controlled by the wet oxidation time. By adjusting the oxidation time correctly, the diameter of the aperture can be set to obtain SM lasing, which happens for an oxide aperture smaller than 5 μm taking the mode-selective feedback from the GC into consideration. With the oxide aperture formed, the 20 nm Ni, 52 nm Ge, and 100 nm Au n-type contacts are deposited, also using electron beam evaporation. The contacts are then annealed. Further, the bottom mesa is formed using another chlorine-based dry etch. The etch is stopped in the middle of the

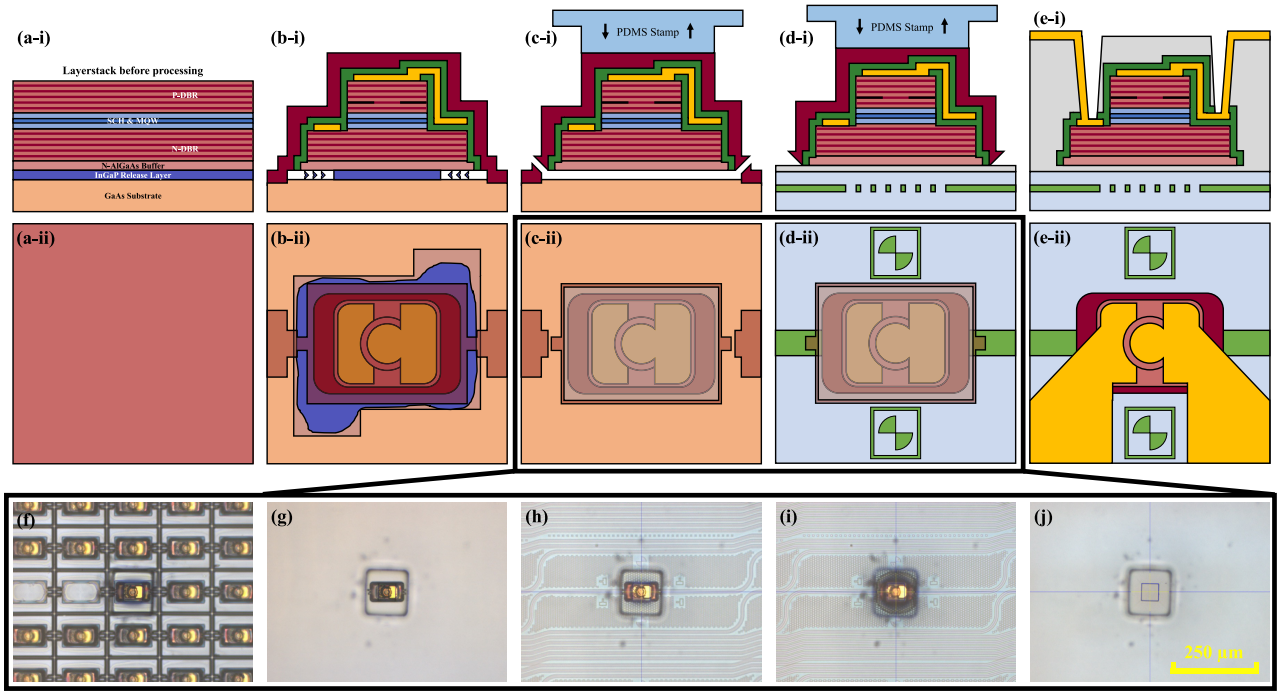

Fig. 4. Fabrication process flow for micro-transfer-printing integration of a bottom-emitting VCSEL. Row (i) shows the cross-section view while row (ii) shows the top-down view. Starting from the epitaxial layerstack in (a), standard VCSEL processing is done to fabricate oxide-aperture-confined VCSELs. Afterwards, the devices are anchored to the substrate with photoresist. An underetch is done in (b) to make them free-standing. With micro-transfer-printing in (c), the devices are picked up with a polydimethylsiloxane (PDMS) stamp and transferred to a new substrate, a SiN_x PIC in (d). Last, a DVS-BCB planarization step is performed, after which the probe pads are connected to the device contact pads in (e). (f)–(j), Microscope images of the micro-transfer-printing process, from pick-up on the GaAs substrate, to transfer, alignment, printing on the PIC, and stamp cleaning.

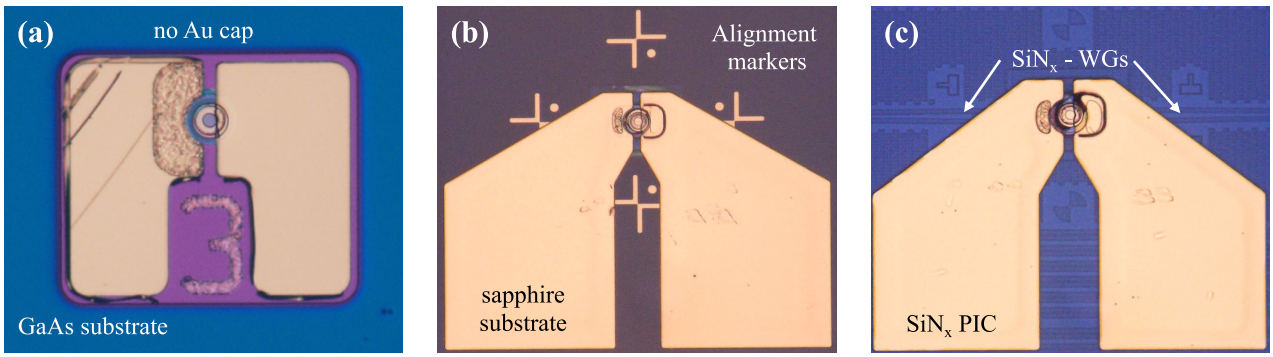

Fig. 5. Microscope images of the different types of devices: (a) top-emitting VCSEL as a test structure on GaAs substrate, (b) bottom-emitting VCSEL on a transparent sapphire substrate, and (c) a bottom-emitting, waveguide-coupled VCSIL on a SiN_x PIC.

527 nm $Al_{0.12}Ga_{0.88}As$ layer, after which a protective and insulating layer of SiN_x is deposited and opened above the contacts for electrical access. At this point, 50 nm Ti and 500 nm Au contact pads are deposited on the test devices to facilitate the electrical access to the on-source test devices with probes. Following this, the SiN_x is then opened up around the VCSEL structure, and the rest of the $Al_{0.12}Ga_{0.88}As$ layer is selectively wet etched using a citric acid and peroxide-based etchant. The release layer is patterned with concentrated HCl, which selectively etches the InGaP release layer with respect to the GaAs substrate and VCSEL buffer layer. The substrate is slightly overetched to securely anchor the photoresist tethers. The 500nm $In_{0.49}Ga_{0.51}P$ layer is removed with another etch using concentrated HCl, thereby suspending the VCSEL structures. The resulting suspended VCSEL structures measure 50 µm × 90 µm.

Micro-transfer printing is performed with a X-Celeprint laboratory-scale printer (µTP-100), with a polydimethylsiloxane (PDMS) stamp picking up either one or multiple devices at once, depending on the layout of the stamp. The adhesion between the photoresist encapsulation and the PDMS stamp is rate dependent, meaning a fast pick-up and slow printing allow the devices to selectively stick to the stamp or to the target substrate [22]. As the pick-up is done in a swift motion, the devices stick to the stamp and are transferred to the target substrate. The target substrate is either a transparent sapphire substrate for characterizing the bottom output power of the VCSELs, or a silicon nitride PIC. On the target substrate, diluted divinyl-siloxane-benzocyclobutene

(DVS-BCB)-mesitylene (1:8) is spin-coated as a bonding layer with a thickness of ∼40 nm. After printing, the encapsulation is removed, the bonding layer is cured, and the target substrate is planarized with a thick DVS-BCB layer. After curing, the DVS-BCB layer is thinned down with a SF_6-based reactive ion etching (RIE). Slanted openings are made in the DVS-BCB in a second RIE step, to reach the device contacts and remove the SiN_x protection layer on the device. In a final step, additional metal (10 nm Ti/300 nm Au) is deposited on the device contacts via sputtering, to form the larger probe contacts. The resulting devices are shown in Figs. 5(b) and 5(c) for the sapphire substrate and the SiN_x PIC.

4. MEASUREMENT RESULTS

A. Surface-Emitting VCSELs

Integrating the VCSELs on top of a diffraction grating can alter the device properties, as discussed in Section 2. For this reason, the VCSEL-component parameters are extracted from top-surface-emitting VCSELs on the source substrate and bottom-surface-emitting VCSELs that are printed on the transparent sapphire substrate. The test VCSELs on the source substrate are measured after the deposition of the additional metal to facilitate probe access to the devices. Light–current–voltage (LIV) measurements and optical spectra are collected from the top with a multi-mode fiber. LIV measurements are also performed on bottom-emitting VCSELs. The bottom-emission of the VCSELs required the use of a large-area photodetector (Hamamatsu S2281) to collect the light and excluded spectral measurements of the transfer-printed VCSELs onto the sapphire substrate.

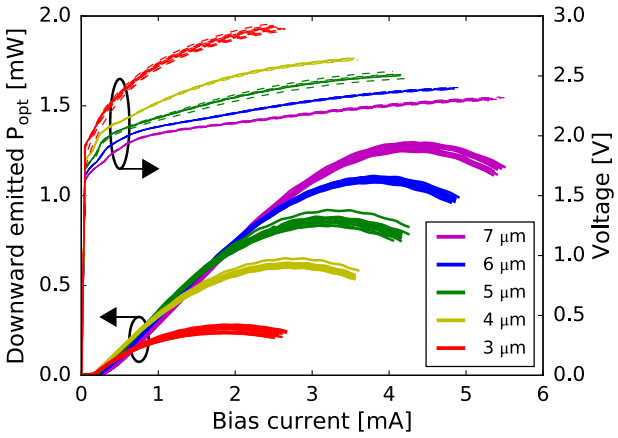

Fig. 6. Optical output power (full line) and voltage (dashed line) of the downward-emitting VCSELs printed on the transparent sapphire substrate. The values in the legend symbolize the oxide aperture diameter.

The LIV curves for each of the aperture sizes of the VCSELs printed on the sapphire substrate are plotted in Fig. 6. The current at thermal rollover occurs between 1.9 and 4 mA, depending on the aperture size. From the light–current (LI) curves, the lasing threshold and SEs are extracted. The results for both types of surface-emitting devices are summarized in Table 2. The SEs were in very good agreement with the simulated values of Table 1, and the low lasing thresholds result in a low-power-consumption integrated laser. The current–voltage (IV) curves showed that the differential resistance Ω_{diff} varied between 40 and 140Ω over the aperture size range. The spectral measurements on top-surface-emitting VCSELs on the GaAs source substrate were limited in sample size and thus do not accurately reflect the per device component, as some uncertainty remained on the size of the oxide aperture of those on-source test devices. The measurements showed that in general the devices with 4 μm apertures were lasing in SM with side mode suppression ratio (SMSR) >20 dB.

B. Waveguide-Coupled VCSILs

The WG-coupled VCSELs were transfer-printed on top of an imec BioPIX300 silicon nitride PIC, to form VCSILs. The bidirectional diffraction grating couples the light laterally into the 300 nm thick, 6 μm wide WG layer, which is then tapered down to a 550 nm wide SM WG and routed towards a fiber GC. A variation of grating parameters with respect to the simulated values in Section 2 were included to offset any variation in fabrication of these gratings (thickness and fill factor). While the grating parameters of the presented devices are slightly different, they each target the same operating regime. The light is collected with a SM fiber and guided to a power meter or optical spectrum analyzer (Agilent OSA 86140). Reference fiber grating test structures indicated an average insertion loss of −8.5 dB per fiber grating, with a fab-confirmed propagation loss of −0.45 dB/cm for the WGs.

Figure 7 shows the WG-coupled power to both left and right WGs, for a ∼4.5 μm aperture VCSIL on a 558 nm pitch SiN_x grating with a 72.5% fill factor and a 760 nm SiO_x top oxide cladding thickness, verified through a focused ion beam (FIB) cross section. FP fringes can be observed on the LI curves. This is related to a parasitic reflection of the fiber GC. The distance between the fiber GC and VCSEL was different on both sides from the VCSEL, resulting in a different periodicity for each side, with

Table 2. Overview of Lasing Threshold, I_{th}, Slope Efficiency, SE, and Optical Output Power, P_{opt}, of Top-Emitting VCSELs on GaAs Substrate and Bottom-Emitting VCSELs on Transparent Sapphire Substrate[a]

		VCSEL Apertures Measured				
Parameter	**Substrate**	**3 μm**	**4 μm**	**5 μm**	**6 μm**	**7 μm**
I th[mA]	GaAs	0.12 ± 0.02	0.14 ± 0.03	0.19 ± 0.03	0.31 ± 0.03	0.38 ± 0.11
	Sapphire	0.14 ± 0.00	0.16 ± 0.02	0.20 ± 0.01	0.27 ± 0.01	0.34 ± 0.00
SE [W/A]	GaAs	0.01 ± 0.00	0.03 ± 0.00	0.03 ± 0.00	0.04 ± 0.00	0.04 ± 0.00
	Sapphire	0.31 ± 0.01	0.42 ± 0.01	0.42 ± 0.01	0.44 ± 0.01	0.43 ± 0.00
P_{opt} [mW]	GaAs	0.02 ± 0.01	0.07 ± 0.01	0.12 ± 0.01	0.16 ± 0.01	0.21 ± 0.01
	Sapphire	0.26 ± 0.02	0.62 ± 0.02	0.87 ± 0.03	1.09 ± 0.01	1.27 ± 0.02
SMSR*[dB]	GaAs	37.7 ± 2.3	23.3 ± 10.1	6.7 ± 3.3	—	—

[a]The measurements of P_{opt} are shown in Fig. 6. On average, more than 10 devices per aperture are tested on both GaAs and sapphire substrates. SMSR is measured only on the GaAs substrate, due to setup constraints. * indicates a reduced sample size of those spectral measurements.

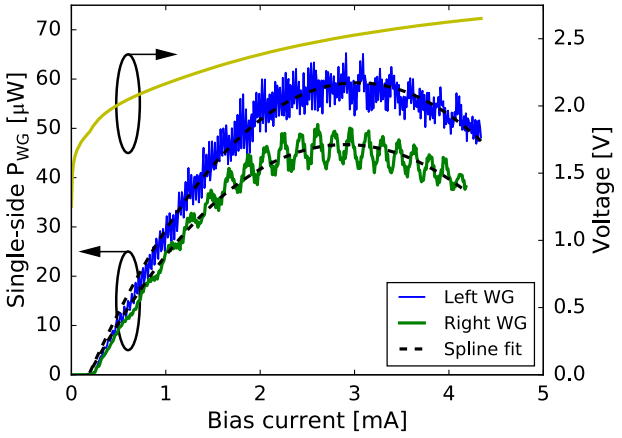

Fig. 7. Waveguide-coupled power of the VCSIL for both left and right waveguides. Ripples in the spectrum are associated with the on-chip Fabry–Pérot cavity between the VCSEL grating coupler and the fiber grating coupler.

even a superposition of the respective cavity effects leading to a more rapid oscillation of the left WG power curve. With the use of reflectionless fiber GCs, this effect can be mitigated.

The net WG-coupled output power exceeds 50 μW for the left WG and combines to over a 100 μW for the two WGs' power values added together. A slight difference in maximum output power between the WGs is attributed to misalignment of the printing process, as illustrated in Fig. 3. While this power level is not particularly high, it more than suffices the requirements for driving a refractive index sensor for optical sensing. The proposed VCSEL can drive well over 100 refractive index sensors in parallel, in combination with high-responsivity, low dark current photodetectors [23]. The power conversion efficiency (PCE), defined as the ratio of the optical output power to the electrical input power, is for this particular VCSEL 2.4% in total, with 1.3% and 1.1% for the left and right WGs, respectively. The measured SMSR of this device remained above 29 dB over the bias range. The WG-coupled output power of the same device in Fig. 7 is plotted for varying ambient (substrate) temperatures in Fig. 8. Between 25°C and 85°C, the VCSIL output power drops with ∼50%. Two interesting temperature related parameters are T_0, the ambient temperature at which the lasing threshold is minimized, and T_1, a parameter representing the change in SE per change in degree of

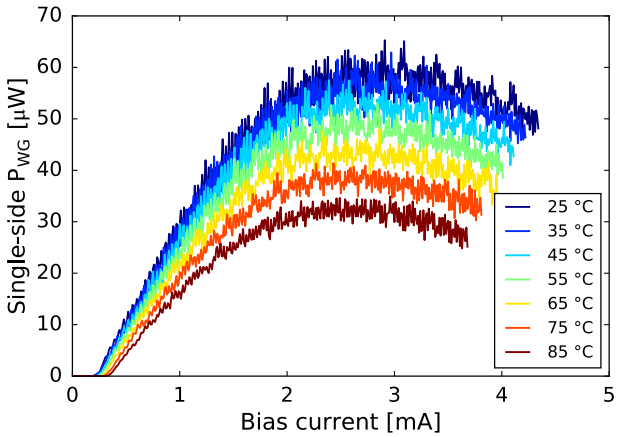

Fig. 8. Waveguide-coupled output power as a function of substrate temperature, demonstrating a large temperature operation range of the VCSIL.

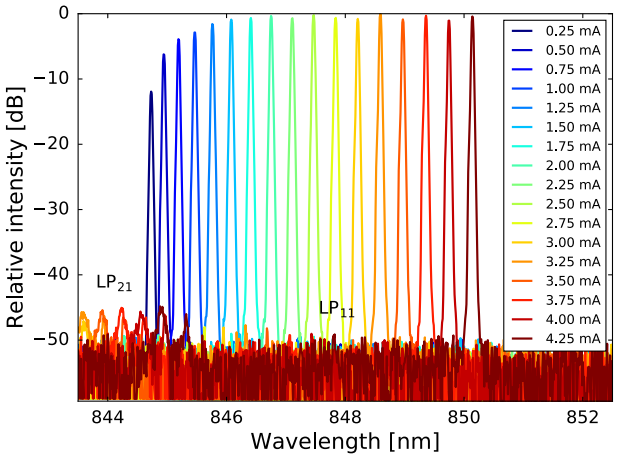

Fig. 9. Output spectrum of a waveguide-coupled VCSIL. The current-induced self-heating results in a wavelength shift close to 5 nm. Mode-selective feedback helps to suppress the first higher-order LP_{11} mode with respect to the LP_{21} mode.

ambient temperature. T_0 and T_1 have been extracted and found to be approximately −0.5°C and −0.6%/°C, respectively, for the device shown in Fig. 8.

The purpose of these WG-integrated VCSILs is to form a narrowband tunable laser. The effective cavity length of the VCSIL changes due to current-induced self-heating [24], which is approximately the same for all devices. As a result, this means that the tuning range of ∼5 nm is the same for all devices. Figure 9 shows the tuning capabilities in the optical spectra of another VCSIL. This specific VCSIL has a high SMSR and shows mode-selective feedback occurring from the grating. The device itself has a ∼3.5 μm oxide aperture, printed on top of a diffraction grating with a 554 nm pitch and 50% fill factor, and the same top oxide thickness as before. The VCSIL couples a net 32 μW of optical power into the WG and remains nicely SM across the entire current range with a SMSR of over 45 dB. Moreover, it can be seen that there is a strong suppression of the first higher-order mode LP_{11}, centered at a wavelength approximately 2 nm below the center wavelength $\lambda_{LP_{01}}$. In this instance, that mode actually falls below the measured noise floor. The most dominant higher-order mode, LP_{21}, can be found at approximately 4 nm below $\lambda_{LP_{01}}$. This is attributed to a mode-selective feedback mechanism of the grating.

5. CONCLUSION AND OUTLOOK

To conclude, with micro-transfer-printing, it is possible to enhance a silicon nitride PIC platform with active components. In this work, we have demonstrated the integration of a vertical cavity laser on a SiN_x PIC using a bidirectional diffraction GC. The micro-transfer-printing allows a more controlled extended cavity design in contrast to stud-bump flip-chipping approaches, while allowing for a more straightforward implementation than wafer bonding, as no III-V processing is required on the PIC wafer. The design of the VCSEL allows both upward emission for process control monitoring and downward emission for WG coupling. The downward-coupled optical power is about 0.6 mW for a 4 μm aperture sized VCSEL, and the combined WG-coupled power is currently over 100 μW for a device with similar aperture size. The demonstrated SM, low-power-consumption, low-cost VCSIL

is ideally suited, e.g., to interrogate PIC-based refractive index sensors for wearable applications.

This work demonstrates the potential of micro-transfer-printed extended-cavity WG-coupled VCSILs as power-efficient SM laser sources on silicon nitride PICs. On silicon nitride platforms, this approach can be applied over a wide wavelength range, down to the visible where blue VCSELs have become a topic of great interest. There are still various possible optimizations on the design of the system, i.e., to boost the WG-CE (including the coupling to a single output WG), to mitigate early thermal rollover and to increase the polarization selectivity of the feedback by introducing high-index materials to form the GC and/or bottom external cavity mirrors.

This paper focused on the integration of low-power-consumption SM VCSELs for optical sensing. With minor changes to the process flow, the capacitance of the VCSEL can be reduced, leading to low-power-consumption transfer-print-compatible VCSELs with larger modulation bandwidths. This will open up new opportunities for power-efficient data-communication applications, especially when a VCSEL diffraction grating design with higher waveguide coupling efficiency is used.

Funding. Horizon 2020 Framework Programme (PIX4LIFE, 688519).

Acknowledgment. The authors thank Emanuel Haglund and Erik Haglund for technical support in VCSEL fabrication and Liesbet Van Landschoot for support with FIB cross-section analysis. This work was performed in part at Myfab Chalmers.

Disclosures. The authors declare no conflicts of interest.

Data Availability. Data underlying the results presented in this paper are available from the authors upon reasonable request.

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91.161.237.252 (a 2022-08-20 04:16:26)