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Analytical Optimal Load Calculation of RF Energy Rectifiers Based on a Simplified Rectifying Model †

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Abstract: Wireless power transfer (WPT) is an essential enabler for novel sensor networks such as the wireless powered communication network (WPCN). The efficiency of an energy rectifier is dependent on both input power and loading condition. In this work, to maximize the rectifier efficiency, we present a low-complexity numerical method based on an analytical rectifier model to calculate the optimal load for different rectifier topologies, including half-wave and voltage-multipliers, without needing time-consuming simulations. The method is based on a simplified analytical rectifier model based on the diode equivalent circuit including parasitic parameters. Furthermore, by using Lambert-W function and the perturbation method, closed-form solutions are given for low-input power cases. The method is validated by means of both simulations and measurements. Extensive transient simulation results using different diodes (Skyworks SMS7630 and Avago HSMS285x) and frequency bands (400 MHz, 900 MHz, and 2.4 GHz) are provided for validation of the method. A 400 MHz 1- and 2-stage voltage multiplier are designed and fabricated, and measurements are conducted. Different input signals are used when validating the proposed methods, including the single sinewave signal and the multisine signal. The proposed numerical method shows excellent accuracy with both signal types, as long as the output voltage ripple is sufficiently low.

Keywords: WPT; RF; rectifier; load resistance; analytical; closed-form; half wave; voltage multiplier

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1. Introduction

Wireless power transfer (WPT) is an emerging technology that removes the traditional charging cables. Due to its convenience, WPT can be found or foreseen in many applications such as electric vehicles, consumer electronics, and new communication networks [1,2]. Specifically, far-field WPT based on RF signals can deliver wireless power over a long distance up to kilometers, which enables new communication and sensing networks in the IoT domain such as wirelessly powered communication network (WPCN). These networks consist of low-power sensor nodes whose power is provided by either dedicated RF sources or ambient RF energy, which prolongs the sensors' lifetime and reduces the maintenance cost [3].

The receiving side of an RF WPT system is called an energy rectifier. The rectifier converts the RF signal into a DC voltage that either directly powers electronics or is stored in storage units such as batteries or super-capacitors. It often consists of an antenna that captures the wireless signal; a matching and rectifying network for RF-to-DC conversion; and a power management unit (PMU), which is the rectifier's load. The power conversion efficiency (PCE) of a rectifier has been shown to depend on both received RF power and its load; thus, the optimal load for a rectifier needs to be understood [4]. Additionally,

novel excitation waveforms such as multisine waveform featuring high peak-to-average-power ratio (PAPR) and multiple frequency components [5] have been proposed to boost the rectification efficiency. To analyze the optimal load with general excitation, transient simulations are often conducted [6], which are time-consuming and computationally intensive. Harmonic balance (HB) is another option, but its complexity poorly scales with the number of frequency components in the excitation waveform so that it soon becomes impractical [7].

Instead of numerical solvers, many efforts were put into the analytical modeling of rectification. The works [8–10] used the time-domain method to analytically analyze the shunt-diode rectifier. Afterwards, ref [11] the model was extended with class-f harmonic termination. In [12–14], Bessel functions are used to separate DC component and the first harmonic of the diode voltage and the optimal load using the developed model is calculated. A limitation to the aforementioned works is that they all assume the applied excitation to be a sine wave. Works in [15,16] extensively analyzed the incurred losses in the complete rectification chain and pointed out the optimal load resistance for the overall efficiency in the low input power range is equal to the diode junction resistance and series resistance combined. The junction resistance, however, depends on the junction bias voltage, which in turn depends on the load; thus, additional steps are needed to calculate or measure this quantity.

There have also been works focusing on developing analytical rectification models for general multisine signals. In [17], a simplified analytical model was developed to mathematically prove the efficiency gain of the multisine excitation. Later, this model was used in [18,19] to optimize the transmission waveform with frequency-selective fading channels because of the tractability of this rectifier model and its ability to capture the non-linearity of the rectifier circuitry. For the same reason, this model was also used in system performance analysis and optimization of WPCNs and shows superior accuracy to the conventional linear rectifier model in [20–23]. Despite the successful applications of this model, the key assumptions in [17,18] when developing it are the ideal diode and the half-wave rectifier topology.

In our previous work [24], the model with diode parasitics in the simplest half-wave rectifier was discussed; then, the model was extended for the voltage-doubler. We also showed the low-complexity method to derive the optimal load. The method works with general multisine input signals, provided that the output voltage ripple is small enough. In the current work, we further extend the model to generic N-stage voltage-multipliers. More extensive transient simulations are conducted to validate the result. Two different Schottky diodes are considered in the simulation, and three different frequency bands: 400 MHz, 900 MHz, and 2.4 GHz, which are simulated as well to investigate the impact of frequency. Finally, rectifier prototypes are designed and fabricated and a measurement campaign is conducted to provide experimental data to further support the results.

The paper is organized as follows: Section 2 introduces the simplified analytical rectifier model for both half-wave and N-stage voltage multiplier with a realistic diode equivalent model; Section 3 describes the calculation of the optimal load and its closed-form asymptotic solutions; and numerical and experimental validations are discussed in Section 4, including the simulation setup, PCB design considerations, measurement setup, results, interpretation, and discussion. Finally, Section 5 summarizes the paper and discusses the implications of applications.

2. Analytical Rectification Model

In this section, we will summarize the rectification model for the half-wave topology and analyze the effects of diode parasitic parameters. Then, we will extend the model to a generic N-stage voltage multiplier.

2.1. Half-Wave Rectification Model

The schematic of a half-wave rectifier is shown in Figure 1a. The diode is modeled by the equivalent circuit shown in Figure 2, where there is the ideal diode junction D_j, junction capacitance C_j, series resistance R_S, parallel capacitance C_P, and series inductance L_S. Assume a multisine input voltage to the rectifier circuit being:

$$v_{in}(t) = \sum_{n=0}^{N_f-1} V_A \cos(2\pi f_n t + \phi_n) \tag{1}$$

where N_f is the number of sub-carriers or tones, V_A is the amplitude of each tone, f_n and ϕ_n are the frequency and phase of the n-th tone, respectively. The tones are assumed to follow a uniform frequency grid, such that $f_n = f_0 + n\Delta_f$, with Δ_f being the frequency separation. As a result, $v_{in}(t)$ is a periodic signal with period $T = 1/\Delta_f$ when $N_f > 1$. The CW signal can be viewed as a special case with $N_f = 1$ and a period of $T = 1/f_0$.

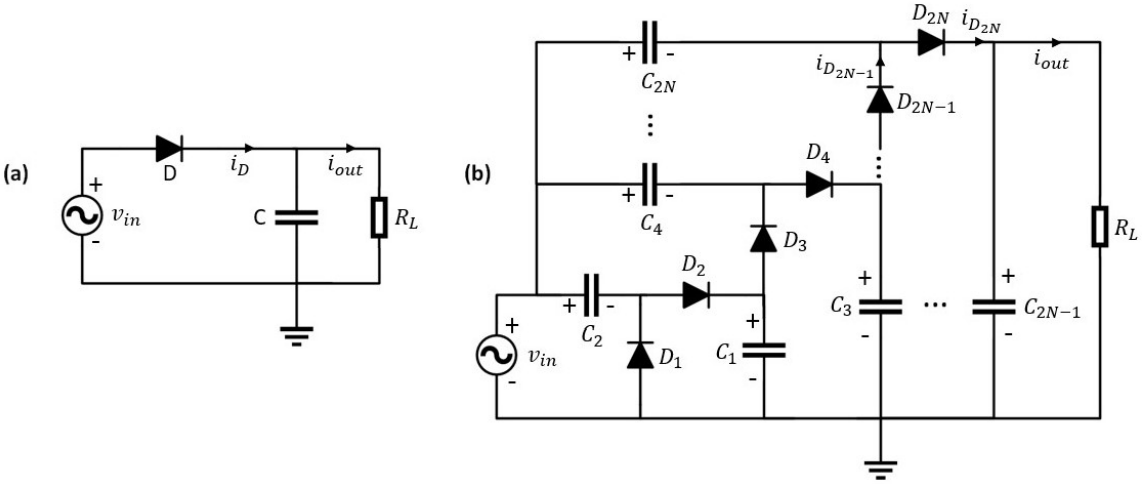

Figure 1. Schematic of (**a**) a half-wave rectifier and (**b**) an N-stage voltage-multiplier.

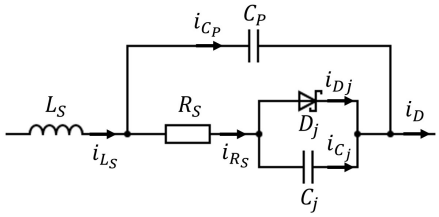

Figure 2. Diode equivalent circuit [25].

According to the Kirchhoff's voltage and current law, and Figures 1a and 2, we have the following relationships:

$$C\frac{dv_{out}(t)}{dt} + i_{out}(t) = C_P\frac{dv_{C_P}(t)}{dt} + i_{D_j}(t) + C_j\frac{dv_{C_j}(t)}{dt} \tag{2}$$

$$i_{D_j}(t) = i_s(e^{\alpha v_{D_j}(t)} - 1) \tag{3}$$

$$v_{D_j}(t) = v_{in}(t) - v_{L_S}(t) - v_{R_S}(t) - v_{out}(t) \tag{4}$$

$$i_{R_S}(t) = i_D(t) - C_P\frac{dv_{C_P}(t)}{dt} \tag{5}$$

where i_s is the diode saturation current, and $\alpha = 1/(nv_t)$ with n and v_t being ideality factor and thermal voltage, respectively. Equation (3) is the Shockley equation of the diode

junction. Because we are interested in the DC output voltage rather than its transient, we average both sides of Equation (2) over a signal period after the system reaches steady state:

$$i_{dc} = \mathcal{E}\{i_{D_j}(t)\} = \frac{i_s}{T}\int_0^T e^{\alpha v_{D_j}(t)}dt - i_s \tag{6}$$

where i_{dc} is the DC component of output current i_{out}, $\mathcal{E}\{.\}$ denotes time averaging, and the juntion current $i_{D_j}(t)$ is substituted by Equation (3). Note that during the time averaging, the current terms related to capacitors vanishe. This is because in the steady state, the amount of electronic charges on a capacitor remains the same in the beginning and the end of a period. As a result, the average current has to be zero.

Next, we assume the output capacitor C in Figure 1a is sufficiently large, such that the output voltage ripple is negligible. Hence, the output voltage over the load is effectively a DC signal, such that we can write $i_{out}(t) \approx i_{dc}$ and $v_{out}(t) \approx i_{dc}R_L$. This is a reasonable assumption since a steady state voltage source is essential for the proper functionality of the circuitry behind the rectifier. Following this assumption, we can further approximate the current through diode $i_D(t) = C\frac{dv_{out}(t)}{dt} + i_{out}(t) \approx i_{dc}$. Substituting these approximations in Equation (4), we obtain

$$v_{D_j}(t) \approx v_{in}(t) - i_{R_S}(t)R_S - i_{dc}R_L \tag{7}$$

The series inductance term is dropped because L_S is typically very small so naturally $v_{L_S}(t) = L_s\frac{di_D(t)}{dt} \approx 0$. Similarly, the parallel capacitance term in Equation (5) is also dropped due to small C_P value. As a result, Equation (5) can be rewritten by $i_{R_S}(t) \approx i_{dc}$, and Equation (7) is now:

$$v_{D_j}(t) \approx v_{in}(t) - i_{dc}(R_S + R_L) \tag{8}$$

Substitute it back to Equation (6):

$$i_{dc} = e^{-\alpha i_{dc}(R_S+R_L)}\frac{i_s}{T}\int_0^T e^{\alpha v_{in}(t)}dt - i_s \tag{9}$$

Note now that i_{dc} is still on both sides of the equation. Move i_s to the left hand side and multiply $\alpha R_h e^{\alpha(i_{dc}+i_s)R_h}$ to both sides:

$$\alpha(i_{dc} + i_s)R_h e^{\alpha(i_{dc}+i_s)R_h} = \alpha R_h e^{\alpha i_s R_h}\frac{i_s}{T}\int_0^T e^{\alpha v_{in}(t)}dt \tag{10}$$

where $R_h = R_S + R_L$. Equation (10) can be solved for i_{dc} by using the principle branch of the Lambert W-function [26]:

$$i_{dc}(v_{in}, R_L) = -i_s + \frac{1}{\alpha R_h}W\left(\alpha R_h(i_s + z_{dc})e^{\alpha i_s R_h}\right) \tag{11}$$

where $z_{dc} = \frac{i_s}{T}\int_0^T e^{\alpha v_{in}(t)}dt - i_s$, which is a monotonic function with the amplitude of input voltage, and $W(x)$ is the Lambert W-function whose value is the solution of w to the equation $we^w = x$. The Lambert W-function does not have an explicit formula but can be evaluated by simple numerical methods described in [26].

2.2. N-Stage Voltage-Multiplier Rectification Model

In this section, we will generalize the analytical half-wave rectification model developed in the previous section to N-stage voltage-multiplier. Figure 1b shows the schematic of a N-stage voltage-multiplier. A voltage-multiplier is often used to boost the output DC voltage by cascading voltage-doublers. The capacitors C_n with even n are used to provide DC offset to each stage so the output voltage is stepped up gradually. Assume all diodes used in Figure 1b are the same. According to the Kirchhoff's current law, for the upper diode of the last stage D_{2N}:

$$C_{2N-1}\frac{dv_{out}(t)}{dt} + i_{out}(t) = C_{2N}\frac{dv_{C_{2N}}(t)}{dt} + C_{P_{2N}}\frac{dv_{C_{P(2N)}}(t)}{dt} + i_{D_{j(2N)}}(t) + C_{j(2N)}\frac{dv_{C_{j(2N)}}(t)}{dt} \tag{12}$$

where $C_{P(2N)}$ and $D_{j(2N)}$ denote the parallel capacitance and junction of the $2N$-th diode. By time-averaging the above equation in the steady state like we did with Equation (2), we get:

$$i_{dc} = \mathcal{E}\{i_{D_{j(2N)}}(t)\} = \frac{i_s}{T}\int_0^T e^{\alpha v_{D_{j(2N)}}(t)}dt - i_s \tag{13}$$

According to the Kirchhoff's voltage law for the diode D_{2N}, the junction voltage is:

$$v_{D_{j(2N)}}(t) = v_{in}(t) - v_{C_{2N}}(t) - v_{L_{S(2N)}}(t) - v_{R_{S(2N)}}(t) - v_{out}(t) \tag{14}$$

where $L_{S(2N)}$ and $R_{S(2N)}$ are series inductance and series resistance of the $2N$-th diode. The same treatment with the series inductance and resistance can be done as when analyzing the half-wave rectifier, to approximate $v_{L_{S(2N)}} \approx 0$ and $v_{R_{S(2N)}} \approx i_{dc}R_S$. To ensure a small output ripple, all capacitors in a voltage-multiplier need to be large enough so the time constant is larger than the signal period. This means the capacitors can be considered short-circuits at high frequency so that their voltage drop has only DC component [27]. At DC, the capacitors are open circuit and the input is shorted because the input voltage does not have DC component. As a result, the voltage drop across C_{2N} is:

$$v_{C_{2N}}(t) = -\frac{2N-1}{2N}i_{dc}R_L \tag{15}$$

which equals to the voltage drop across the first $2N-1$ cascaded diodes. Using it in Equations (13) and (14), we get:

$$i_{dc} = e^{\alpha i_{dc}(R_S + \frac{R_L}{2N})}\frac{i_s}{T}\int_0^T e^{\alpha v_{in}(t)}dt - i_s \tag{16}$$

Again, solve it for i_{dc} using the principle branch of the Lambert W-function:

$$i_{dc}(v_{in}, R_L) = -i_s + \frac{1}{\alpha R}W\left(\alpha R(i_s + z_{dc})e^{\alpha i_s R}\right) \tag{17}$$

where $R = R_S + \frac{R_L}{2N}$ and N is the number of stages of a voltage-multiplier. Given the similarity between Equation (11) for half-wave and Equation (17) for voltage-multiplier, the half-wave model can be viewed as a special case of the multiplier model with number of stages $N = 0.5$.

3. Calculation of Optimal Load Resistance

3.1. Problem Formulation

We have so far developed the output DC current in the last chapter. By definition, the output DC power P_{dc} is:

$$P_{dc} = i_{dc}^2 R_L \tag{18}$$

The optimal load that maximizes P_{dc} can be found by numerically evaluating Equation (18) based on Equation (17) with a scanned R_L. This solution is called numerical solution of the analytical model.

To find the closed-form solution to the optimal load, the first derivative of P_{dc} needs to be formulated. We first write the i_{dc}'s first derivative with respect to the load using (17):

$$\frac{\partial i_{dc}}{\partial R_L} = -\frac{1}{2\alpha N R^2}W(E) + \frac{1}{\alpha R}\frac{\partial W(E)}{\partial R_L} \tag{19}$$

where $E = \alpha R(i_s + z_{dc})e^{\alpha i_s R}$. To simplify the notation, we omit the dependency of both i_{dc} and P_{dc} on v_{in} and R_L in equations from here on. The derivative of P_{dc} with respect to the load resistance:

$$\frac{\partial P_{dc}}{\partial R_L} = i_{dc}(i_{dc} + 2R_L\frac{\partial i_{dc}}{\partial R_L}) \tag{20}$$

Use Equations (17) and (19) in (20) we further have:

$$\frac{\partial P_{dc}}{\partial R_L} = i_{dc}\Big(- i_s + \frac{NR - R_L}{\alpha NR^2}W(E) + \frac{2R_L}{\alpha R}\frac{\partial W(E)}{\partial R_L}\Big) \triangleq i_{dc}I_0 \tag{21}$$

Since i_{dc} is by definition a non-negative number, solving for $I_0 = 0$ is equivalent to solving $\frac{\partial P_{dc}}{\partial R_L} = 0$. However, finding the closed-form solution can be a challenge due to the lack of explicit formula of the W-function.

3.2. Closed-Form Approximations for Low Input Power

The W-function can be approximated in closed-form under some assumptions. By definition, the value of the W-function in Equation (21) is the solution of the equation:

$$W(E)e^{W(E)} = \alpha i_s R e^{\alpha i_s R} + \alpha z_{dc} R e^{\alpha i_s R} \tag{22}$$

An easy solution would be obtained if the second term on the right hand side was absent, which is $W(E) = \alpha i_s R$. This situation is similar to solving a nonlinear ordinary differential equation (ODE). When the ODE is constructed in a way that there is a simple part added by a complex nonlinear term, often the perturbation method can be applied if the nonlinear term is small [28]. Here, we apply the perturbation method to solve Equation (22) under the condition that z_{dc} is small compared with i_s. Because z_{dc} is a monotonic function of input voltage amplitude, the condition is equivalent to a small input power.

The exact solution $W(E)$ is obviously a function of z_{dc}; thus, a power series about z_{dc} exists that approximates $W(E)$:

$$W(E) \approx W_a^{(K)}(E) = \sum_{k=0}^{K} z_{dc}^k W_k \tag{23}$$

where $W_a^{(K)}(E)$ is the approximation to $W(E)$ with order K and the coefficients W_k, $\forall k = 0, 1, \ldots, K$ are the generating solutions. Naturally, the smaller z_{dc} is, the less order K is needed before the approximation converges. After substituting (23) into (22) and taking logarithm on both sides, we obtain

$$\ln\big(\sum_{k=0}^{K} z_{dc}^k W_k\big) + \sum_{k=0}^{K} z_{dc}^k W_k = \ln\big(\alpha(i_s + z_{dc})R\big) + \alpha i_s R \tag{24}$$

Taking the derivative of this equation from 0 to K times and equating z_{dc} to zero each time gives us $K + 1$ generating equations. We list them with $K = 2$ here:

$$\ln(W_0) + W_0 = \ln(\alpha i_s R) + \alpha i_s R \tag{25}$$

$$\frac{1}{W_0}W_1 + W_1 = \frac{1}{i_s} \tag{26}$$

$$-\Big(\frac{W_1}{W_0}\Big)^2 + 2\frac{W_2}{W_0} + 2W_2 = -\frac{1}{i_s^2} \tag{27}$$

Then, it is straightforward to get the generating solutions:

$$W_0 = \alpha i_s R, W_1 = \frac{\alpha R}{1+\alpha i_s R}, W_2 = -\frac{\alpha^2 R^2(2+\alpha i_s R)}{2(1+\alpha i_s R)^3} \tag{28}$$

Using the first two generating solutions and (23), the $W(E)$ is approximated in order $K = 1$ by:

$$W_a^{(1)}(E) = \alpha i_s R + \frac{\alpha R z_{dc}}{1 + \alpha i_s R} \tag{29}$$

Substitute this into $I_0 = 0$ and solve for R_L, the optimal resistance based on the 1st order approximation is:

$$R_{L,1}^* = 2N(R_S + \frac{1}{\alpha i_s}) \tag{30}$$

This solution is then the closed-form approximation with the first-order truncation for extremely low input power. Note that what is inside the bracket is the diode's resistance at low power [29], which suggests the load should match the resistance of all diodes in series to obtain maximum output power.

Furthermore, using all three generating solutions in (28), the $W(E)$ is approximated in order $K = 2$ by the following:

$$W_a^{(2)}(E) = W_a^{(1)}(E) - \frac{\alpha^2 R^2 (2 + \alpha i_s R) z_{dc}^2}{2(1 + \alpha i_s R)^3} \tag{31}$$

This approximation of higher order is accurate over a wider z_{dc} range than the 1st order approximation in (29). By substituting this into $I_0 = 0$, multiplying a positive term $\alpha(\alpha^{-1} + i_s R)^4/(i_s^2 z_{dc})$ to both sides of the equation, and simplifying, we get a cubic equation about R:

$$\mu R^3 + \frac{\mu}{\alpha i_s} R^2 - \frac{\mu + 5z_{dc}/2}{\alpha^2 i_s^2} R + \frac{1}{\alpha^3 i_s^2} = 0 \tag{32}$$

where $\mu = z_{dc}/2 - i_s$. Since only positive multipliers are used during the derivation of (32), the equation (32) is equivalent to $\frac{\partial P_{dc}}{\partial R_L} = 0$. During the simplification of the above equation, we used approximation $R \approx R_L/2N$ in order to simplify the derivation. This is supported by the fact that the diode series resistance R_S is normally no more than a few tens of Ohm while the optimal load is typically in the order of kilo-Ohm. As the optimal load decreases to lower magnitudes with higher input power, the approximation (31) will become inaccurate, as we will show in Section 4 for validation results. The solution to the above cubic function is found by using Cardano's general cubic formula. The roots of a cubic equation $ax^3 + bx^2 + cx + d = 0$ are given by:

$$x_k = -\frac{1}{3a}(b + \xi^k B + \frac{\Delta_0}{\xi^k B}), \quad k \in \{0, 1, 2\} \tag{33}$$

where x_k is the k-th root, $B = \sqrt[3]{\frac{\Delta_1 \pm \sqrt{\Delta_1^2 - 4\Delta_0^3}}{2}}$, $\Delta_0 = b^2 - 3ac$, $\Delta_1 = 2b^3 - 9abc + 27a^2 d$, $\xi = \frac{-1+\sqrt{-3}}{2}$. The choice of plus or minus in B is arbitrary as long as it does not lead to $B = 0$. We then choose the smallest positive real root out of the three, i.e.,

$$R_{L,2}^* = \min_{\forall k \in \Theta} (2N x_k) \tag{34}$$

where $\Theta = \{k \in \{0, 1, 2\} | x_k \text{ is real and positive}\}$.

Theorem 1. *The smallest positive root of* (32) *is the optimal load resistance that maximizes* P_{dc} *when* $z_{dc} < 2i_s$.

Proof of Theorem 1. Denote the left hand side of (32) by C_{I_0}. C_{I_0} has a positive y-intercept $\frac{1}{\alpha^3 i_s^2}$, so its positive before R increases to its minimum positive root and becomes negative after that. C_{I_0} has the same polarity as partial derivative $\frac{\partial P_{dc}}{\partial R_L}$ because there is only a positive

term multiplied to I_0, which means the first positive root is a local maximizer of P_{dc}. It can be easily proven that C_{I_0} either monotonically decreases or increases first then decreases when $z_{dc} < i_s$ by inspecting C_{I_0}'s derivative. This means C_{I_0} always has a single positive root when $z_{dc} \leq 2i_s$; thus, the local maximizer is also a global maximizer. When $z_{dc} \geq 2i_s$, there may be more than one positive root, but the small z_{dc} assumption is violated so the perturbation approximation is inaccurate anyway. □

4. Validation and Discussions

The validation consists of two parts: simulation and measurement, whose details will be explained in this section. The results and insights obtained from the validation will also be discussed.

4.1. Simulation Setup and Results

To verify the accuracy of the proposed methods, a set of transient simulations are carried out with MATLAB Simscape Electrical [30] by sweeping the load R_L. The load sweep starts from 10 Ω to several tens of kΩ. Two low-barrier Schottky diodes Skyworks SMS7630 and Avago HSMS285x are used for comparison. Key parameters of the two considered types of diode are taken from their data sheets and summarized in Table 1. In Simscape, the junction capacitance C_J is modeled as a voltage dependent parameter calculated based on zero-bias junction capacitance C_{J0}, junction potential V_J, and grading coefficient M. All capacitors in Figure 1 are set to 500 pF. Besides, the simulation is carried out in three different frequency bands: 400 MHz, 900 MHz, and 2.4 GHz, due to their availability of license-free bands.

Table 1. Parameters of two types of Schottky diode that are considered in the simulation.

	i_s	R_S	N	C_{J0}	M	V_J	L_S	C_P
SMS7630	5 μA	20 Ω	1.05	0.14 pF	0.4	0.51 V	0.05 nH	0.005 pF
HSMS285x	3 μA	25 Ω	1.06	0.18 pF	0.5	0.35 V	2 nH	0.08 pF

Figure 3(a1) shows the calculated optimal load of three different rectifier topologies, i.e., half-wave, 1-, and 2-stage voltage-multipliers with Skyworks SMS7630 diode at 400 MHz frequency band. It can be seen that the numerical solution to the analytical model (red) has good accuracy compared with simulated results (blue) for all topologies. This proves that our proposed simplified analytical model is sufficiently accurate and that no numerical simulation is needed. Besides, the optimal load of 1- and 2-stages voltage-multipliers are roughly 2 and 4 times larger than that of the half-wave rectifier, which corresponds to 2 and 4 times more series diodes from the load's view point.

Figure 3(a1) also shows the closed-form solutions with truncation order $K = 1$ (yellow) and $K = 2$ (purple). When $K = 1$, the closed-form result is accurate only when input power is extremely low and is an upper bound of optimal load. This is helpful when determining the specification of an adaptive optimal load system. For $K = 2$, the valid input power region is wider until approximately 30 mV of input voltage amplitude, after which it becomes inaccurate. This completely closed-form solution is helpful in very low power applications due to its extremely low computational complexity.

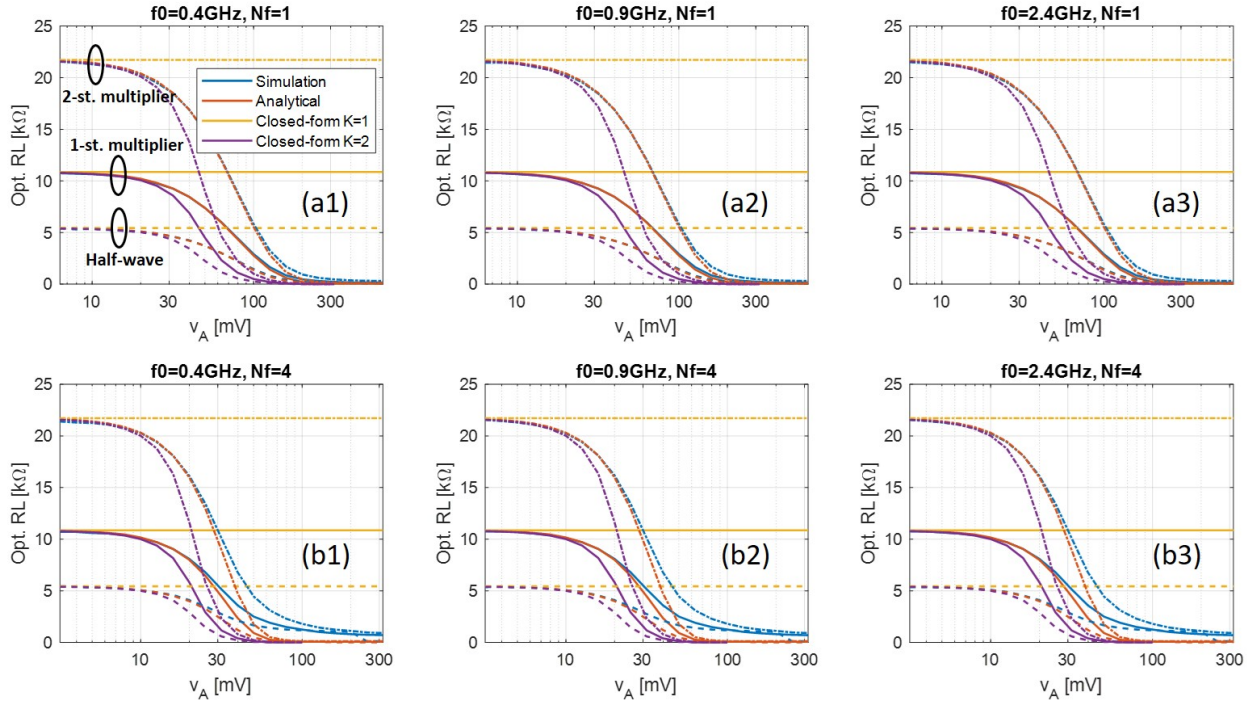

Figure 3. Optimal load calculated by transient simulation (blue), numerical solution of the analytical model (red), and closed-form solutions (yellow and purple), when (**a**) $N_f = 1$, and (**b**) $N_f = 4$ with $\Delta_f = 1$ MHz, with half-wave, 1-, and 2-stage voltage-multipliers using Skyworks SMS7630. The results under different frequency bands (**a1**,**b1**) 400 MHz, (**a2**,**b2**) 900 MHz, and (**a3**,**b3**) 2.4 GHz are shown, too.

Figure 3(a2,a3) also shows results at 900 MHz and 2.4 GHz bands. No clear difference can be observed when frequency is increased to 2.4 GHz. This is because the Skyworks diode has very small parasitic parameters, see Table 1, which means the reactance part of the diode impedance remains negligible within the frequency spectrum that we considered.

Figure 3(b1–b3) shows the calculated optimal load at three different frequency bands, with multisine signals consisting of four subcarriers that are separated by 1 MHz. The numerical solution to the analytical model (red) still shows high accuracy in low input power region, while larger discrepancy is observed as input amplitude increases than when $N_f = 1$. This is because a much larger signal period and thus a much larger ripple is created by the multisine signal. As a result, to minimize the output ripple, an output R-C section with a much larger time-constant is needed than when single-sinusoid signal is used. In the simulation, the output capacitor is 500 pF all the time, so when the load decreases, it will come to a point when the output ripple becomes significant, which is also when the low ripple assumption of the rectification model fails. In practice, this can be avoided by using a large enough capacitor in the output R-C section based on the applied signal.

Figure 4 shows the optimal load calculated by the proposed methods and simulation when using Avago HSMS285x. Similarly to the results with the Skyworks diode, the proposed analytical solution (red) shows very good accuracy compared with simulated results (blue). However, at 2.4 GHz, a slightly larger discrepancy can be observed between the analytical and the simulated results, due to the fact that the Avago diode has considerably larger parasitic capacitance and inductance as can be seen from Table 1. This means at higher frequency, the effect of parasitics becomes more significant while the simplified model neglects it. Nevertheless, the error is still minor within the frequency range that we consider.

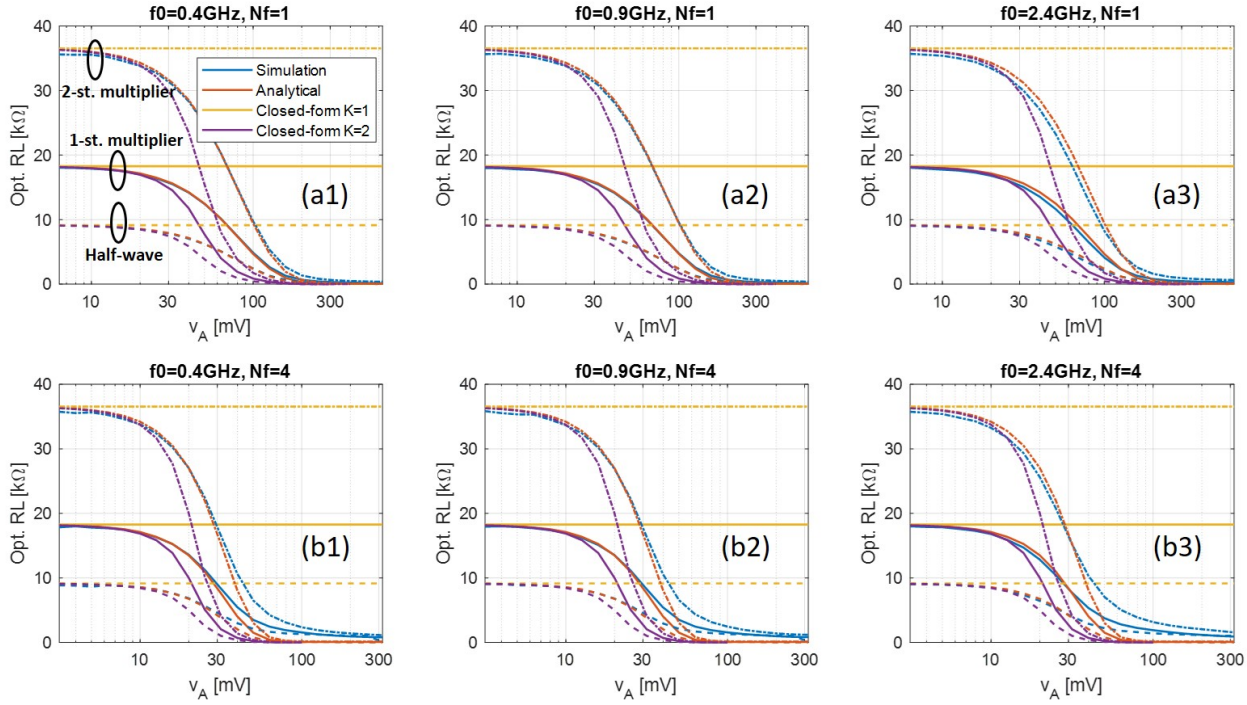

Figure 4. Optimal load calculated by transient simulation (blue), numerical solution of the analytical model (red), and closed-form solutions (yellow and purple) when (**a**) $N_f = 1$, and (**b**) $N_f = 4$ with $\Delta_f = 1$ MHz, simulated with half-wave, 1-, and 2-stages voltage-multipliers using Avago HSMS285x. The results under different frequency bands (**a1**,**b1**) 400 MHz, (**a2**,**b2**) 900 MHz, and (**a3**,**b3**) 2.4 GHz are shown, too.

Another observation is that the optimal load with the Avago diode is almost twice as large as the Skywork's. This can be interpreted from the order 1 closed-form solution. The saturation current i_s of the Avago diode is almost half of the Skyworks one. According to (30), this corresponds to an approximate twice as large optimal load. This observation shows the optimal load of a rectifier is highly dependent on the diode's parameter.

4.2. Measurement Setup

To further validate the results, the one-, and two-stage voltage multiplier PCBs are designed in Altium Designer at 400 MHz and fabricated, see Figure 5. Only 400 MHz is chosen for fabrication because of the lack of high-frequency probes for debugging purposes in our lab. An IS400 substrate with dielectric constant $\epsilon_r = 4.3$ and thickness $h = 0.119$ mm is used. Grounded co-planar waveguide (GCPW) with vias is used as transmission line with track and slot width of 0.225 mm and 0.17 mm to ensure 50 Ω characteristic impedance. An edge-mount SMA connector is used for RF input, and a pin header is used to connect external variable load. All capacitors used on the PCBs are 500 pF. The used Schottky diode is SMS7630-040LF from Skyworks. Measurements have been conducted to obtain experimental data to validate the model presented in Section 2.

The variable load is achieved by a resistor bank on a bread board, see Figure 6. In total, there are 14 resistors, and 16 resistance values are used in the measurement. The used resistance values are listed in Table 2.

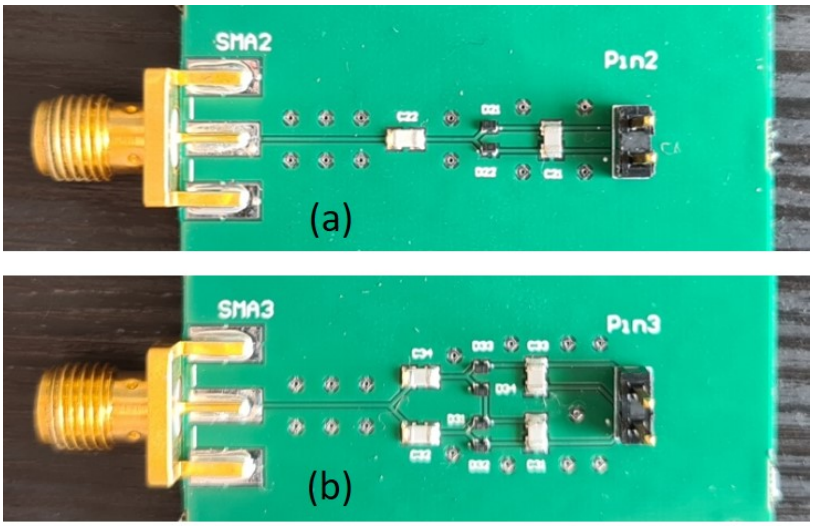

Figure 5. PCB picture of (**a**) one-stage multiplier and (**b**) two-stage multiplier.

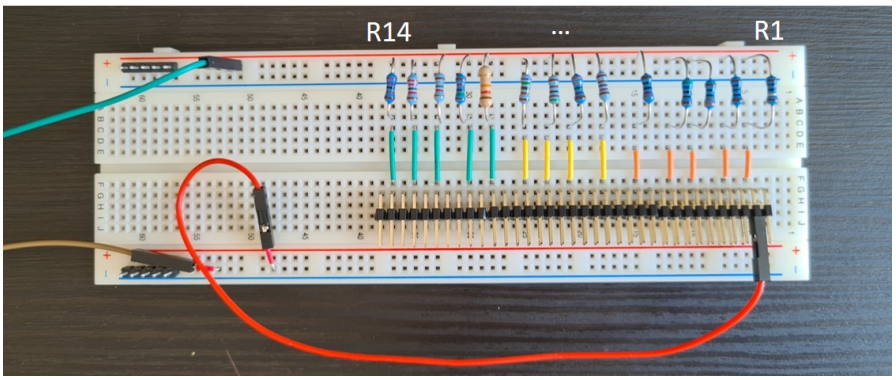

Figure 6. Resistor bank on a bread board.

Table 2. Load resistance values used in the measurement.

	R1	**R2**	**R3**	**R4**	**R5**	**R6**	**R7/R8**	**R7**
Value [Ω]	16.2	100.3	328	558	822	1.2 k	1.99 k	3.29 k
	R8	**R9**	**R11/R14**	**R10**	**R11**	**R12**	**R13**	**R14**
Value [Ω]	5.1 k	7.49 k	9.63 k	11.97 k	14.96 k	18.01 k	22 k	26 k

A Rohde & Schwarz SMW200A signal generator is used as RF source to generate the input signal. The RF source is fed to the SMA connector on the PCB using a coaxial RF cable. The average output voltage of the rectifier is measured by a Keysight MSO7104B digital oscilloscope. The acquisition of measured average voltage is controlled by a windows PC through SCPI remote commands via a USB connection. The remote control session is established by MATLAB using Instrument Control Toolbox. The output DC voltage is measured 20 times during each measurement with 0.5 s interval between consecutive acquisitions. The 20 acquired samples are then averaged to obtain a final measurement result. A picture of the measurement setup is shown in Figure 7.

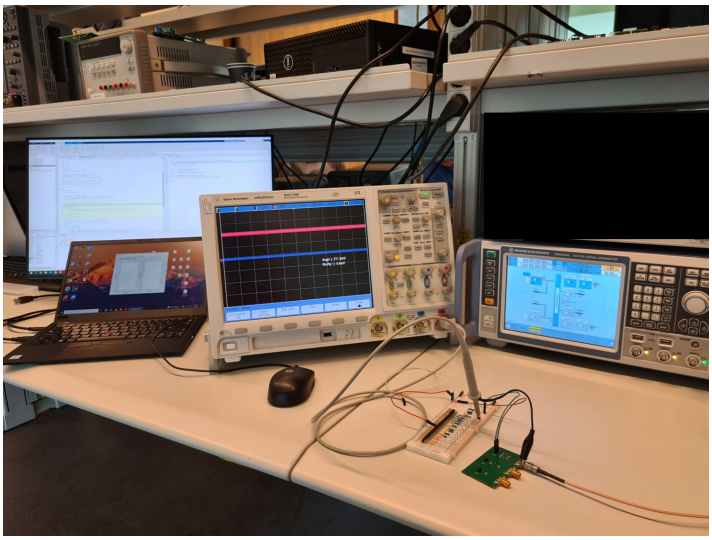

Figure 7. Picture of the measurement setup.

The measured output DC voltage and power with one- and two-stage multipliers are shown in Figures 8 and 9, respectively. The voltage and power are plotted against the load resistance with different tone amplitude V_A. During measurement, V_A is measured at the central pin of the SMA connector on the PCB using a Teledyne LeCroy SDA816Zi serial data analyzer with a ZS1000 active probe with 1 GHz bandwidth. The fluctuation with the measured results with low input V_A and especially low load resistance is because of the low output voltage, which is close to the digital oscilloscope's noise floor. Despite this, the measured and simulated results are consistently in very good agreement.

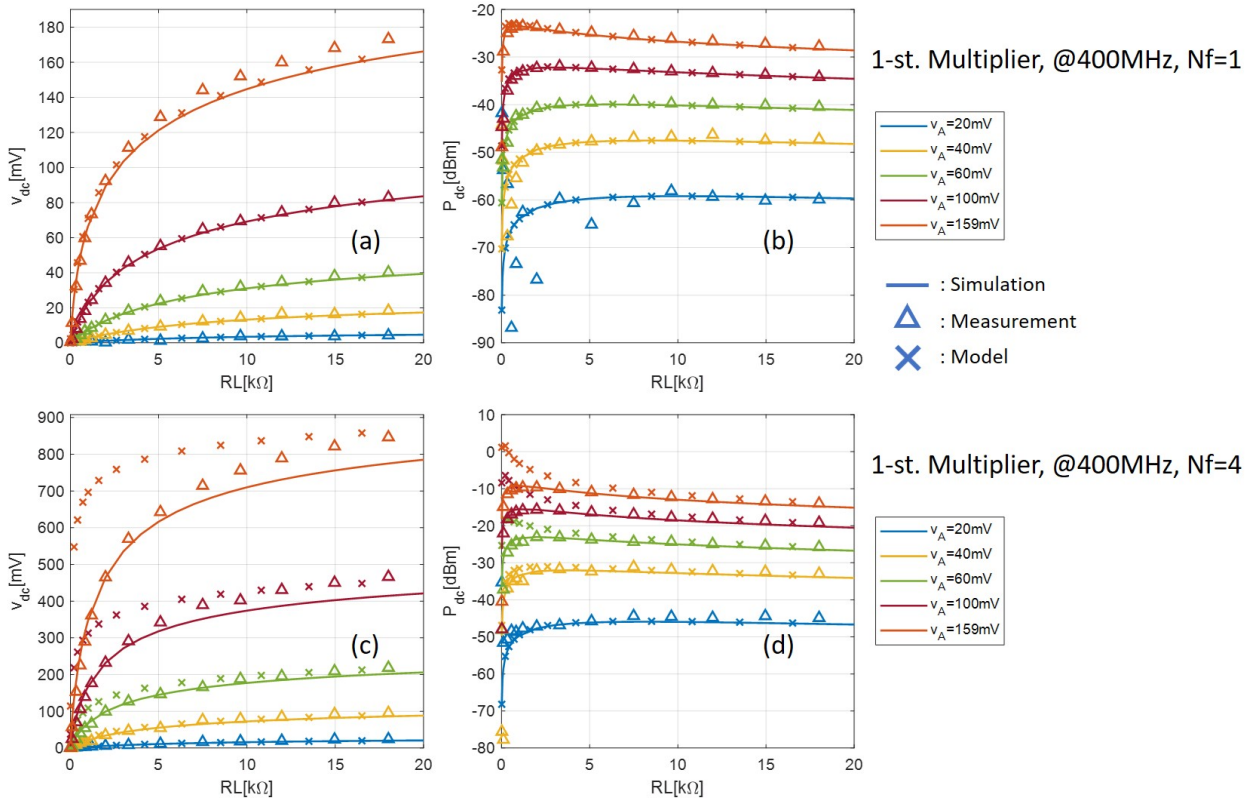

Figure 8. Comparison between measurement, simulation, and analytical model of the one-stage multiplier. Output DC voltage with (**a**) $N_f = 1$ and (**c**) $N_f = 4$; output DC power with (**b**) $N_f = 1$ and (**d**) $N_f = 4$.

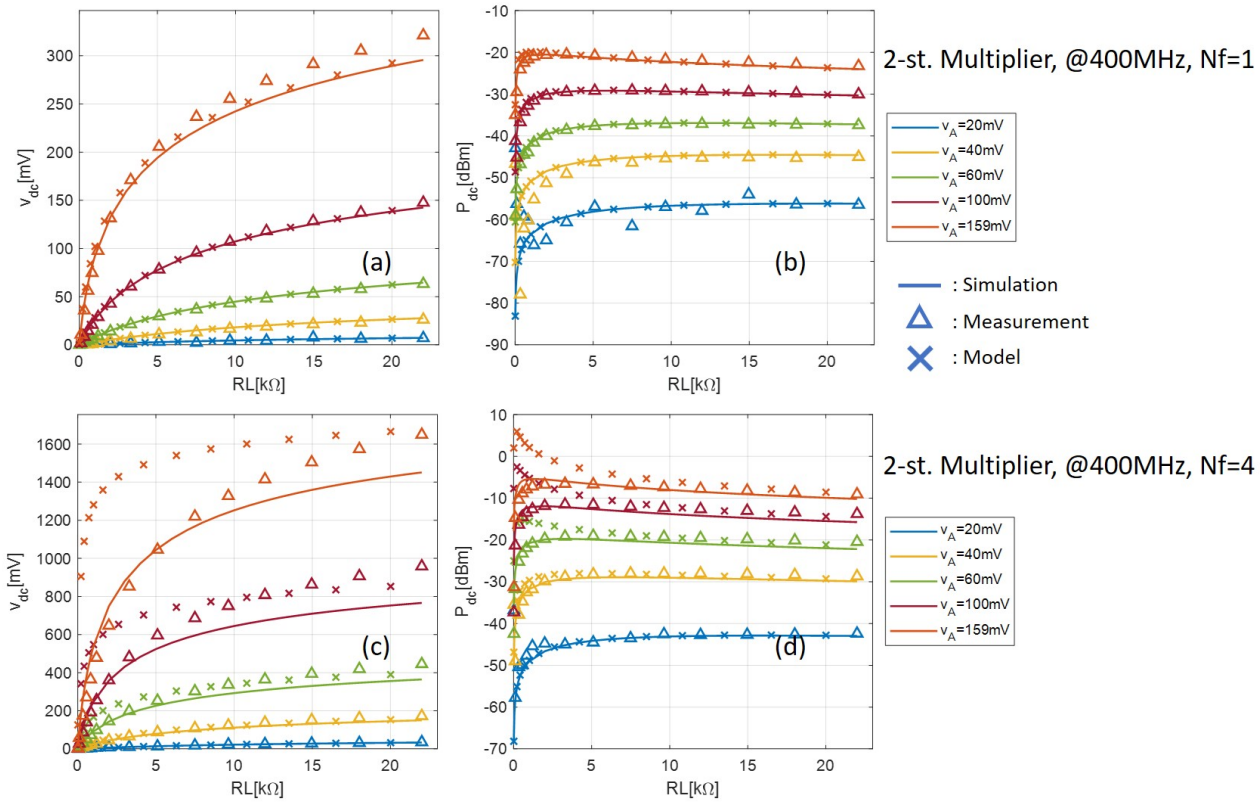

Figure 9. Comparison between measurement, simulation, and analytical model of the two-stage multiplier. Output DC voltage with (**a**) $N_f = 1$ and (**c**) $N_f = 4$; output DC power with (**b**) $N_f = 1$ and (**d**) $N_f = 4$.

Figures 8 and 9 also show the output DC voltage and power calculated by the analytical model given by (17) and (18). The accuracy of the analytical model is confirmed with respect to both measured and simulated results when $N_f = 1$ for all input levels. When $N_f = 4$, however, the model fails to predict the rectifier output with small loads when the input level is high. This is because high PAPR signals in general (in this case the multisine signal) need an R-C section with a higher time constant than the conventional single-sine signal to eliminate the output voltage ripple, and a negligible ripple is a prerequisite for our simplified model, as we explained in Section 4.1. Indeed from Figures 8 and 9, as the load increases, which leads to a larger time-constant, the model becomes more and more accurate.

Moreover, the optimal load based on the measured data as a function of V_A is shown in Figure 10. The simulated results and the numerical solution of the analytical model are also shown as solid and dashed lines, respectively, for comparison. Note that the resolution of the measured optimal load is limited by the step size of the variable load listed in Table 2. Also note that the optimal load associated with the lowest input level tends to be an outlier since the rectifier's output voltage is close to the oscilloscope's noise floor, so more randomness is observed on the left-most measured point in Figure 10a,b. It can be seen that the simulated data is in close agreement with the measured data when $N_f = 1$ and $N_f = 4$. The numerical solution of the analytical model also shows great agreement with the measured data except in the high input V_A region with four-tone multisine signal, which has already been explained before.

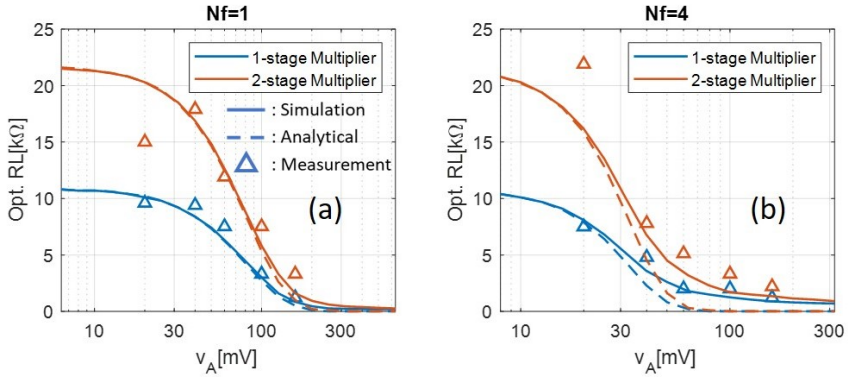

Figure 10. Optimal loads calculated by simulation, numerical solution of the analytical model, and measurement with (**a**) $N_f = 1$ and (**b**) $N_f = 4$. Note that the measured results with the lowest input tone amplitude v_A tend to be outliers since the rectifier's output voltage is close to the noise floor of the oscilloscope.

5. Conclusions

In this paper, we analyzed simplified analytical rectification models for the half-wave rectifier and the N-stage voltage-multiplier. The targeted rectifier topologies are generic, and the models consider the diode as its realistic equivalent circuit. Based on the models, a set of methods that calculate the optimal loading condition for the rectifiers are given, including a low-complexity numerical method, and closed-form approximations for low input power scenarios. The proposed methods are validated by both simulation and measurement.

The simulation results show that the parameters of the diode, namely, saturation current i_s and ideality factor n, significantly influence the optimal loading condition. The simulation results also show that the carrier frequency does not influence the optimal loading condition with Skyworks SMS7630 diode. The effect of frequency gets larger only when the frequency and the diode parasitics get larger. In our simulation, the Avago HSMS285x diode with much higher parasitics exhibits more discrepancy between simulated and analytical optimal loads at 2.4 GHz than 400 MHz and 900 MHz. However, the discrepancy is still negligible. This means the frequency impact is negligible at least below 2.4 GHz.

The proposed numerical and closed-form methods have low computational complexity, which can provide a head start when designing a rectifier system. It provides very good accuracy without the need for either harmonic balance or transient simulation provided that the output voltage ripple is eliminated. Moreover, the proposed methods are also valid for general signals, for example, novel input signals such as the multisine waveform, with which the problem can quickly become infeasibly large for harmonic balance as the number of tones increases [7]. Another possible application is adaptive load control in an actual rectifier to ensure optimal efficiency. Implementation of such a control scheme constitute future work.

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