FACULTY OF ENGINEERING
AND ARCHITECTURE

III-V-on-Si Transceivers Based on Micro-Transfer-Printing

Jing Zhang

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Supervisors
Prof. Günther Roelkens, PhD - Prof. Geert Morthier, PhD

Department of Information Technology
Faculty of Engineering and Architecture, Ghent University

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Supervisors

Prof. Günther Roelkens, PhD, Ghent University
Prof. Geert Morthier, PhD, Ghent University

Dankwoord

When I think about finalizing this over seven years of research and life in Ghent, so many unforgettable moments are flashing through my mind, like playing a movie. All the things that have happened in the past years eventually bring me a clear vision about what I should do and what kind of person I would like to be.

I was lucky to be one of this big family, the Photonics Research Group, while it rather likes a result of destiny. Given this chance, I would like to express my appreciation to a number of people who guided and helped me along the way.

The first one that comes to my mind is my master thesis supervisor, Prof. Xueguang Qiao. He opened the gate of research for me and guided me to the correct route when I was lost. He is cautious, strict, liberal, friendly and, always encouraged me to go further. Prof. Tuan Guo is my lucky charm. With his encouragement, I realized that studying abroad seems not an impossible task, and this will became stronger day by day. I started hunting for a PhD position during my last master year. Time flies and my life switched to a tough mode after my master thesis defense, as I didn't get a PhD position by then, and I had no income. I had to turn to my family for financial support. In this period, I met my girlfriend, who is now my wife, in a series of coincidences, that pretty much looks like a romantic story in a movie. The happiness however did not last long: she started her Ph.D. in Lille, France after a few months and I continued to fight for a Ph.D. position. One day a paper named 'Silicon microring resonators' attracted my attention and following the author's information, I found the Photonics Research Group at Ghent University - imec. Thanks to the help from Yanlu Li, I got in contact with Prof. Günther Roelkens. Two weeks after the interview, I was accepted as a Ph.D. candidate for a project on integrated coherent receivers. After a few days of serious consideration, I decided to start my PhD adventure in Gent. Today, after almost eight years of great experiences, it turns out to have been a correct decision.

Many people were jealous of my PhD project - 'III-V-on-Si heterogeneous integration technologies for advanced optical transceivers', whereas it took me a while to realize how hot and also how challenging it is. Of course, whose PhD research is easy? There were many obstacles, challenges, disappointment, and even hopelessness, especially in the first two years. Fortunately, with the guidance from Prof. Günther Roelkens and Prof. Geert Morthier, the help from colleagues and the support from my family and friends, I could eventually overcome this and

finally accomplished this task. I can never be grateful enough for all these support that I got from you.

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Gent, March 2021
Jing Zhang

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List of Acronyms

A

AlGaInAs	Aluminum Gallium Indium Arsenide
AON	Active Optical Network
APD	Avalanche Photodiode
ASK	Amplitude-shift Keying
AWG	Arrayed Waveguide Gratings

B

BER	Bit Error Rate
BHF	Buffered Hydrofluoric
BOX	Buried Oxide

C

CCW	Counter Clockwise
CMOS	Complementary metal oxide semiconductor
CMP	Chemical Mechanical Polishing
CMRR	Common Mode Rejection Ratio
CO	Central Office
CW	Clockwise

D

DBR	Distributed Bragg Reflector
DC	Directional Coupler

DFB	Distributed Feedback
DI	Deionized
DML	Directly Modulated Laser
DSP	Digital Signal Processing
DVS-BCB	Divinylsiloxane Bis Benzocyclobutene
DWDM	Dense Wavelength Division Multiplexing

E

EAM	Electro-absorption Modulator
EDFA	Erbium Doped Fibre Amplifier
EO	Electrical-to-Optical

F

FDTD	Finite Difference Time Domain
FIB	Focused Ion Beam
FSR	Free Space Range
FTTB	Fiber To The Building
FTTH	Fiber To The Home
FTTX	Fiber To The X
FWHM	Full Width at Half Maximum

G

GaAs	Galliumarsenide
GC	Grating Coupler
Ge	Germanium
GPON	Gigabit Passive Optical Networks
GS	Ground Signal

H

HCl	Hydrochloric
HD	High Definition
HDP	High Density Plasma

I

ICP	Inductively Coupled Plasma
IP	Internet Protocol
IPA	Isopropyl Alcohol
InGaAs	Indium Gallium Arsenide
InGaAsP	Indium Gallium Arsenide Phosphide
InP	Indium Phosphide

L

$LiNbO_3$	Lithium Niobate

M

MF	Mixed Frequency
MMI	Multimode Interference
MOD	Modulator
MQW	multiple quantum well
MZI	Mach-Zehnder Interferometer

N

NGPON	Next Generation Passive Optical Network
NRZ	None Return to Zero

O

OE	Optical-to-Electrical
OOK	On-Off Keying

P

PECVD	Plasma-Enhanced Chemical Vapor Deposition
PD	Photodetector
PDMS	Polydimethylsiloxane
PI	Power Versus Current
PIC	Photonic Integrated Circuits
PON	Passive Optical Network
PPG	Pulse Pattern Generator
PRBS	Pseudorandom Binary Sequence
PSK	Phase-shift Keying
P2P	Point To Point

Q

QAM	Quadrature Amplitude Modulation
QD	Quantum Dot
QPSK	Quadrature Phase Shift keying
QW	Quantum Well

R

RIE	Reactive-Ion Etching

S

SCH	Separated Confinement Heterostructure
SEM	Scanning Electron Microscope
Si	Silicon
SiN	Siliconnitride
SiO_2	Silicon Dioxide
SMSR	Side Mode Suppression Ratio
SOA	Semiconductor Opitcal Amplifier
SOI	Silicon-on-Insulator

T

TE	Transverse Electric

TIA	Transimpedance Amplifier
TPD	Transparent Photodetector

U

UV	Ultraviolet

V

VNA	Vector Network Analyzer
VOA	Variable Optical Attenuator
VCSEL	Vertical Cavity Surface Emitting Laser

W

WDM	Wavelength Division Multiplexing
WG	Waveguide

Nederlandse samenvatting –Summary in Dutch–

1 Inleiding

De opkomst en populariteit van verschillende online diensten en toepassingen in het afgelopen decennium hebben veel aspecten van ons dagelijks leven veranderd. Het zorgt ook voor een buitengewoon druk internetverkeer. In 2020 zal het wereldwijde verkeer naar verwachting 194,4 exabytes/maand bereiken. Tegelijkertijd is het aantal internetgebruikers gestegen tot 52% van de huidige wereldbevolking, wat leidt tot een zware inzet van optische vezels en optische zendontvangers over de hele wereld [1]. Optische communicatie, gebruik makend van optische vezels met enorm lage verliezen, maakt lange-afstandsverbindingen en een hoge bandbreedte van dataoverdracht mogelijk. De toename van de netwerkcapaciteit gaat echter meestal gepaard met de inzet van complexe en dure zendontvangers met een hoog stroomverbruik. De enige manier om dit probleem aan te pakken is fotonische integratie, waarbij een diversiteit van geminiaturiseerde optische en optoelektronische componenten intiem worden geïntegreerd op fotonische chips. Van de bestaande oplossingen biedt silicium (Si) fotonica het grootste potentieel in het realiseren van complexe en compacte fotonische geïntegreerde schakelingen (photonic integrated circuits, PIC's) vanwege het hoge indexcontrast en de mogelijkheid tot monolithische integratie van Si/Ge hogesnelheidscomponenten. Door gebruik te maken van de gevestigde CMOS-procestechnologie kunnen Si PIC's tegen lage kost op grote wafers worden gefabriceerd. Bovendien is het veelbelovend voor de co-integratie van fotonica en elektronica op een gemeenschappelijk substraat.

De indirecte bandkloof van Si belemmert echter monolithische integratie van efficiënte lichtbronnen op SOI-substraten. Hybride integratie van III-V opto-elektronische componenten door middel van flip-chip bonding of pick-and-place is op grote schaal toegepast in de Si-fotonica industrie voor de integratie van III-V-laserdiodes op Si. Maar het blijkt moeilijk om de schaal te vergroten en de kosten van de resulterende PIC's te verlagen vanwege het sequentieel karakter van de operatie en de gecompliceerde uitlijnprocedures. Heterogene integratie door middel van meervoudige die-to-wafer bonding maakt de integratie van III-V/Si-componenten op waferschaal mogelijk. Deze techniek is de afgelopen jaren door Intel gebruikt voor de productie van commerciële Si fotonica zendontvangers.

Het vereist echter een substantiële aanpassing van het Si fotonica back-end proces om de III-V componenten te kunnen bewerken. De intieme integratie van III-V componenten die bestaan uit verschillende epitaxiale lagen is ook zeer uitdagend.

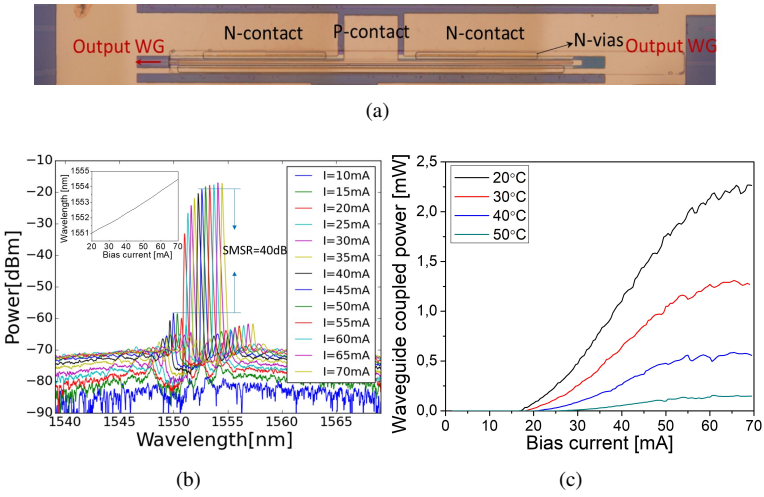
In dit proefschrift hebben we ons gericht op een nieuwe heterogene integratietechnologie: microtransferprinting (μTP), die niet alleen de nauwe integratie mogelijk maakt van bijna elk materiaal of component die kan worden losgemaakt van het oorspronkelijke substraat naar een gemeenschappelijk substraat (hier de Si fotonica wafer), maar ook de mogelijkheid biedt voor de wafer-schaal integratie van deze componenten op een sterk geparallelliseerde wijze. Bovendien is er geen aanpassing van het Si fotonica back-end proces nodig. Door het pre-fabriceren van componenten in dichte arrays op de bronwafer, wordt de verspilling van dure III-V materialen drastisch verminderd in vergelijking met andere technieken, wat weer leidt tot een kostenreductie van de resulterende III-V-on-Si PIC's. Als nieuwe technologie voor de integratie van III-V-halfgeleiders op Si moeten essentiële fabricageprocesstromen ontwikkeld en gestandaardiseerd worden om het gebruik van deze technologie in de fotonica-industrie mogelijk te maken in de toekomst. In dit werk behandelen we de ontwikkeling van processtromen voor de realisatie van verschillende III-V-on-Si componenten via deze aanpak, waaronder de pre-fabricage van III-V componenten (C-band halfgeleider optische versterkers (SOA's) en O-band fotodetectoren (PD's)) op het oorspronkelijke substraat, het vrijmaken en overdragen van deze componenten op een silicium-op-isolator (SOI) substraat, en de post-processing op het SOI substraat. Met deze gevestigde processtromen demonstreren we enkele belangrijke bouwstenen voor optische ontvangers/zendontvangers, waaronder gedistribueerde feedback (DFB) lasers, lasers met een smalle lijnbreedte en brede afstembaarheid en O-band fotodetectoren. Tot slot hebben we twee verschillende fiber-to-the-home (FTTH) zendontvangers gedemonstreerd en de haalbaarheid onderzocht van de realisatie van volledig geïntegreerde coherente ontvangers (ICR's) door middel van co-integratie van verschillende functionaliteiten op een enkele chip via μTP.

2 Resultaten

2.1 Micro-transfer-geprinte gedistribueerde feedback lasers

We hebben eerst III-V-on-Si DFB-lasers gedemonstreerd op basis van de μ-TP van III-V-materiaalcoupons. Een III-V epitaxiale lagenstructuur met 6 AlGaInAs kwantumputlagen en een 500 nm-dikke AlInAs onderetslaag onder de III-V componentlaag werd ontworpen om het vrijgeven van de materiaalcoupons mogelijk te maken. Een volledige processtroom werd ontwikkeld en geoptimaliseerd, met inbegrip van de definiëring van materiaalcoupon arrays op de III-V wafer, het vrijgeven van deze coupons en de μTP van deze coupons op het doelsubstraat (hier SOI PIC's) met een dunne DVS-BCB lijmlaag. Een succesratio van bijna 100% met een ultradunne ($<$30 nm) en uniforme DVS-BCB lijmlaag werd gedemonstreerd in de μTP experimenten. De optische koppeling tussen het Si en het III-V

werd gerealiseerd door middel van een III-V/Si modeconvertor die werd gedefinieerd met behulp van 300 nm contactlithografie. Een representatieve component (Fig. 1), met een Bragg rooster van 300 µm lang, vertoonde continue en monomodale (continuous wave single mode) werking rond 1550 nm met 40 dB zijmode-onderdrukking (SMSR: side mode suppression ratio). De drempelstroom en het maximale enkelzijdige golfgeleidervermogen zijn respectievelijk 20 mA en meer dan 2 mW, bij 20 °C.

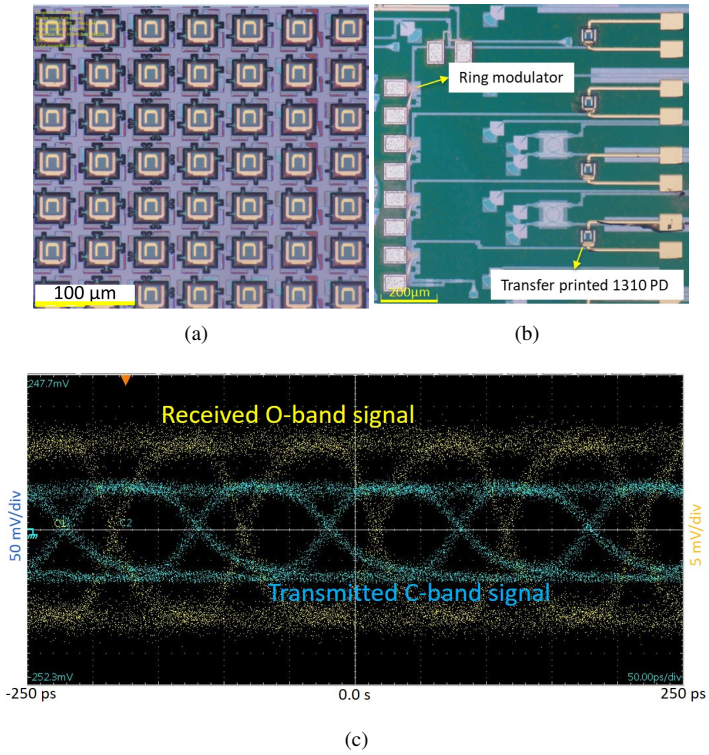


Figuur 1: Performantie van de gefabriceerde III-V-on-Si DFB laser. (a) Microscoopbeeld van een representatieve DFB-laser, (b) Superpositie van de uitgangsspectra bij verschillende stromen, de ingevoegde figuur toont de evolutie van de lasergolflengte als functie van de stroom, (c) P-I-curve bij verschillende temperaturen.

2.2 Fiber-to-the-home zendontvanger array met 4 kanalen

We ontwikkelden een hele processtroom voor de integratie van voorgemaakte III-V PDs via µTP (Fig. 2(a)). Gebaseerd op deze reeds gevestigde processtroom, hebben we een 4 kanaals Point-to-Point (P2P) FTTH zendontvanger array gedemonstreerd (Fig. 2(b)). De Si PICs werden gerealiseerd op het imec iSiPP25G platform, en bestonden uit een array van C-band Si ringmodulatoren en een array van C-band glasvezelroosterkoppelaars (fibre grating couplers). De PDs werden eerst geprocest op de III-V wafer en voorzien van elektrische contacten en dan vrijgemaakt in een $FeCl_3$ oplossing. We aligneerden en transfereerden deze PDs met succes op de corresponderende glasvezelroosterkoppelaars voor de O-band data ontvangst. De geïntegreerde III-V/Si PD's vertoonden een responsiviteit van 0.39-0.49 A/W voor het O-band signaal, vier grootteordes groter dan voor de C-band, wat bidirectioneel gebruik toelaat. Een 10 Gbit/s werking werd gedemonstreerd in

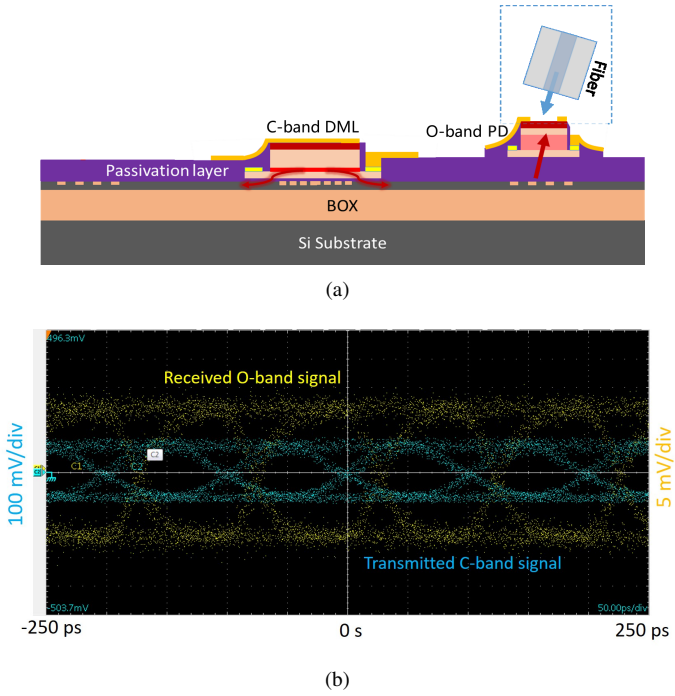
dit werk (Fig. 2(c)).



Figuur 2: (a) Microscoopbeeld van een geprefabriceerde O-band III-V PD-array na onderetsen. (b) Microscoopbeeld van de gefabriceerde zendontvanger-array met een array van getransferprinte O-band PD's, (c) Oogdiagram aan 10 Gbit/s.

2.3 FTTH zendontvanger met enkelvoudig kanaal

We demonstreerden een FTTH zendontvanger met enkelvoudig kanaal door de co-integratie van een O-band PD, geassisteerd door een glasvezelroosterkoppelaar, met een C-band III-V-op-Si DFB laser (het schema is weergegeven in Fig. 3(a)). De responsiviteit van de getransferprinte O-band PD is ~ 0.3 A/W voor het O-band signaal. De DFB laser is gefabriceerd door µTP van III-V coupons en het post-processen van deze coupons op de Si fotonische chip. De laser werd rechtstreeks gemoduleerd om het stroomafwaartse C-band signaal te encoderen. 10 Gbit/s en 12.5 Gbit/s werking werd gerealiseerd met deze zendontvanger (Fig. 3).



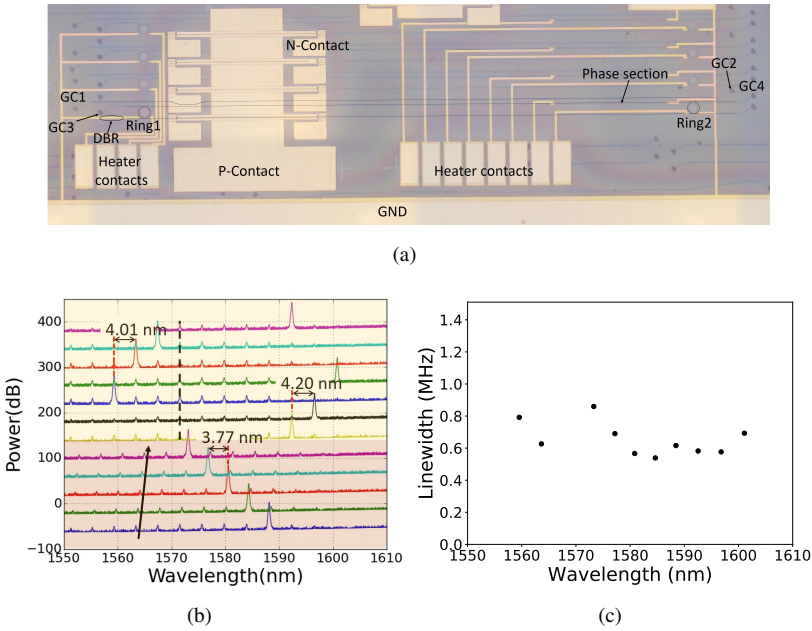
Figuur 3: (a) Schema van de III-V-on-Si enkelvoudig kanaal zendontvanger; (b) Oogdiagram aan 10 Gbit/s.

2.4 Getransferprinte breed afstembare lasers met smalle lijnbreedte

Na het realiseren van breed afstembare (40 nm golflengte bereik) en lage lijnbreedte (onder 1MHz) lasers door middel van die-to-wafer bonding (Fig. 4), demonstreerden we soortgelijke lasers door µTP van geprefabriceerde SOA's op passieve fotonische circuits die werden gerealiseerd op het imec 400 nm platform. Een III-V/Si modeconvertor met een zijdelingse uitlijningstolerantie van 1 µm werd ontworpen. Deze componenten lieten 48 nm golflengtebereik zien en een minimale intrinsieke lijnbreedte van 300 kHz (Fig. 5). Het vermogen in de golfgeleider gaat tot 6 dBm.

2.5 Volledig geïntegreerde coherente ontvangers

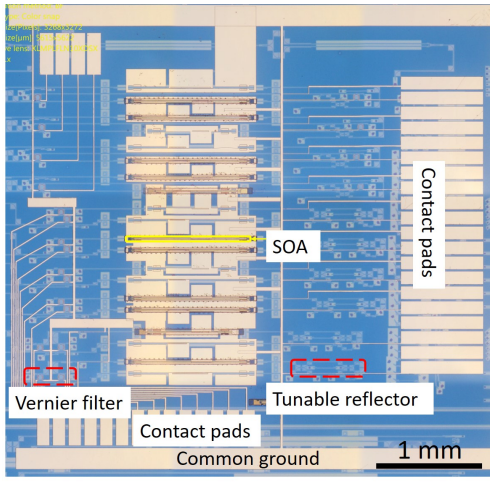
Er zijn twee verschillende benaderingen onderzocht om volledig geïntegreerde coherente ontvangers (ICR's) aan te tonen. De eerste methode is gebaseerd op de



Figuur 4: (a) Microscoopbeeld van een reeks breed afstembare lasers die door middel van die-to-wafer bonding worden gerealiseerd. (b) Gesuperponeerde uitgangsspectra van een gefabriceerd component, met een afstembereik van 40 nm. (c) Gemeten lijnbreedte bij verschillende golflengten.

co-integratie van een III-V-on-Si lokale oscillator (LO) en III-V gebalanceerde detectoren op een enkele passieve Si-fotonische chip door µTP van geprefabriceerde III-V componenten (SOA's en PD's) . In dit geval werden de Si PIC's gedefinieerd op een SOI-wafer met een 400 nm-dikke Si laag met behulp van e-beam lithografie. De geprinte PD's vertoonden 16 GHz 3-dB bandbreedte bij -3 V en de afstembare lasers vertoonden een 40 nm afstembereik (Fig. 6). Helaas werkten de geïntegreerde ICR's niet door grote golfgeleiderverliezen als gevolg van naadfouten (stitching errors) in de e-beam lithografie.

De tweede methode omvat het co-integreren van C-band III-V-on-Si breed afstembare lasers op het imec iSiPP25G/50G platform, bestaande uit passieve componenten, fotodetectoren, verwarmers en modulatoren. De prestaties van de Si ICR zonder geïntegreerde LO, geïntegreerd met een $0.13\,\mu\mathrm{m}$ SiGe BiCMOS transimpedantieversterker (TIA) array (Fig. 7), werden eerst onderzocht. Kwadratuur faseverschuiving (QPSK) en 16-kwadratuur amplitudemodulatiewerking (16-QAM) bij 28 Gbaud (Fig. 8), werd gedemonstreerd. Processen werden ontwikkeld om pregefabriceerde SOA's in voorgedefinieerde uitsparingen op iSiPP50G fotonische chips over te brengen (Fig. 9). Deze vooruitgang maakt de weg vrij voor de realisatie van volledig geïntegreerde ICR's op (maar niet beperkt tot) het imec iSiPP50G



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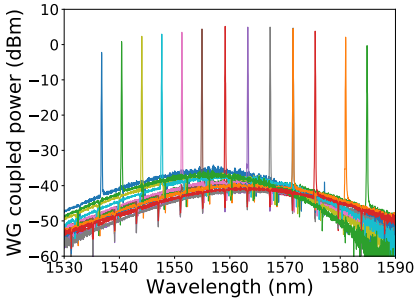

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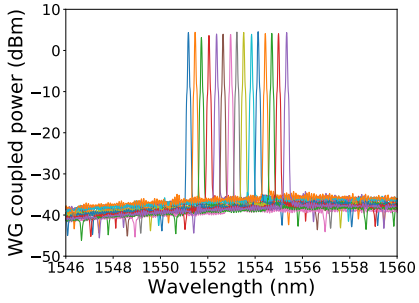

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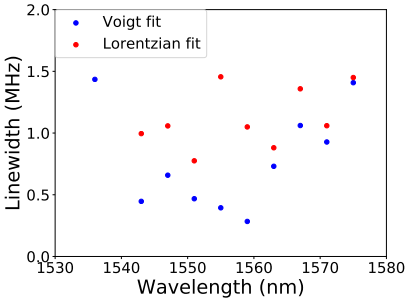
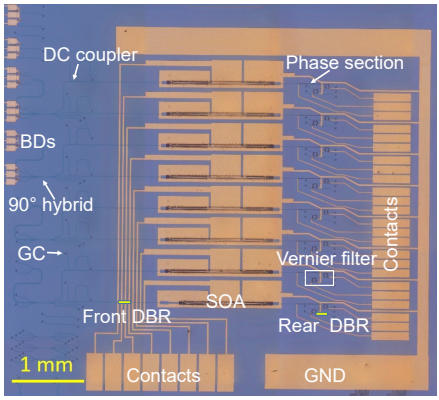


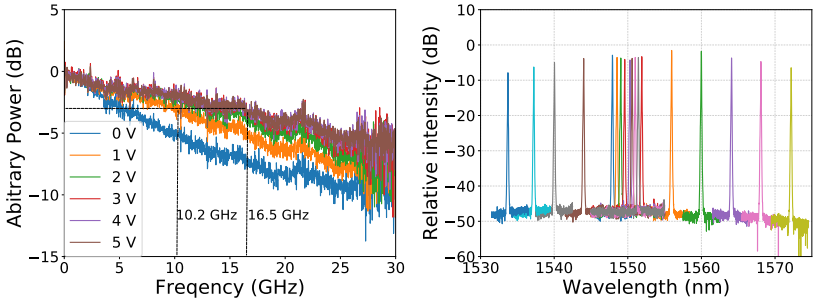
(d)

Figuur 5: (a) Microscoopbeeld van een reeks breed afstembare transferlasers. (b) Gesuperponeerde uitgangsspectra van een gefabriceerd component, met een afstemmingsbereik van 48 nm golflengte. (c) Fijne golflengteafstemming over een volledige FSR van een ringresonator. (d) Gemeten lijnbreedte als functie van de emissiegolflengte.

platform in de toekomst (Fig. 11).



(a)

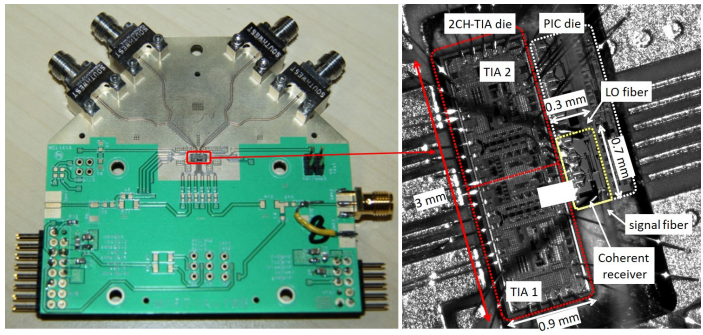


(b) (c)

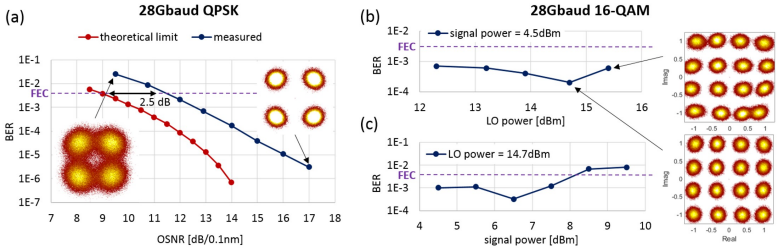
Figuur 6: (a) Microscoopbeeld van gefabriceerde Si ICR's op een passieve fotonische chip. (b) Een representatieve klein-signaalrespons van de transfergeprinte PD, (c) Gesuperponeerde uitgangsspectra van de geïntegreerde afstembare laser, met een afstemmingsbereik van 40 nm golflengte.

3 Conclusie

Dit proefschrift richtte zich op de ontwikkeling van micro-transfer-printing technologie voor de realisatie van III-V-on-Si geïntegreerde opto-elektronische componenten en geïntegreerde ontvangers/zendontvangers. We presenteerden de III-V epitaxiale lagenstructuren die compatibel zijn met het microtransferprintproces. Processtromen, inclusief de fabricage van III-V componenten op de III-V wafer, onderetsen, µTP van deze componenten op Si fotonische wafers en post-printing processen, werden ontwikkeld en geoptimaliseerd in dit werk. Een uitlijningsto-



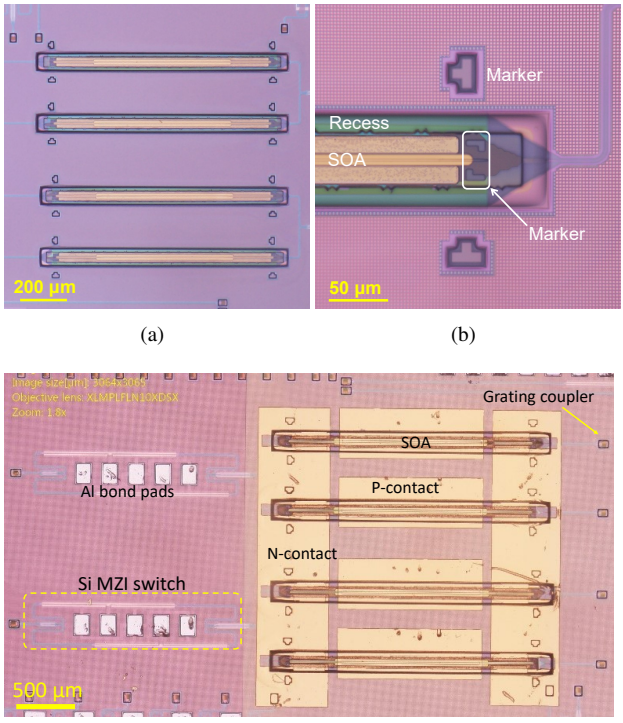
Figuur 7: De hogesnelheidsprintplaat (PCB) met de Si fotonische ICR- en TIA-array en een ingezoomd microscoopbeeld van de wire-bonded elektronische en fotonische chip op de printplaat.



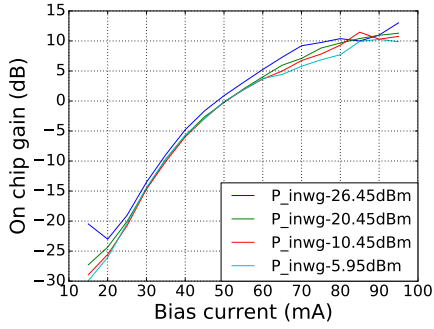
Figuur 8: (a) Bit error rate (BER) vs. optische signaal-ruisverhouding voor 28 GBaud QPSK, (b) BER vs. LO vermogen voor 28 GBaud 16-QAM, (c) BER vs. signaalvermogen voor 28 GBaud 16-QAM.

lerante III-V/Si modeconvertor werd voorgesteld om de realisatie van getransferprinte III-V-op-Si lasers mogelijk te maken. Hetzelfde concept kan worden toegepast voor de integratie van andere soorten III-V componenten (bv. fasemodulatoren en PD's).

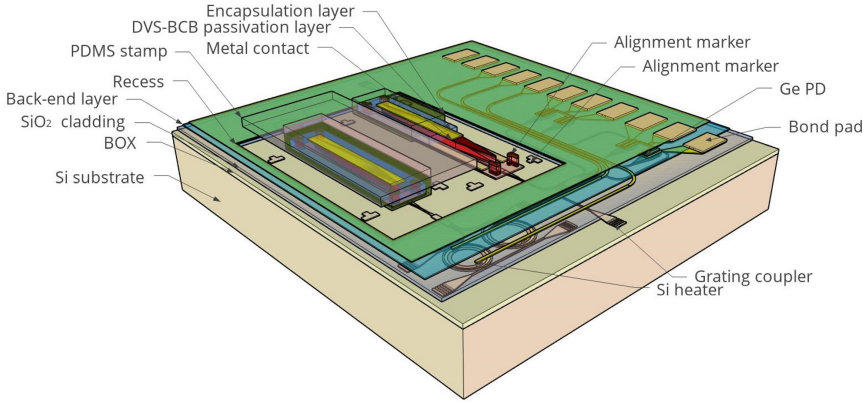
Alleenstaande III-V-op-Si geïntegreerde componenten (bv. DFB-lasers, PD's en breed afstembare lasers) met behoorlijke prestaties (vergelijkbaar met de componenten die via waferbonding worden verkregen) werden met succes gedemonstreerd. We presenteerden ook een vier-kanaals FTTH-zendontvanger-array en een enkelvoudig kanaal FTTH-zendontvanger. Deze twee zendontvangers werden gedemonstreerd door de integratie van geprefabriceerde O-band III-V PD(s) met Si-microring modulatoren en met een transfergeprinte III-V-on-Si DFB laser respectievelijk. We hebben de processtroom voor de co-integratie van III-V-op-Si breed afstembare lasers en C-band PD's op een passief SOI-substraat overlopen voor de realisatie van volledig geïntegreerde ICR's. Anderzijds hebben we belangrijke stappen gezet in de richting van het realiseren van een coherente ontvanger met geïntegreerde LO op het imec iSiPP50G platform via transferprinten. Deze



Figuur 9: (a) PICs met een array van getransferprinte SOA's in uitsparingen. (b) Ingezoomd microscoopbeeld van een getransferprinte SOA.(c) Microscoopbeeld van een array van transfergeprinte SOAs met gedeponeerde metaalcontactblokken.



Figuur 10: Gemeten on-chip versterking vs. geinjecteerde stroom, met meer dan 10 dB versterking bij een stroom van 90 mA.



Figuur 11: Schema van complexe III-V-on-Si PIC's die gerealiseerd kunnen worden op het imec iSiPP50G platform door μTP van III-V optoelektronische componenten.

demonstraties laten de voordelen zien van de veelzijdigheid, het zeer efficiënte III-V materiaalgebruik en de intieme integratie van verschillende functionaliteiten op een enkele Si-fotonische chip. Vanuit het perspectief van de technologische ontwikkeling moeten in de toekomst de inspanningen worden gericht op de automatische en parallelle integratie van grote aantallen geprefabriceerde componenten op 200 mm of 300 mm Si-fotonische wafers.

References

[1] *Global - 2020 Forecast Highlights*. https://www.cisco.com/c/dam/m/en_us/solutions/service-provider/vni-forecast-highlights/pdf/Global_2020_Forecast_Highlights.pdf.

English summary

1 Introduction

The emergence and popularity of various online services and applications in the past decade have changed many aspects of our daily lives. It also results in an extraordinary busy Internet traffic. In 2020, the global traffic is expected to reach 194.4 exabytes/month. At the same time, the number of the Internet users increased to 52% of the global population today, which leads to a heavy deployment of optical fibers and optical transceivers all over the world [1]. Optical communication, utilizing ultra-low loss silica optical fibers, enables long distance connections and allows for high bandwidth data transmission. The increase in network capacity is however usually accompanied by the deployment of complex and expensive transceivers with high power consumption. The only way to address this issue is photonic integration, in which a variety of miniaturized optical, electro-optical/opto-electronic components are intimately assembled/integrated on photonic chips. Amongst the existing solutions, silicon (Si) photonics has the greatest potential in realizing complex and compact photonic integrated circuits (PICs) due to its high index contrast and compatibility with monolithic integration of Si/Ge high speed components. By leveraging the well established CMOS process technology, Si PICs can be scalably manufactured on large wafers at low cost. Moreover, it has potential for the co-integration of photonics and electronics on a common substrate.

However, the indirect bandgap of Si hinders the monolithic integration of efficient light sources on SOI substrates. Hybrid integration of III-V opto-electronic components through flip-chip bonding or pick-and-place has been widely adopted in the Si photonics industry for the integration of III-V laser sources on Si. But it is facing difficulties in scaling up and reducing the cost of the resulting PICs due to the sequential operation and the complicated alignment procedures. Heterogeneous integration through multiple die-to-wafer bonding allows for the wafer scale integration of III-V/Si devices. This technique has been used by Intel for the manufacturing of commercial Si photonics transceivers in recent years. However, it requires substantial modification of the Si photonics back-end process to accommodate the III-V devices. The intimate integration of III-V devices composed of different epitaxial layer stacks is also very challenging.

In this PhD thesis, we focused on a new heterogeneous integration technology - micro-transfer-printing (μTP), which not only enables the close integration of al-

most any material or device that can be released from its native substrate onto a common substrate (here the Si photonics wafer), but also allows for the wafer scale integration of these devices in a massively parallel manner. Moreover, it does not require modification of Si photonics back-end process flow. By pre-fabricating devices of interest in dense arrays on the source wafer, the waste of expensive III-V materials is drastically reduced compared to other techniques, which again leads to a cost reduction of the resulting III-V-on-Si PICs. As a young technology for the integration of III-V semiconductors on Si, essential fabrication process flows have to be developed and standardized to enable the use of the technology in the photonics industry in the future. In this work, we deal with the development of process flows for the realization of various III-V-on-Si devices through this approach, which include the pre-fabrication of III-V devices (C-band semiconductor optical amplifiers (SOAs) and O-band photodetectors (PDs)) on the native substrate, the release and transfer printing of these devices on a target silicon-on-insulator (SOI) substrate, and the post-processing on the target substrate. With these established process flows, we demonstrate some key building blocks for optical receivers/transceivers, including distributed feedback (DFB) lasers, widely tunable and narrow linewidth lasers and O-band photodetectors. Finally, we demonstrated two different fiber-to-the-home (FTTH) transceivers and investigated the feasibility of the realization of fully integrated coherent receivers (ICRs) by co-integrating different functionalities on a single chip via μTP.

2 Results

2.1 Micro-transfer-printed distributed feedback lasers

We first demonstrated III-V-on-Si DFB lasers based on the μTP of III-V material coupons. A III-V epitaxial layer stack with 6 AlGaInAs quantum well layers and a 500 nm thick AlInAs sacrificial layer beneath the III-V device layer was designed to allow for the release of the material coupons. An entire process flow was developed and optimized, which includes the definition of material coupon arrays on the III-V wafer, release of these coupons and the μTP of these coupons on the target substrate (here SOI PICs) with a thin DVS-BCB adhesive bonding layer. Nearly 100% printing yield with ultra thin (<30 nm) and uniform DVS-BCB adhesive bonding layer was demonstrated in the μTP tests. The mode coupling was realized through an inverse III-V/Si taper structure that was defined using 300 nm contact lithography. A representative device (Fig. 1) with a $300\,\mu\mathrm{m}$ long Bragg grating exhibited continuous wave single mode operation around 1550 nm with 40 dB side-mode-suppression-ratio (SMSR). The threshold current and the maximal single-side waveguide-coupled power are 20 mA and over 2 mW respectively, at $20\,^{\circ}\mathrm{C}$.

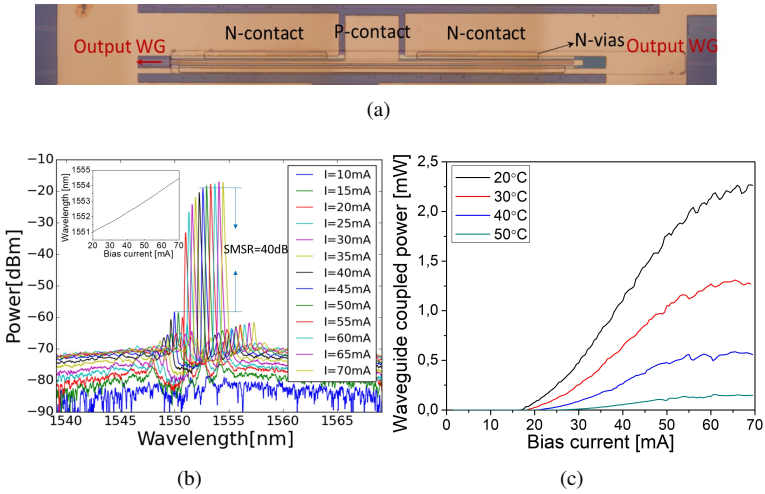


Figure 1: Performance of the fabricated III-V-on-Si DFB laser. (a) Microscope image of a representative DFB laser, (b) Superposition of the output spectra at different bias currents, the inset shows the lasing wavelength evolution as a function of current, (c) P-I curve at different temperatures.

2.2 4 channel fiber-to-the-home transceiver array

We developed an entire process flow for the integration of pre-fabricated III-V PDs via μTP (Fig. 2(a)). Based on this established process flow, we demonstrated a 4 channel Point-to-Point (P2P) FTTH transceiver array (Fig. 2(b)). The Si PICs were realized on the imec iSiPP25G platform, consisting of an array of C-band Si ring modulators and an array of C-band fiber grating couplers. The PDs were first processed on the III-V source wafer with n-type and p-type metal contacts and then released in an aqueous $FeCl_3$ solution. We successfully aligned and transfer printed these PDs onto the corresponding fiber grating couplers for the O-band upstream data reception. The integrated III-V/Si PDs exhibited a responsivity of 0.39-0.49 A/W for the O-band signal and four orders of magnitude lower for the C-band signal, allowing bidirectional operation of the transceiver. 10 Gbit/s operation was demonstrated in this work (Fig. 2(c)).

2.3 A single channel fiber-to-the-home transceiver

We demonstrated a single channel FTTH transceiver by co-integrating a grating coupler assisted O-band PD with a C-band III-V-on-Si DFB laser (the schematic is shown in Fig. 3(a)). The responsivity of the transfer printed O-band PD is ~ 0.3 A/W for the O-band signal. The DFB laser was fabricated by μTP III-V material coupons and post-processing of these coupons on the Si photonic chip. The laser

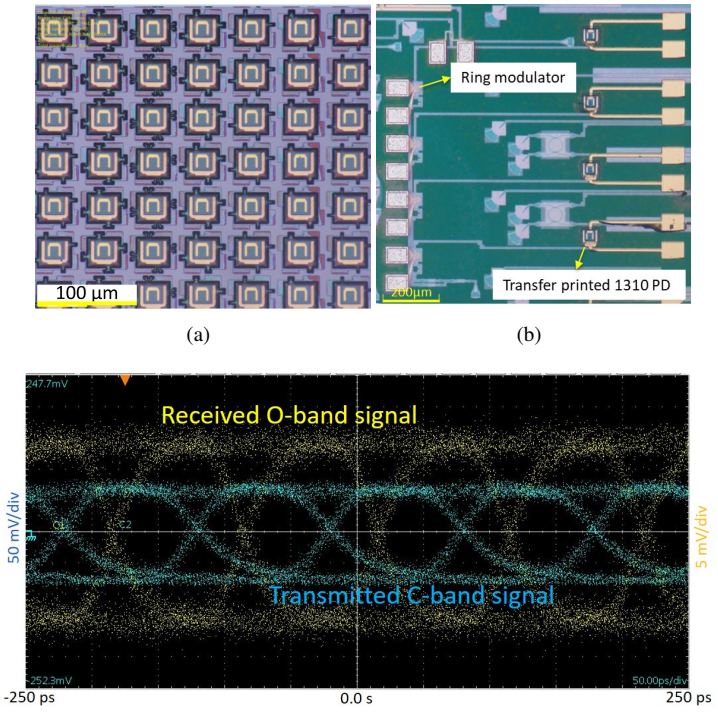


Figure 2: (a) Microscope image of a pre-fabricated O-band III-V PD array after release. (b) Microscope image of the fabricated transceiver array with an array of transfer printed O-band PDs, (c) Demonstrated eye diagram at 10 Gbit/s.

was directly modulated to encode the downstream C-band data signal. 10 Gbit/s and 12.5 Gbit/s operation was realized using this transceiver (Fig. 3).

2.4 Transfer printed widely tunable and narrow linewidth laser

After realizing widely tunable (40 nm wavelength tuning range) and narrow linewidth (below 1 MHz) lasers through die-to-wafer bonding (Fig. 4), we demonstrated similar lasers by µTP pre-fabricated SOAs on passive photonic circuits that were realized on the imec 400 nm platform. A III-V/Si taper structure with a lateral alignment tolerance up to 1 µm was designed to accommodate the (± 1.5 µm, 3σ) alignment accuracy that can be obtained by the µTP system. The fabricated devices showed 48 nm wavelength tuning range and a minimal intrinsic linewidth of 300 kHz (Fig. 5). The waveguide-coupled power goes up to 6 dBm around the gain peak.

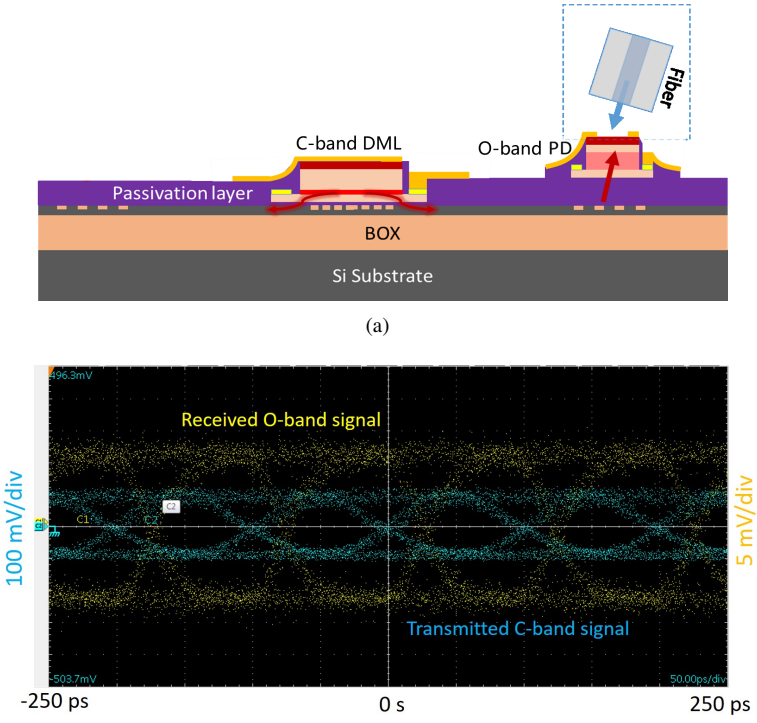


Figure 3: (a) Schematic of the III-V-on-Si single channel transmitter; (b) Demonstrated eye diagram at 10 Gbit/s.

2.5 Fully integrated coherent receiver

Two different approaches were investigated for demonstrating fully integrated coherent receivers (ICRs). The first method is based on the co-integration of a III-V-on-Si local oscillator (LO) and III-V balanced detectors on a single passive Si photonic chip by μTP of pre-fabricated III-V devices (SOAs and PDs) . In this case the Si PICs were patterned on an SOI wafer with 400 nm thick device layer using E-beam lithography. The transfer printed PDs showed 16 GHz 3-dB bandwidth at -3 V and the tunable lasers exhibited a 40 nm wavelength tuning range (Fig. 6). Unfortunately, the integrated ICRs did not operate due to large waveguide losses caused by stitching errors in the e-beam lithography.

The second method is by co-integrating C-band III-V-on-Si widely tunable lasers on the imec iSiPP25G/50G platform, comprising passives, photodetectors,

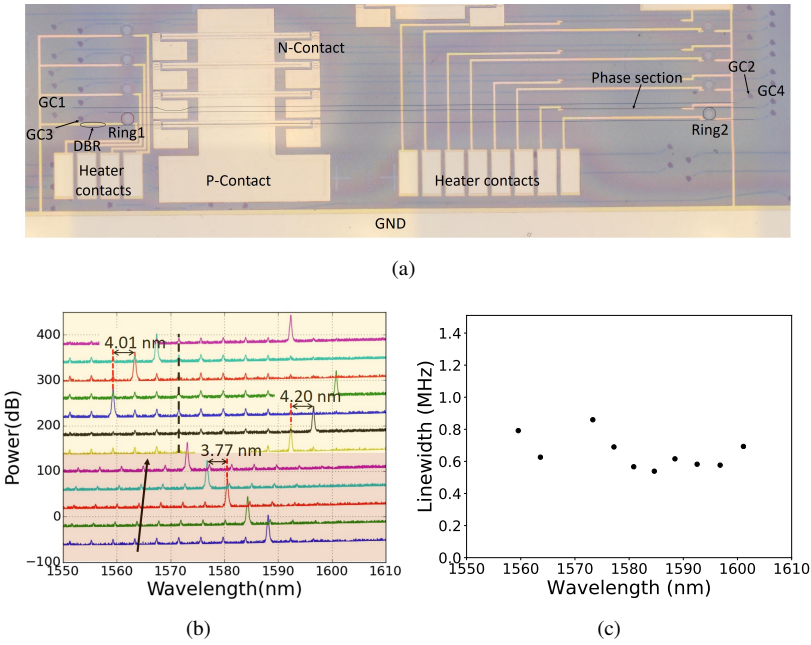
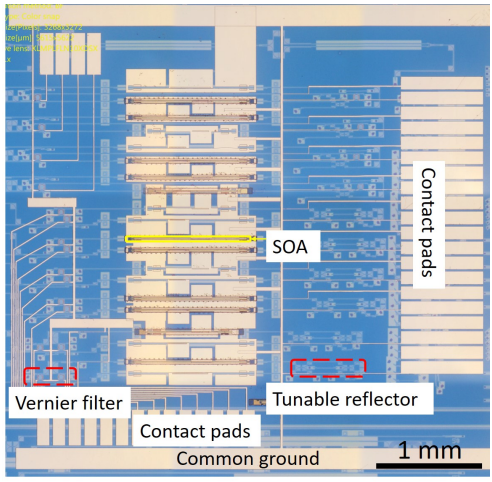


Figure 4: (a) Microscope image of an array of widely tunable lasers realized through die-to-wafer bonding. (b) Superimposed output spectra of a fabricated device, showing a 40 nm tuning range. (c) Measured linewidth at different wavelengths.

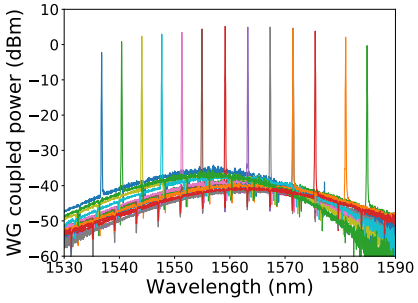
heaters and modulators. The performance of the Si ICR without integrated LO, which was integrated with a $0.13\,\mu m$ SiGe BiCMOS transimpedance amplifier (TIA) array (Fig. 7), was first investigated. Quadrature phase shift keying (QPSK) and 16-quadrature amplitude modulation (16-QAM) operation at 28 Gbaud (Fig. 8) was demonstrated. Processes were developed to transfer print pre-fabricated SOAs in pre-defined recesses on iSiPP50G photonic chips (Fig. 9) and over 10 dB on-chip gain was demonstrated with $950\,\mu m$ long devices (Fig. 10). This progress paves the way for the realization of fully integrated ICRs on (but not limited to) the imec iSiPP50G platform in the future (Fig. 11).

3 Conclusion

This PhD thesis focused on the development of micro-transfer printing technology for the realization of III-V-on-Si integrated opto-electronic components and integrated receivers/transceivers. We presented the III-V epitaxial layer stacks that are compatible with the µTP process. Process flows, including the fabrication of III-V devices on the III-V wafer, release, µTP of these devices on Si photonic



(a)



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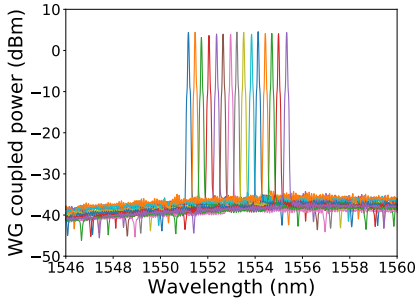

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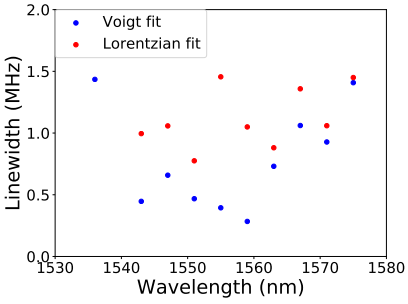


(d)

Figure 5: (a) Microscope image of an array of transfer printed widely tunable lasers. (b) Superimposed output spectra of a fabricated device, showing 48 nm wavelength tuning range. (c) Fine wavelength tuning over a full FSR of a ring resonator. (d) Measured linewidth as a function of the emission wavelength.

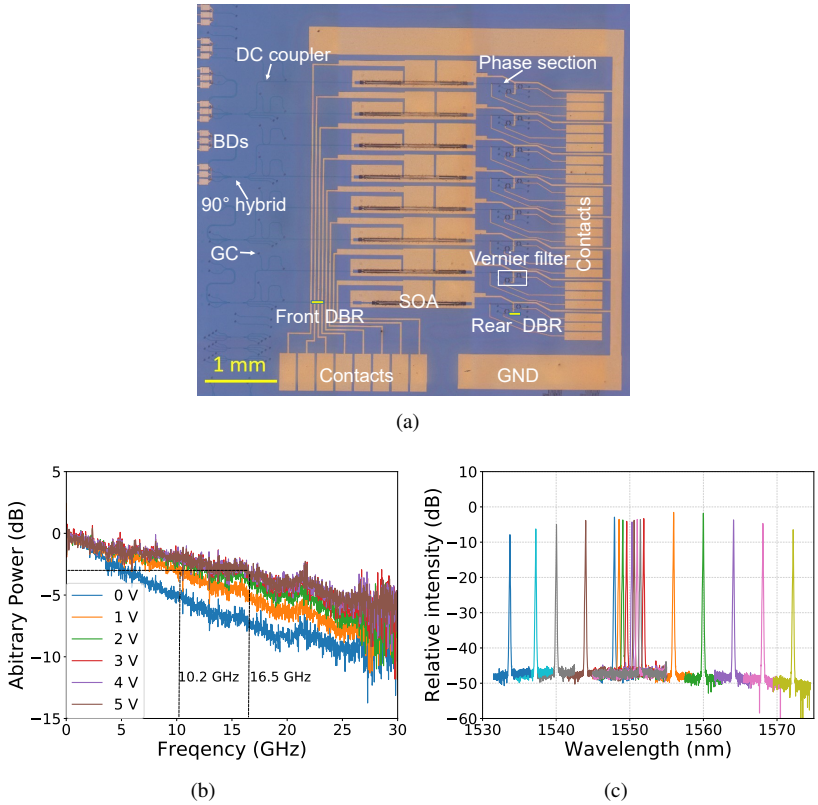


Figure 6: (a) Microscope image of fabricated Si ICRs on a passive photonic chip. (b) A representative small signal response of the transfer printed PD, (c) Superimposed output spectra of the integrated tunable laser, showing 40 nm wavelength tuning range.

wafers and post-printing processing, were developed and optimized in this work. An alignment-tolerant III-V/Si taper structure was proposed to enable the realization of transfer printed III-V-on-Si lasers. The same concept can be adopted for integrating other types of III-V devices (e.g. phase modulators and PDs).

Stand alone III-V-on-Si integrated devices (e.g. DFB lasers, PDs and widely tunable lasers) with decent performance (comparable with the devices demonstrated via wafer bonding) were successfully demonstrated. We also presented a four channel FTTH transceiver array and a single channel FTTH transceiver. These two transceivers were demonstrated by intimately integrating pre-fabricated O-band III-V PD(s) with Si microring modulators and with a transfer printed III-V-on-Si DFB laser respectively. We went through the process flow for the co-integration of III-V-on-Si widely tunable laser and C-band PDs on a passive SOI substrate for the realization of fully integrated ICRs. On the other hand, we made

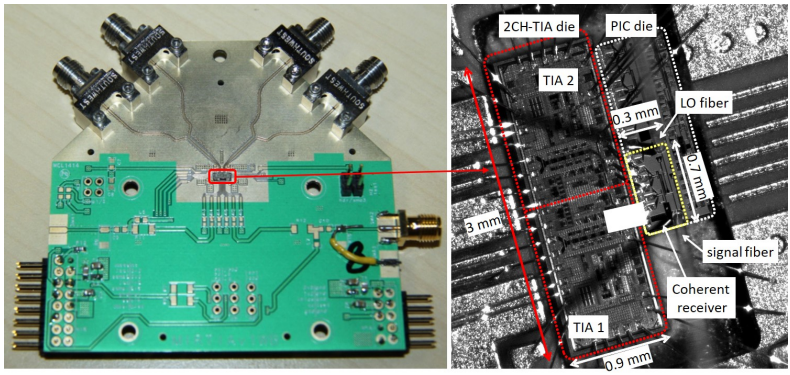


Figure 7: View of the high-speed printed circuit board (PCB)with the Si photonic ICR and TIA array and a zoom-in microscope image of the wire bonded electronic and photonic die on the PCB.

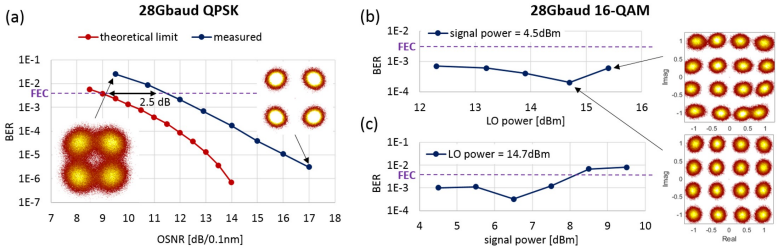
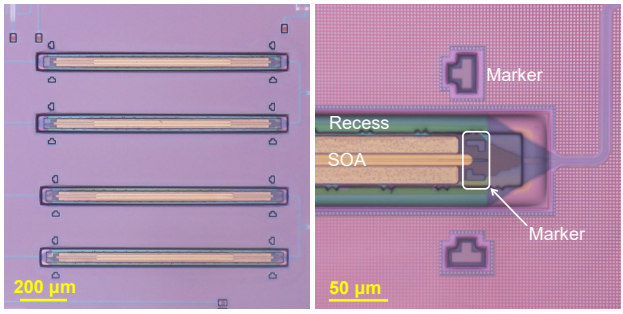
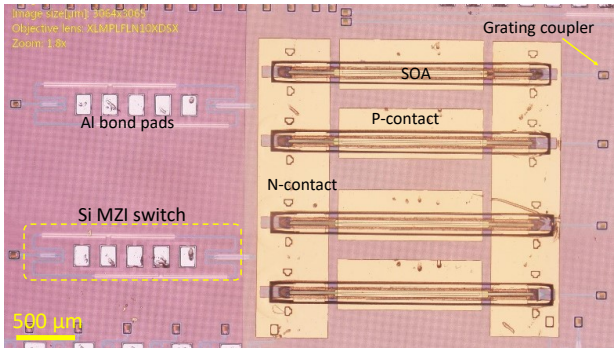


Figure 8: (a) 28 Gbaud QPSK bit error rate (BER) versus optical signal to noise ratio (OSNR) curve, (b) 28 Gbaud 16-QAM BER versus LO power, (c) 28 Gbaud 16-QAM BER versus signal power.

important strides towards realizing a coherent receiver with integrated LO on the imec iSiPP50G platform via transfer printing. These demonstrations showcase the μTP advantages of versatility, highly efficient III-V material usage and intimate integration of different functionalities on a single Si photonic chip. From the perspective of technology development, future efforts should be devoted to the automatic and parallel integration of large numbers of pre-fabricated devices on 200 mm or 300 mm Si photonic wafers.



(a) (b)



(c)

Figure 9: (a) Si PICs with an array of transfer printed SOAs in recesses. (b) Zoom-in microscope image of a transfer printed SOA. (c) Microscope image of an array of transfer printed SOAs with deposited metal contact pads.

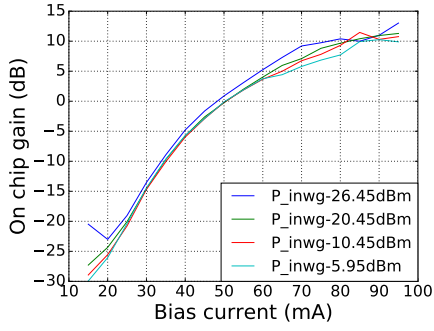


Figure 10: Measured on-chip gain with the bias current, showing over 10 dB on-chip gain at a bias current of 90 mW.

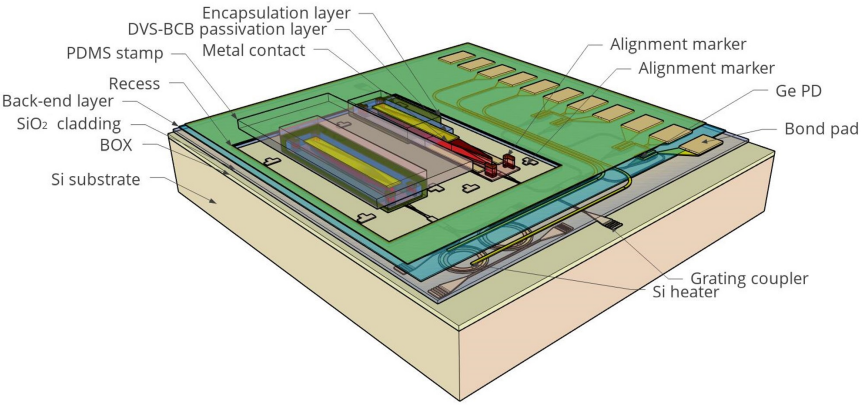


Figure 11: Schematic of complex III-V-on-Si PICs that can be realized on the imec iSiPP50G platform through μTP of III-V opto-electronic components.

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[1] *Global - 2020 Forecast Highlights*. https://www.cisco.com/c/dam/m/en_us/solutions/service-provider/vni-forecast-highlights/pdf/Global_2020_Forecast_Highlights.pdf.

1 Introduction

1.1 Fiber-optic communication

The invention of the telegraph and the morse coding technique in the 1830s started the era of long-distance communication. In a later stage, the ubiquitous deployment of telephones radically changed life all over the world. With the growing popularity of these telecommunication services, the electrical networks started showing their limits in terms of bandwidth and reach due to the high transmission loss of electric cables at high frequencies (>10 MHz) for long interconnects [1].

This issue drove scientists to seek a better solution to address the capacity shortage and stretch the reach of the networks. By then the use of light to transmit data re-emerged. Soon after the breakthrough in low loss optical fiber manufacturing and the demonstration of room temperature operation lasers, the first fiber-optic telecommunication system (45 Mbit/s over 45 km distance) was installed in the late 1970s, followed by a numbers of field trials undertaken in the UK and the US (AT&T, British Post Office, etc.) [2]. These successes marked the arrival of the fiber-optic communication era.

It took an enormous effort and vast investments to form today's fibre-optic networks. As shown in Fig. 1.1, the whole world is connected by optical fibers. Over 400 fiber optic cables have been deployed undersea and the overall length of them reaches 1.2 million kilometers [3]. In recent years, the emerging online social media (Twitter, FaceBook,etc.) and a variety of services such as Youtube, and the demand for high definition (HD) video streaming resulted in an exponential

growth of the the required network capacity. As predicted by Cisco, the global internet traffic will reach 396 Exabytes/Month by 2022 (Fig. 1.3). Optical networks can be roughly divided into three layers: long haul, metro and access networks based on the distance, as shown in Fig. 1.2. In the late 2010s, coherent communication together with powerful digital signal processing (DSP) techniques were implemented in long haul systems to improve the spectral efficiency and capacity. The highest capacity underseas fiber links today, the Marea cable, which is partially owned by Microsoft, Amazon, and Facebook operates at 160 Tbit/s [4]. Today, coherent communication is also finding its way in shorter reach links, such as metro networks and some access networks (although mostly intensity modulation / direct detect (IM/DD) is still used in access). In order to cope with the growing hunger for bandwidth of end users, tremendous efforts and investments have been devoted to fully exploit the potential of the existing twisted pair and coax networks. However, the maximum speed is still limited to tens of Mbps, and it decreases profoundly with distance because of the high transmission loss, as shown in Fig. 1.4 [5]. The only route to address this issue is connecting end users with optical fibers. These fiber optic systems that connect to the end users are represented as 'Fibre To The X' (FTTX), where the 'X' describes to where the optical fiber that comes from the central office (CO) reaches and, on the other hand, also indicates the length of the remaining copper wires in this 'last mile', as shown in Fig. 1.5 [6]. If the fiber reaches the user's home, then this system is called fiber-to-the-home (FTTH). Benefiting from the rapid evolution of fiber-optic technologies the cost of optical communication systems as well as the management cost of the network have been significantly reduced over the past decades. This trend has greatly accelerated the implementation of FTTX networks. The emergence of 5G wireless technologies are shaping today's optical networks and bring them new challenges.

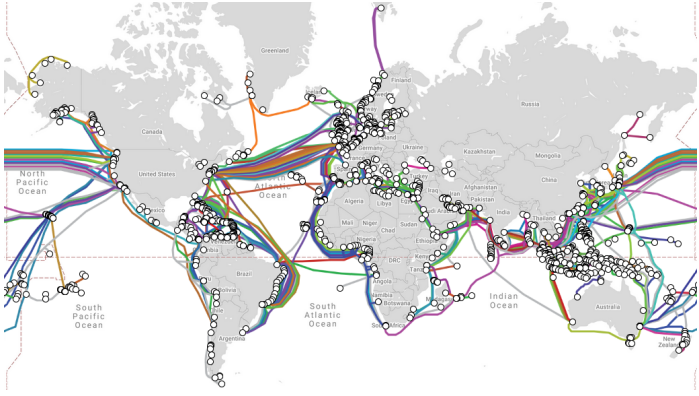

Figure 1.1: Submarine optical fiber connections. Reproduced from [7].

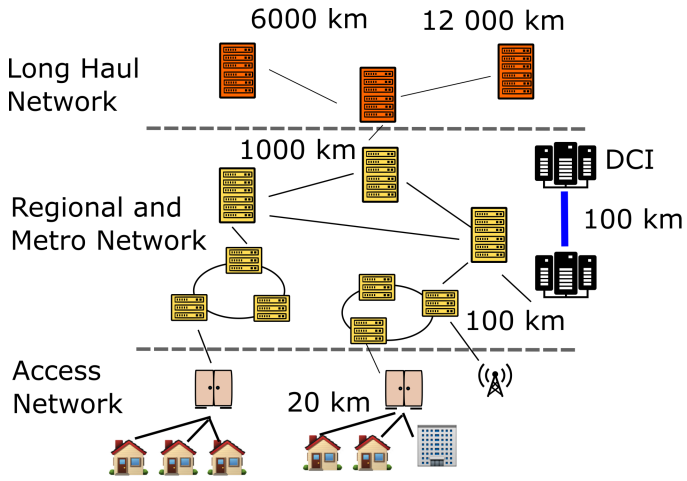

Figure 1.2: Three levels of optical networks with different reach of the fibre-optic link. Reproduced from [8].

1.2 Optical fiber links

A generic fiber-optic transmission system consists of three essential elements : a transmitter, a fiber link and an optical receiver, as shown in Fig. 1.6. The optical transmitter is used to convert the electrical signal, which represents the original data stream to be delivered, into optical form. Here an optical source that is electrically pumped provides a stable optical signal, whose amplitude, phase or both of them are varied corresponding to the electrical signal via an optical modulator (while for short reach links also direct modulation of the laser source can be used). The resulting modulated optical carrier is then launched into the optical fiber and transmitted to the other end through the fiber link. To reach further, fiber-based optical amplifiers are often used in the fiber link to boost the optical signals. Moreover, wavelength multiplexers and demultiplexers are also intensively employed to increase the network capacity. At the other end, a receiver is used to convert the incoming optical signals to electrical signals using photodetectors (PDs), a signal which is then often processed using a digital signal processing (DSP) module to readout the delivered data. The function of the optical fibers is to transport light that carries data. Therefore the most important characteristics of optical fibers is the attenuation and the dispersion. The most used optical fibers in today's optical networks is the single mode silica fiber, which has a thin silica core with a diameter around $9\,\mu\mathrm{m}$ and a $62.5\,\mu\mathrm{m}$ thick cladding with slightly lower refractive

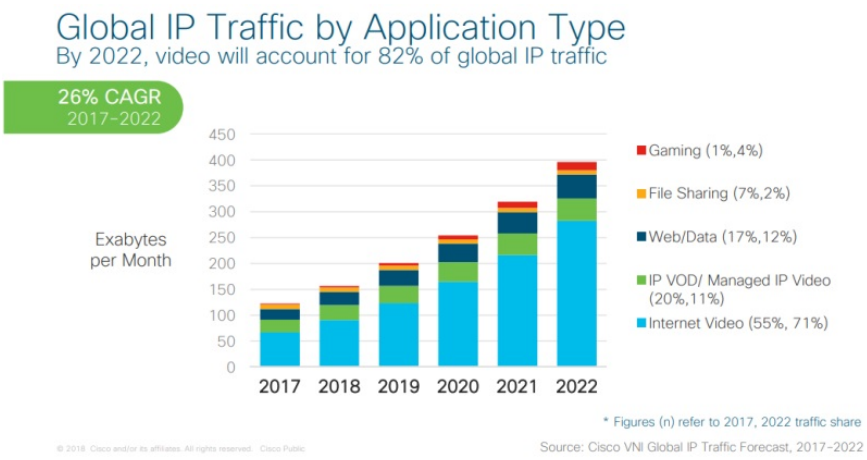

Figure 1.3: Prediction of global IP traffic in the coming years by Cisco.

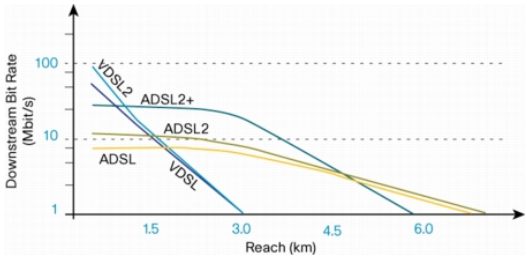

Figure 1.4: Approximate reaches achieved for different asynchronous digital subscriber line (ADSL) standards. (source:cisco)

index. This optical fiber exhibits a low loss and near zero dispersion in O-band and minimal loss (0.2 dB/km) in C-band. Therefore these two wavelength ranges are mostly utilised for data transport with O-band for short-reach and C-band for long-reach optical networks.

Determined by the fiber transmission windows, the lasers required in the transmitters have to operate either in the O-band or in the C-band. III-V semiconductors, e.g. InP [10] and GaAs [11] material systems, with direct bandgaps are ideal candidates for light emission. Different types of III-V lasers, depending on their characteristics and cost, have been used in optical transmitters, including DFB lasers [8, 12], DBR lasers [13, 14], widely tunable and narrow linewidth lasers [15–18], VCSELs [19, 20], etc.

Data is encoded on the optical carrier produced by the laser source, by adjusting its amplitude (intensity), with the high and low amplitude (intensity) representing the 1 and 0, respectively. This modulation format is called On-Off keying. In

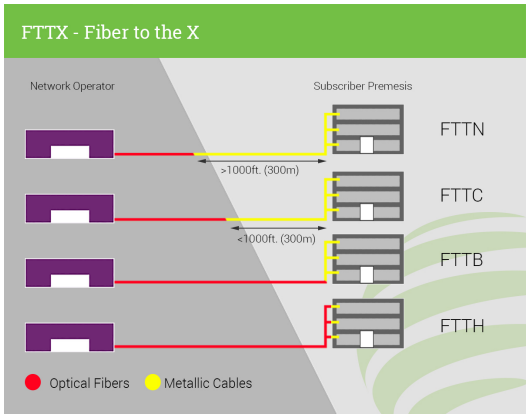

Figure 1.5: Schematic layout of the FTTx describing where the optical fiber reaches and the length of the remaining copper wire. Reproduced from [9]

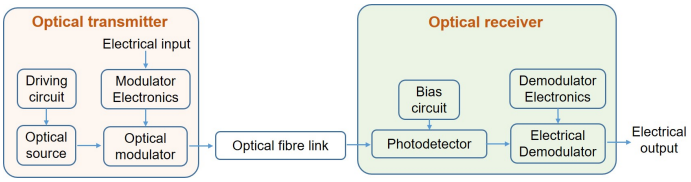

Figure 1.6: Block diagram of a fiber-optic transmission system.

order to increase the data rate, pulse-amplitude modulation (PAM) with more than two amplitudes levels can be used. Electro-optical modulators, such as Si microring modulators and Si Mach-Zehnder interferometer (MZI) modulators based on the carrier-depletion effect in Si have been developed for this intensity modulation. Alternatively, III-V or Ge based electro-absorption modulators can be used for the same purpose. Compared to OOK or PAM intensity modulation, more advanced modulation formats can achieve much higher spectral efficiency of the transmitted signal, in which the information is encoded with two degrees of freedom (e.g. phase-shift-keying (PSK) modulation, amplitude-shift-keying (ASK) modulation or both combined (X-QAM)) [21]. An IQ-modulator consisting of two parallel nested MZI modulators is usually used to modulate the amplitude and phase simultaneously.

The PD is another key building block in optical receivers. It converts the incoming optical signal into an electrical signal. Both InP-based semiconductors and Ge are suitable for realizing high speed O-band and C-band PDs with high responsivity and low dark current. The amplitude/intensity information can be directly detected using a single detector. In a coherent receiver typically a local oscillator

and a pair of balanced detectors is needed to extract the phase information.

In case of short-reach communication systems (e.g. access networks, intra-datacenter connections), the requirements in terms of cost, power consumption and form factor for optical transceivers are stringent. DFB lasers are usually employed as optical sources or transmitters due to their compact footprint, high output power and single longitudinal mode output. As an example, 56 Gbit/s NRZ operation over 2 km nonzero dispersion shifted fiber was demonstrated by Dr. A. Abbasi, et al. in 2017, using a III-V-on-Si integrated DFB laser [12]. In the same year, he extended the fiber link to 20 km using standard single mode fiber by applying a chirp management technique [22].

In case of long haul optical systems, the cost of the system is mostly determined by the fiber links and the deployment of these, which puts less stringent requirements on cost, power consumption and form factor of the transmitters. An effective route to amortize the operation cost is to increase the network capacity. This is realized by employing advanced modulation formats, however with the cost of extra complexity of coherent transceivers, where a narrow linewidth tunable laser and IQ modulators are required for the transmitter and, on the other hand, an optical hybrid, a pair of balanced detectors, a local oscillator (in case of an intradyne scheme) and a powerful DSP are required at the receiver side. The first commercial coherent communication system was put in use in 2008, operating at 40 Gbit/s (10 Gbaud/s) [23]. One year later, a 100 Gbit/s (28 Gbaud) single wavelength transceiver was released by Alcatel-Lucent [24]. This was arguably a milestone in optical communication history. Very soon, these transceivers were widely deployed in the long haul networks and later in metro networks. Driven by the rapid increase in bandwidth demand, an enormous research and development is carried out in pursuing Tbit/s transceivers. Today, coherent transceivers already are key components in metropolitan area networks and in the near future they most likely will also penetrate the shorter-reach networks, especially in inter-data centre interconnections. Together with the application of these transceivers in shorter optical links, the issue of power consumption, cost and footprint becomes important again, particularly in central offices and datacenters where a huge number of transceivers are deployed. These requirements dictate the need for photonic integrated circuits.

1.3 Photonic integrated circuits

The great success of electronic integrated circuits (EICs) has set an good example for the photonics industry. By minimizing the size of electronic components and integrating them closely to form a compact electronic circuit on a chip, the performance of the resulting electronics systems are significantly improved. Directed by Moore's law, the semiconductor fabrication technology has been constantly im-

proved over the past 60 years. Today, it is possible to squeeze close to 100 million transistors per square millimeter using the 7 nm process technology. This density can be increased to 171.3 million transistors per mm^2 in the 5 nm process node [25]. The reduction of footprint also brings other benefits, including reduced cost, improved stability and lower power consumption.

The demonstration of the laser by Maiman in 1960 revolutionized modern optics. 10 years later semiconductor lasers with continuous wave output at room temperature were developed [26, 27]. This groundbreaking achievement together with the improvement in low loss optical fiber enabled optical communication. It also sparked enormous research interests in developing waveguide circuit technology. Inspired by the success in integrated electronic circuits, S.E. Miller proposed the concept of integrated optics (the origin of today's photonic integrated circuits, PICs) in 1969, which includes the integration of various optical functions on a single planar substrate and interconnecting them with low loss waveguides [28]. Similar to integrated electronics, the miniaturization of optical components and their integration on a single chip was later verified to be the only route to realize high performance, low power consumption and low cost optical systems. A variety of waveguide platforms have been developed based on different material systems (e.g. Silica, Silicon, III-V materials, Lithium Niobate, Polymer, etc.) and fabrication technologies. Determined by the material properties, these platforms all have their pros and cons.

1.3.1 Silica-on-silicon

This platform enables ultra low loss [29] and fiber matched waveguides due to its low refractive index and small index contrast [30]. It is promising to integrate Er-doped optical sources and amplifiers in waveguide circuits. However, the large required bending radius ($>$2 mm) makes these circuits less compact and, the absence of electrically driven active components limits the complexity of photonic integrated circuits (PICs) realized on this platform.

1.3.2 Silicon-on-insulator

This platform consists of a thin crystalline Si device layer, a thick Si substrate to provide a mechanical support and typically a $2\,\mu m$ thick SiO_2 in between. The Si waveguide circuits can be covered by a back-end layer stack to electrically interface with the modulators and PDs and to integrate metal heaters [31]. This platform is suitable for devices operating in a wavelength range from $1.1\,\mu m$ to $4\,\mu m$, due to the absorption of Si at shorter wavelength and the absorption of SiO_2 and leakage loss at longer wavelength. The high index contrast of Si/Ge over SiO_2 not only allows for compact PICs but also results in an enhanced light-matter

interaction enabling efficient active devices including Si ring modulators, Ge photodiodes, avalanche photodiodes and electro-absorption modulators. The use of complementary metal-oxide-semiconductor (CMOS) processes allows for scalable and low-cost production of PICs on 200 mm or 300 mm wafers [32]. However, the indirect bandgap of Si makes it unsuitable for realizing integrated optical sources.

1.3.3 Lithium Niobate

Lithium Niobate ($LiNbO_3$) has large electro-optic, acousto-optic, and piezoelectric coefficients, which attracted interest for realizing high-speed optical modulators and other active devices [33]. $LiNbO_3$ waveguides fabricated by the diffusion of metal ions, have a propagation loss below 1 dB/cm [34]. Due to the rise of optical communication which required a large number of high speed optical modulators in the 1980s, the $LiNbO_3$ waveguide technology was significantly accelerated. Similar to silica-on-silicon platform the small index change induced by the metal ion diffusion or proton exchange results in a large required bending radius and hence large footprint of waveguide circuits. Therefore, this platform is also mostly used for stand-alone devices. With the advent of a $LiNbO_3$-on-silicon platform and the break through in dry etching of $LiNbO_3$, the index contrast is significantly improved. This progress led to a revival of $LiNbO_3$ photonics in recent years [33–36].

1.3.4 III-V semiconductors

III-V semiconductor materials are alloys that consist of group III elements and group V elements [37]. These material films are epitaxially grown on a binary semiconductor wafer. Their superior properties, such as low effective masses, high mobilities and a direct band gap make these material systems competitive not only for PICs but also for high-speed EICs. By engineering the composition of the elements, the bandgap of the material can be tuned over a large range, which enables the use of these materials for the realization of complex PICs with various integrated functions, such as lasers, optical modulators, photodetectors and passive waveguides [38]. However, for particular applications in telecom and datacom big companies such as Intel, IBM, Cisco, Acacia Communications prefer the use of silicon photonics (augmented with III-V semiconductors) because of the maturity and scale at which these transceivers can be deployed. These materials are also expensive and dedicated process lines are required.

1.3.5 Siliconnitride

Si_3N_4 is a CMOS compatible material and is transparent in the visible and beyond, which makes it a complementary material choice (as it is being used in

CMOS processing) to Si in the visible regime [39, 40]. However, the low losses of the platform can also be exploited at telecom wavelengths [41]. The Si_3N_4-based photonics platform is similar to an SOI passive waveguide platform, but with a thin Si_3N_4 device layer, which is typically deposited by either Low Pressure Chemical Vapour Deposition (LPCVD) or by Plasma Enhanced Chemical Vapour Deposition (PECVD). The refractive index of Si_3N_4 is around 2 at the wavelength of $1.55\,\mu m$. The moderate index contrast (0.5) leads to a reduced compactness but a low waveguide loss [42, 43]. Si_3N_4 has a low thermo-optic coefficient of $2.45\times10^{-5}K^{-1}$ at $1.55\,\mu m$, which makes the photonic circuits insensitive to temperature variation. However, as a trade-off, realizing a large wavelength tuning range becomes difficult. Moreover, due to the large band gap, Si_3N_4 has no two photon absorption at telecom wavelengths, which makes it possible to handle high optical power in waveguides. Similar to other dielectric material based photonic platforms, optical sources are also absent on the Si_3N_4 platform.

1.3.6 Polymers

A variety of polymers that are transparent in the visible and near-infrared wavelength range can be used for photonic integration [44–46]. They are compatible with a wide range of substrates. Polymers with a high electro-optic coefficient are attractive for high speed and low voltage optical modulators. The simple fabrication processes and low material cost makes the polymer waveguide circuits very cheap, whereas these photonic circuits are less compact due to the low index contrast and this platform also lacks active devices. Reliability is also a challenge for these platforms.

1.3.7 Conclusion

Amongst the aforementioned material systems, InP-based compound semiconductors and Si/Si_3N_4 photonic platforms (where the Si_3N_4 can be combined with Si waveguides in the same platform) are the two most popular platforms for today's photonic integrated circuits. The III-V platform offers the possibility of building complex photonic circuits with the broadest range of active optical functions. However, the difficulty in enlarging the InP wafer size and the relative low integration density limit the high volume fabrication of photonic integrated circuits. In contrast, the potential in realizing complex and compact photonic integrated circuits and the CMOS compatibility makes Si/Si_3N_4 photonics more competitive for the future. Again an elegant solution for on-chip integrated optical sources is needed.

1.4 Silicon photonics

In the mid 1980s, Soref and Lorenzo demonstrated the very first optical waveguides in single crystalline silicon with an underlying highly doped silicon substrate with slightly lower refractive index ($\sim$0.01) [47]. These waveguides showed 15 dB/cm propagation loss at $1.3\,\mu\mathrm{m}$. Today's Si photonic integrated circuits are based on SOI substrates, which were first introduced to microelectronics industry to reduce the parasitic capacitance and leakage current in the late 1980s. It was soon recognized that this material system can be also used for the realization of optical waveguides. The high index contrast between Si (3.476 at 1550 nm) and the SiO_2 offers the possibility of miniaturization and the realization of Si based active devices such as modulators, switches and variable optical attenuators by exploiting the enhanced plasma dispersion effect in thin waveguides. In the early days, the top Si device layer was considerably thick, usually micron scale. By using large waveguide cores, most of these Si waveguides exhibited less than 1 dB/cm propagation loss [48]. Tremendous effort has been devoted in downscaling the Si waveguide dimensions and at the same time pursuing low propagation loss in the following years. Today, SOI wafers with a thin (mostly between 200 nm and 500 nm [49, 50]) Si device layer and a $2\,\mu\mathrm{m}$ thick buried SiO_2 are usually used for manufacturing Si PICs. When the waveguide core reduces to sub-micron scale, the scattering loss and back reflection induced by the sidewall roughness becomes more obvious. In 2004, P. Dumon demonstrated 500 nm wide Si wire waveguides with 2.4 dB/cm propagation losses, which were fabricated using 193 nm deep ultraviolet (UV) lithography and RIE dry etching at imec. When the waveguide width reduces to 450 nm, which is latter selected as the standard width for the C-band single transverse electric (TE) mode waveguide width by imec, the propagation loss increased drastically to 7.4 dB/cm. As of today, its propagation loss has been reduced below 2 dB/cm. Besides low loss waveguides, high performance passive building blocks, including fiber grating couplers, MMIs, high quality factor ring resonators, arrayed waveguide gratings, etc. and high speed devices such as doped-Si phase shifters, ring modulators, MZI modulators, Ge PDs, Ge electro-absorption modulators, etc. have been demonstrated. These available building blocks allow for the realization of complex PICs for use in a wide range of applications. However, the lack of integrated optical sources hinders the further reduction of the cost of products due to the required complicated assembly of light sources with Si PICs.

1.5 III-V-on-Si integration

As mentioned above, several III-V semiconductor materials have a direct bandgap, which make them very suitable for light emission, modulation and detection. In

the past years, great effort has been devoted to establishing mature technologies for realizing the cost-effective integration of III-V-on-Si lasers and other non-inherent functionalities on Si PICs. Different approaches including directly epitaxial growth, flip-chip bonding, die-to-wafer/wafer-to-wafer bonding, photonic wire bonding and micro-transfer-printing are being followed. We will discuss these approaches in the following section.

1.5.1 Flip-chip bonding

Flip-chip bonding is a classic integration approach that has been widely explored for the assembly of electronic ICs on a substrate. To mount the chip on the substrate and enable electrical connections, solder bumps are first deposited on the bond pads on the chip (device) of interest. In the flip-chip process, the chip is flipped face down so that its bond pads can be aligned to the corresponding bond pads defined on the substrate. Then a reflow process is performed to melt the solder bumps to have reliable electrical connections. At the same time, due to the surface tension of the molten solder bumps, the chip can be self-aligned to the targeted position, which results in an enhanced alignment accuracy. Passive alignment assisted by markers on both the device and target substrate can be applied [51–55]. By employing a properly designed flip-chip integration interface, array integration is also possible [56, 57]. Today, flip-chip bonders with better than $0.5\,\mu\mathrm{m}$ alignment accuracy are already available [58]. As a way to further improve the alignment accuracy, active alignment can be used. Recently, M. Theurer, et al. proposed an approach that allows for laser array integration to a SiN photonic chip, where optical backscatter reflectometry is utilized to monitor the gap between the laser die and the SiN chip, while mechanical alignment stops are used to level the laser die in vertical direction [57]. An average insertion loss of -2.1 dB was realized in their demonstration. The advantages of flip-chip bonding are obvious. It allows us to use the superior characteristics of readily fabricated III-V devices such as lasers, amplifiers and photodetectors (PDs) and allows for pretesting before assembly, enhancing the compound yield. Wafer scale integration is also possible. However, the die-per-die operation makes the integration slow and costly.

1.5.2 Wafer bonding

Wafer bonding technology enables the transfer of thin material films or devices onto a new substrate wafer. It has long been used in MEMS and IC industry for the fabrication of substrates and devices, 3D integration, etc. Various wafer bonding techniques have been developed [59]. Heterogeneous integration of III-V-on-Si photonic devices through die-to-wafer or wafer-to-wafer bonding has attracted a lot of attention in recent years, as in this case the critical alignment of the III-V structure to the Si waveguide circuit is realized using wafer-scale lithographic

processes. Amongst the existing wafer bonding techniques, direct wafer bonding and adhesive wafer bonding are mostly used for the realization of III-V-on-Si PICs.

Direct wafer bonding Direct wafer bonding is a process that allows for bonding of two wafers without any adhesive. The primary force that attracts the surfaces and joins them together are Van der Waals forces. As this force is extremely short-ranged, the wafers have to be polished and have an ultra-flat, smooth and clean surface [59]. In the process, the wafers are brought into direct contact at a certain point by a slight pressing, normally at the center of the wafer, to initiate the bonding. Once this occurs, the bonding area expands rapidly over the entire wafer. Then high temperature annealing is performed to obtain covalent bonds. This process comes in two flavors: hydrophilic and hydrophobic bonding [60]. Although both the cases provide high quality wafer bonding, the required high temperature annealing is incompatible with processed silicon photonics wafers($<450\,^{\circ}\mathrm{C}$) and III-V epitaxial layer stacks. To overcome this issue, a number of low temperature processes have been developed [61]. The reduction of annealing temperature is realized mainly by modifying the surface properties via a proper surface treatment, e.g. plasma activation. In 2000, D. Pasquariello reported an oxygen plasma-activated wafer bonding process. The annealing temperature was as low as $<200\,^{\circ}\mathrm{C}$ [62]. In this process, the InP wafer and Si wafer are first immersed, respectively, in NH_4OH and buffered HF to remove the native oxide and particles. Then the wafers are loaded together in a RIE tool for an oxygen plasma treatment, which created a very thin layer of highly reactive oxide (15 nm) with silanol(Si-OH) groups, resulting in a hydrophilic surface. Next, the wafers are mated in the RIE chamber and are annealed at $200\,^{\circ}\mathrm{C}$ to form Si-O-Si covalent bonds. An alternative approach, SiO_2 covalent bonding, by depositing thin layer of SiO_2 on both InP and SOI substrate and proper surface treatment (e.g. immersion in boiling diluted RCA-1 solution) also allows for high quality wafer bonding at ($300\,^{\circ}\mathrm{C}$). Care has to be taken that the deposited SiO_2 layer has to be sufficiently thin (typically below 100 nm) to allow for efficient coupling between the III-V devices and the underlying Si waveguides. In 2009, D. Liang et. al successfully transferred a 150 mm InP wafer to a equal size Si substrate via direct wafer bonding [63], which revealed the potential of wafer bonding for III-V-on-Si integration at wafer scale. Following the success in low temperature direct III-V to Si bonding, a wide variety of III-V-on-Si integrated devices have been demonstrated through direct bonding, including micro-disk lasers [64], Fabry-Perot lasers [65], DFB lasers [66] and various tunable lasers [67, 68], photodetectors [69, 70], modulators [71], etc. However, such wafer-to-wafer bonding approach was not followed due to the inefficient use of the expensive III-V material and the large mismatch in commodity III-V and SOI wafer sizes. Some foundries are developing multiple-die-to-wafer bonding processes and a CMOS-compatible III-V post-process flow [72, 73], where III-V dies with millimeter-scale size are first distributed on a temporary carrier, e.g., a Si

wafer, by a pick-and-place method and then integrated on the target SiPh wafer (after its front end processing) through die-to-wafer bonding (as depicted in Fig. 1.7), followed by a back-end process flow for the definition of the III-V structures and the back-end metallization stack. This process has been maturated for commercial use in recent years. In 2016, Intel released its 100G quad small form-factor pluggable (QSFP) transceiver module [74] with lasers integrated through die-to-wafer bonding. However, the back-end process flow has to be modified to accommodate the III-V devices. The compound yield of the III-V-on-Si PICs can be affected, as the III-V devices can only be tested after they have been integrated on the Si photonic wafer. Although the efficiency of the usage of III-V epitaxial materials has been significantly increased, there is still room left for further improvement, as the dimension of the III-V dies (a few square millimeters) are much larger than required. The intimate integration of different III-V materials/devices on a common substrate, while possible [75, 76], is also still challenging.

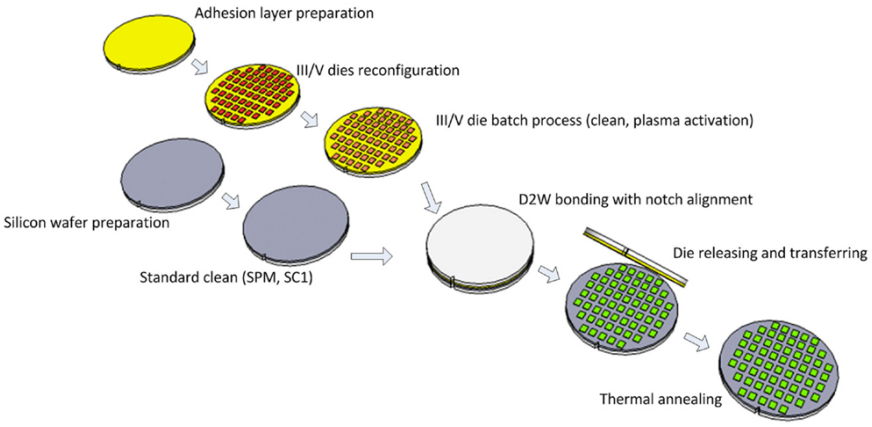

Figure 1.7: Schematic process flow for multiple-die-to-wafer bonding. Reproduced from [73]

Adhesive wafer bonding Compared to direct wafer bonding, adhesive bonding significantly relaxes the requirements on topography, roughness and cleanliness of the wafer surfaces. For the integration of III-V-on-Si devices that require efficient optical coupling between the III-V devices and the Si waveguide circuit, the adhesive of choice has to be transparent in the wavelength range of interest and the bonding layer has to be sufficiently thin. The adhesive material should be cured at a low temperature and be able to survive in aggressive chemicals, which are involved in the III-V processing, after being cured. Divinylsiloxane-bis-benzocyclobutene (DVS-BCB), a thermosetting polymer that was initially developed for applications in on-chip interconnections and microelectronics packaging, well fits the aforementioned restrictions. G. Roelkens et al. from the Photonics

Research Group at Ghent University developed and optimized the DVS-BCB adhesive bonding process for the integration of III-V-on-Si devices [77, 78]. In this process, DVS-BCB is first spin-coated on the SOI substrate, followed by a soft bake to let the solvent (mesithylene) evaporate. Due to its high degree of planarization, this DVS-BCB layer can planarize a waveguide topography with a few hundred nanometers step [79]. After DVS-BCB spin coating, the III-V die or wafer is flipped face down and positioned on the SOI substrate. Afterwards the wafer stack is loaded in a bonding tool for annealing at $250\,^{\circ}\mathrm{C}$ for 1 hour to completely polymerize the DVS-BCB. By using a highly diluted DVS-BCB:Mesithylene (e.g. 1:8) solution, an ultra-thin (<50 mn) and uniform DVS-BCB bonding layer can be realized. Almost all the devices realized via direct bonding were also demonstrated through DVS-BCB adhesive bonding with comparable performance.

1.5.3 Micro-transfer-printing

Micro-transfer-printing (μTP) is a relatively recent integration technique developed by the Rogers group at the University of Illinois in 2004 [80, 81]. This technique allows for the manipulation of micrometer-sized thin film materials and thin film devices and enables the transfer of these thin film materials/devices in a massively parallel manner from a source substrate to a target substrate with high alignment accuracy ($\pm 1.5\,\mu\mathrm{m}$ ($3\,\sigma$) in high throughput and better than $\pm 0.5\,\mu\mathrm{m}$ in individual coupon placement) . It is a fast process where each printing cycle takes 30 to 45 seconds. As the material coupons/devices can be pre-fabricated in dense arrays on a III-V wafer, the efficiency of the usage of the expensive III-V epitaxial material is significantly improved. On the other hand, μTP also allows for the intimate integration of different materials/devices on a single chip, as depicted in Fig. 1.8. Moreover, this integration requires no modification of the Si photonics back-end process flow, except for a local back-end opening where the devices need to be integrated. Fig. 1.9 shows an example of a complex III-V-on-Si integrated PIC realized using μTP. This PIC consists of two micro-transfer-printed tunable lasers with thermally tunable micro-ring filters and an array of germanium (Ge) PDs. Similar to the flip chip assembly, μTP allows for pre-testing of the devices on its native substrate prior to their integration on a target Si PIC wafer. Compared to wafer bonding, in which the thick substrate (e.g. a 500 micron thick InP or GaAs substrate) is consumed in the III-V bonding process, μTP provides the possibility of recycling the III-V substrate, which not only leads to a cost reduction, but also makes the III-V-on-Si integration more eco-friendly. Moreover, this technique is compatible with a wide range of materials. In fact nearly all the material systems/devices that can be released from their native substrate can be transfer printed. Due to the versatility and its potential for high-volume production of complex and ultra-compact PICs and EICs at low cost, μTP has attracted a lot of attention in re-

cent years. In 2012, J. Justice, *et al.* from Tyndall National Institute demonstrated the wafer-scale integration of GaAs FP lasers on a Si substrate through μTP. This integration is realized by first transfer printing an array of III-V material coupons on a target Si substrate and the post-processing of the III-V lasers on the Si target wafer [82]. In the same year, H. Yang, *et al.* from Dongguk University reported a transfer-printed stacked nanomembrane laser on a Si substrate. This laser is optically pumped and operates in the 1550 nm wavelength range [83]. Following the strategy adopted by J. Justice, an optically pumped III-V-on-Si integrated LED was demonstrated by A. De Groote, *et al.* from Ghent University [84]. A III-V taper structure that is patterned in the printed III-V material coupon through a contact UV lithography with a high alignment accuracy (< 300 nm) is used to realize an efficiently optical coupling to the underlying Si waveguide circuits. In 2018, J. Juvert, *et al.* successfully transfer-printed pre-fabricated etched facet Fabry–Pérot lasers on an SOI substrate. The laser facet is butt-coupled to the Si waveguide circuit via a Si spot size converter [85].

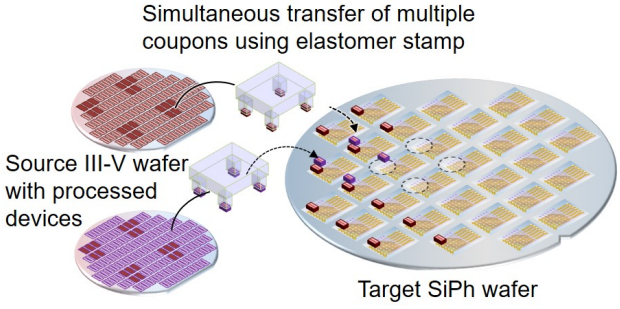

Figure 1.8: Schematic of μTP-based integration on 200 mm or 300 mm Si photonic wafers in a parallel manner.

1.5.3.1 Operation principle

The μTP process relies on the rate-dependent adhesion strength of the to-be-transferred object to the elastomeric stamp (Fig. 1.8). When picking up an object, the peeling velocity has to be sufficiently high such that the adhesion strength of the object to the stamp overcomes the one to its native substrate so that the object can be picked up. To print the object on a new substrate, the retraction of the stamp has to be performed slowly. In this case the adhesion strength of the object to the stamp is weaker that the one to the target substrate so that the object can be released from the stamp and stays on the target substrate.

This rate-dependent adhesion strength of an object to the elastomeric stamp is

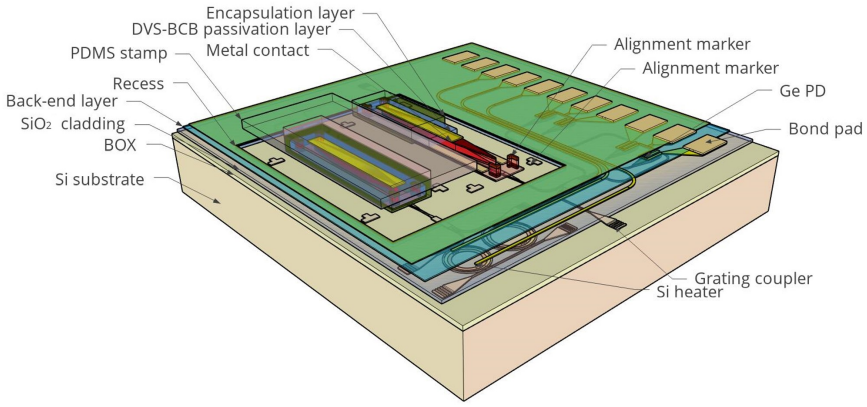

Figure 1.9: An example of the integration of III-V-on-Si lasers on a complex Si PIC, only requiring a local opening of the back-end stack and a post-printing electrical connection between the III-V opto-electronic devices and the Si PIC.

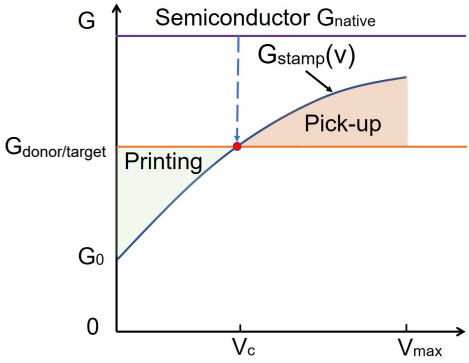

Figure 1.10: Schematic illustrating rate-dependent pick-up and release behavior. Reproduced from [86]

represented by the separation energy:

$$G_{stamp}(v) = G_0(1 + (v/v_0)^n) \tag{1.1}$$

where G_0 denotes the separation energy with peeling velocity approaching to zero. v is the peeling velocity and v_0 is the peeling velocity at which the separation energy equals to $2G_0$. n is a scaling number that is obtained by fitting the experimental data. Given a rigid nature of the object and both the substrates, the separation energy of the object to the native substrate (G_{donor}) and to the target substrate G_{target} is not dependent on the peeling velocity. In case that the donor substrate

and the target substrate have the same surface properties (or have equal separation energy for the device), this separation energy has to be within the range of G_0 and $G_{\upsilon_{max}}$ to allow the pick up and printing of the device, as illustrated in Fig. 1.10. There is a critical velocity at which $G_{donor/target}$ equals to G_{Vc}. It is expressed as:

$$\upsilon_c = \upsilon_0((G_{donor/target} - G_0)/2)^{(1/n)} \tag{1.2}$$

It is clear that the pick-up occurs when $\upsilon > \upsilon_c$ and the printing occurs when $\upsilon < \upsilon_c$. In reality a device (e.g. a III-V device/material coupon) is often transfer printed from its native substrate (e.g. InP or GaAs substrate) to a new substrate (e.g. Si wafer) with different surface properties, therefore G_{donor} is not equal to G_{target}. It needs to satisfy $G_{donor} < G_{\upsilon_{max}}$ and $G_{target} > G_0$ to allow the pick-up and transfer printing, respectively. Directly picking up a thin III-V film / device from its substrate is impossible, due to the strong interface between the stack layers. In order to release the III-V material coupon/device from the native substrate, a sacrificial layer is incorporated between the III-V device layer and the substrate, which can be selectively etched, while using an anchor/tether system to keep the devices in place. This reduces the semiconductor G_{native} below the $G_{\upsilon_{max}}$ such that the predefined material coupon/device can be picked up from the substrate. The G_{donor} can be varied by using a different number of tethers (or tethers with different mechanical strength).

Fig. 1.8 shows a schematic of the μTP process. An elastomeric (PDMS) stamp is used to pick up and transfer these devices from the source wafer onto a new target substrate. The stamp is prepared by casting PDMS on a Si master mold defining post arrays (or a single post) whose size and pitch match those of the device arrays that have been defined on the source wafer. The stamp is then released from the Si master and is laminated on a transparent carrier (glass) wafer. As indicated in Fig. 1.11, devices are patterned on the III-V source wafer and are protected with an encapsulation layer (typically a photoresist layer in the case of III-V devices) with local openings to access the release layer. Then the release layer is undereteched to maintain the registration of the III-V devices during and after the release process. For pick up from the native substrate, the PDMS stamp is first aligned and laminated to the desired device/device array and is then pulled back at a high velocity. This results in a relatively high adhesion strength of the device to the stamp, thereby breaking the tethers. The device or device array is then aligned to and printed on the target wafer by laminating the stamp to the target wafer and slowly retracting the stamp. This results in a low adhesion strength between the devices and the stamp and leaves the device together with the encapsulation layer attached to the Si photonics target wafer (either using Van der Waals forces [82] or with an adhesive bonding agent [84]). The alignment is realized by locating the center of the co-designed fiducial marks on both the source device and the tar-

get substrate -as seen through the transparent PDMS stamp— through a pattern recognition function. ± 1.5 µm 3σ alignment accuracy is achieved when printing devices in large arrays. Better alignment accuracy can be achieved by reducing the size of the array. The final processing steps on the Si target wafer consist of removing the encapsulation and electrically connecting the III-V opto-electronic components to the rest of the PIC.

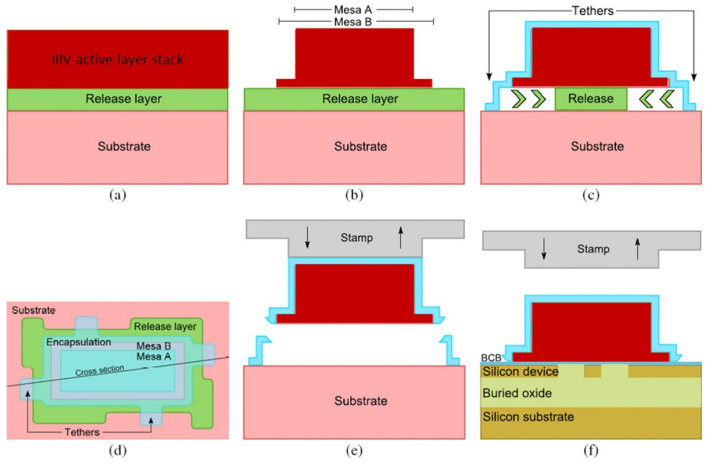

Figure 1.11: Prefabrication of III-V devices on their native substrate and the µTP integration sequence. Reproduced from [87]

1.5.4 Hetero-epitaxial growth of III-V

Monolithic integration of III-V semiconductors on a Si substrate through hetero-epitaxial growth is recognized as the ultimate solution, as it allows for wafer scale processing and high density integration. However, it is quite challenging to grow high quality III-V epitaxial layer stacks on a Si(001) substrate, due to their different material properties, such as large lattice mismatch, polar vs non-polar surface and different thermal expansion coefficients. The defects include anti-phase boundaries, threading dislocations and misfit dislocations. By using a Si(001) substrate with a slight off-cut (typically $4°$) towards the (011) plane and a thick GaAs buffer layer, the anti-phase boundaries can be significantly suppressed [88]. Various O-band devices with moderate performance have been demonstrated via this approach [89]. The use of off-cut substrates was later circumvented by a two-step growth of the GaAs buffer [90]. Alternative solutions include the use of GaAs-on-V-Grooved Si [91, 92], InP-on-V-Grooved Si [93] and the use of a GaP template [94]. So far however no coupling to a waveguide circuit was demonstrated, nor the incorporation of such lasers in a silicon photonics process flow.

To decrease the distance between the III-V device layer and the Si waveguide layer, methods based on selective area growth were proposed. In 2015, Z. Wang *et al.* demonstrated optically pumped InP DFB nanowire lasers around a wavelength of 925 nm, where the InP was selectively grown in predefined V-groove Si trenches with exposed <111> planes. Optically pumped nano-lasers with emission at a longer wavelength were later demonstrated by adding multiple quantum well layers in the III-V layer stack [95, 96]. Moreover, Y. Shi from Ghent University also proposed an electrically pumped nano-ridge DFB laser design and an adiabatic coupler for the optical coupling from the nano-ridge laser to the Si waveguide [97]. However promising, this is still at an early stage, with much work to be done on the integration of these process modules in the SiPh process flow and demonstrating the reliability and performance of the resulting devices.

1.6 Research objectives

This PhD thesis focuses on the realization of III-V-on-Silicon Photonic receivers/-transceivers via μTP. This work includes the following aspects:

- The development of the process flow for the pre-fabrication of III-V material coupons/devices on the native III-V wafer, the release and the μTP of these coupons/devices onto target Si photonic chips.
- The demonstration of III-V-on-Si integrated DFB lasers based on μTP. It includes the preparation of the III-V source wafer with pre-defined III-V material coupon arrays, transfer printing of III-V material coupons on SOI substrates, the post-processing of the printed III-V material coupons on Si photonic chips and the characterization of the fabricated devices.
- The demonstration of FTTH transceivers based the μTP of pre-processed O-band III-V photodiodes.
- The demonstration of widely tunable narrow linewidth lasers through μTP. It includes the design of an alignment-tolerant III-V taper structure, the preparation of III-V source wafer with pre-fabricated SOA arrays, transfer printing of III-V SOAs on a Si photonic chip, post-μTP processing, and the characterization of the fabricated tunable lasers.
- The demonstration of a Si photonic integrated coherent receiver (ICR) realized on the imec iSiPP25G platform with an external local oscillator (LO).
- The realization of Si photonic ICRs by micro-transfer printing the III-V LO and PDs on a passive Si photonics platform and demonstrating the integration of III-V SOAs on the imec iSIPP50G platform through μTP.

The research was supported by the H2020 TOPHIT and CALADAN projects and was carried out in the Photonics Research Group (PRG) at Ghent University in collaboration with Tyndall National Institute, which provided the C-band epitaxial materials, and X-Celeprint which provided technical support in the transfer printing development.

1.7 Outline of this thesis

In this Chapter, we reviewed the background of integrated photonics and III-V-on-Si integration. This work aims for the realization of III-V-on-Si integrated receivers/transceivers via μTP.

In Chapter 2, we will focus on the integration of C-band III-V-on-Si distributed feedback lasers through μTP. We will first present a DFB laser design and a standard III-V-on-Si die-to-wafer bonding process flow. Based on that, we designed a III-V epitaxial layer stack that is suitable for μTP-based III-V-on-Si integration. The development of the process flow for the pre-definition of the III-V coupon array on the native substrate, the release and the transfer printing of these material coupons is described. After that, we described the fabrication and characterization of the DFB lasers.

In Chapter 3, we will present two different FTTH transceivers based on μTP of pre-fabricated O-band III-V PDs. We will start with the development of the process flow for the pre-fabrication, release and μTP of O-band III-V PDs. The second section of this chapter deals with the demonstration of the FTTH transceiver array. The Si PICs with integrated Si microring modulators are realized on the imec iSiPP25G platform. The upstream receivers are realized by μTP of an array of pre-fabricated O-band III-V PDs over the corresponding fiber grating couplers. The demonstrated transceiver array realized 10 Gbit/s operation for simultaneous up and downstream transmission. In the third section, we will present the fabrication and characterization of a single channel FTTH transceiver on the imec 400 nm Si photonics platform. The downstream transmitter is a directly modulated III-V-on-Si DFB laser, which is demonstrated in Chapter 2, and the upstream receiver is a grating-assisted O-band PD. This transceiver also realized 10 Gbit/s operation.

Chapter 4 deals with the realization of III-V-on-Si widely tunable and narrow linewidth lasers. Prior to the laser demonstration, we first review some essential building blocks that have been demonstrated in the imec 400 nm photonics platform to realize these lasers. To verify the feasibility of the use of these existing building for the realization of widely tunable lasers, a fabrication via DVS-BCB adhesive die-to-wafer bonding is first performed. The fabricated devices show over 40 nm tuning range with below 1 MHz linewidth over the entire tuning range. The second part of this chapter deals with III-V-on-Si tunable and narrow linewidth lasers based on μTP. An alignment tolerant III-V/Si taper structure is

designed to accommodate the alignment accuracy (± 1.5 µm, 3σ) that can be obtained by the µTP system (X-celeprint µTP-100 tool). A III-V source substrate with pre-fabricated SOA arrays is fabricated for the µTP based laser integration. The demonstrated laser shows 48 nm wavelength tuning and minimal linewidth of 300 kHz.

In Chapter 5, we will present the progress that we have made towards the realization of Si photonics ICRs with integrated LO. Two approaches are proposed with one based on a passive SOI substrate with 400 nm thick Si device layer and the other one based on the imec iSiPP50G platform. This chapter starts with a brief introduction of the principle of coherent detection and the basic configuration of an ICR. The second section of this chapter focuses on the realization of an ICR on an Ebeam written passive SOI waveguide circuit. This ICR consists of a pair of transfer-printed C-Band III-V PDs in a balanced configuration and a transfer-printed III-V-on-Si tunable laser as LO. The demonstrated standalone components were found to be working well, but a high optical loss was observed in the waveguide circuits, resulting a failure for this ICR. Next, we will present the design of a Si ICR on the imec iSiPP25G photonic platform. First an ICR consisting of a pair of high speed Ge balanced PDs and a 90 degree hybrid is presented. It was co-integrated with a 4 channel linear transimpedance amplifier(TIA) array and an external narrow linewidth laser is used as LO. Operation at 28 Gbaud/s QPSK and 16-QAM are demonstrated. After that, we will design an ICR with integrated LO on the imec iSiPP50G platform. The µTP of pre-fabricated III-V SOAs on the iSiPP50G platform will be demonstrated.

In Chapter 6, we will summarize the work of the thesis and present a discussion of the future work.

1.8 Publications

1.8.1 Publications in international journals

1. B. Haq, J. Rahimi Vaskasi, J. Zhang, Agnieszka Gocalinska, Emanuele Pelucchi, Brian Corbett, G. Roelkens, "Micro-transfer-printed III-V-on-silicon C-band distributed feedback lasers", Optics Express, 28(22), pp. 32793-32801 (2020).

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1.8.2 Publications in international conferences

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1.8.3 Publication in national conferences

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2

Micro-transfer-printed III-V-on-Si DFB laser

In this chapter, we aim to develop a process flow for the integration of III-V-on-Si distributed feedback lasers (DFB) lasers based on the micro-transfer-printing (μTP) of III-V material on Silicon Photonic Integrated Circuits (Si PICs). Following the success of the DVS-BCB adhesive bonding technique and based on the standardized post-processing flow developed in the cleanroom at Ghent University, here a straightforward integration strategy by combining the advantages of the μTP and DVS-BCB adhesive bonding technologies is proposed. This approach exhibits significant improvement in efficiency of the use of III-V materials and allows for wafer-scale integration. This chapter starts with a brief introduction of the optical design of the III-V-on-Si DFB laser, followed by a short description of the standard process flow of the laser fabrication through die-to-wafer bonding. In the second section, we present the integration of III-V material on Si PICs through the μTP technique, which includes the definition of the III-V coupon arrays on the native InP substrate and, the μTP of these coupons to a target SOI chip. The third section presents the development of the post-processing for the DFB laser fabrication, and the performance of the fabricated devices. The Si PICs used in this work are realized on a passive photonic platform with a 400 nm thick Si device layer, fabricated at imec. The III-V epitaxial materials are provided by Tyndall, while the process-flow was developed in Ghent University cleanroom.

2.1 III-V-on-Si DFB laser

The term 'LASER' is the abbreviation of 'Light Amplification by Stimulated Emission of Radiation,' which defines the operation principle. Generally speaking, a laser requires three essential elements: pump mechanism, gain material, and resonant cavity. The gain material works as a power converter (e.g. converting the pump current to photon flux) meanwhile amplifing the incident optical signal through stimulated emission. Besides that, a feedback mechanism introduced by a resonant cavity is necessary. Once the gain balances the loss of the cavity, lasing starts. In the case of the III-V-on-Si integrated lasers, the integrated III-V material provides the optical amplification. It can be pumped either optically or electrically, although the latter case is preferable. The laser cavity can be a standing wave cavity built with a pair of mirrors, e.g., highly reflective interfaces [1], loop mirrors [2], DBR gratings [3], with the gain section in between, or a ring-shape cavity [4]. The laser cavity defines the longitude modes, however,when broadband mirrors are used decent side mode suppression ratio can not be achieved. Therefore narrow band filters, such as a micro-ring resonators [4–6] or DBRs are usually incorporated in the laser cavity to select a single longitudinal mode.

Amongst the different laser types, DFB lasers exhibit superior features including compact size, low cost, high power efficiency and the potential for high-speed direct modulation, making them good candidates for being applied as optical sources or as transmitters in short-reach communication systems, e.g., access networks [7–9] and inter- and intra-datacenter optical interconnects [10–12].

Instead of connecting discrete mirrors or optical filters on a waveguide platform, the optical feedback in the DFB laser is provided by a periodic variation of the refractive index along the gain section, a Bragg grating. In a III-V-on-Si DFB laser, this Bragg grating is usually defined in the Si layer. The first electrically pumped heterogeneously integrated III-V-on-Si DFB laser was demonstrated by Alexander W. Fang via low temperature wafer bonding [13] in 2008. The laser exhibited single-mode continuous-wave operation with 50 dB side mode suppression ratio (SMSR) at 1600 nm. The maximum output power was over 5 mW at $10\,^{\circ}\mathrm{C}$. As the optical mode is mainly confined in a 700 nm thick Si layer, leaving a small portion of optical field in the III-V active region, this laser is also called an evanescent III-V-on-Si laser. This concept was also adopted by S. Stankovic from Ghent University in his DFB laser demonstration, but based on the DVS-BCB adhesive bonding technique [14]. Later S. Keyvaninia *et. al.* proposed and demonstrated a III-V-on-Si DFB laser, where the Bragg grating is patterned on a 400 nm thick Si layer, showing high optical confinement in the III-V active region [15]. This laser operated around 1550 nm and the waveguide-coupled output power was up to 14 mW with 50 dB SMSR. Following these successes, many high-performance III-V-on-Si DFB lasers, including high-speed directly-modulated DFB lasers, have been

developed in the Photonics Research Group at Ghent University [16–21]. Besides the researchers in UCSB and Ghent Unversity, H. Duprez *et al.* from LETI demonstrated III-V-on-Si DFB lasers through the direct bonding technique in 2015. This laser emits at 1310 nm with up to 56 dB SMSR and, the waveguide-coupled power was measured to be 22 mW [22]. High-Q DFBs were also demonstrated by A. Gallet from III-V lab. This laser shows an ultra-low relative intensity noise (-147 dB/Hz over 20 GHz) and 128 kHz intrinsic linewidth [23, 24].

2.1.1 III-V epitaxial materials

III-V compounds that have a direct bandgap are ideal candidates for light generation and absorption. Moreover, their band gaps can be engineered by varying the composition of the semiconductor. Amongst the III-V epitaxial materials, AlGaInAs/InP and InGaAsP/InP are the most commonly used material systems for active devices (e.g., lasers, photodetectors, and modulators) operating in the$1.3\,\mu\mathrm{m}$ to $1.6\,\mu\mathrm{m}$ wavelength range. To improve the performance of lasers, in terms of threshold and high speed performance, epitaxial layer stacks with multiple quantum wells (QWs) sandwiched by barriers rather than bulk materials are usually used. Owing to the larger conduction band offset and smaller valence band offset, AlGaInAs has enhanced electron confinement and thus a reduction of the temperature sensitivity of the threshold current. It also provides higher differential gain, which is beneficial for enhancing the high-speed performance. Therefore this material system is selected for the integration of III-V-on-Si lasers in our work. Table.2.1 lists the information of a classic III-V layer stack with AlGaAsIn QWs for C-band lasers. It consists of a 400 nm thick active region with 6 layers of 6 nm thick AlGaAsIn QW interleaved with 10 nm thick barriers and a pair of separated confinement heterostructure (SCH) layers, a 200 nm thick highly p-doped InGaAs layer for a good ohmic contact, a $1.5\,\mu\mathrm{m}$ thick p-type InP cladding layer, and a 200 nm thick n-type InP layer. 6 quantum wells were chosen as a safe option to be able to demonstrate lasing of transfer-printed devices. In order to further improve the performance of these devices (e.g. threshold current, slope efficiency, bandwidth, linewidth, *et. al.*) the number of quantum wells needs to be further optimized.

2.1.2 Si photonic platform for III-V-on-Si integration

Given the high refractive indices of the quaternary III-V materials (as shown in Table. 2.1), it is challenging to integrate III-V-on-Si devices on a commonly used Si photonic platform with 220 nm thick device layer, unless an ultra-narrow taper tip and/or a thin III-V layer stack is used [25–28]. In order to overcome this issue, Si photonic platforms with thicker Si device layers, *et. al.* 700 nm [13], 500 nm [14, 22, 29] and 400 nm [15, 17], were chosen for the integration of III-V-on-Si devices/circuits.

Table 2.1: Classic III-V laser epitaxial layer stack for bonding based III-V-on-Si integration

Layer	Layer type	Material	Thickness (nm)	Doping level (cm^{-3})	Dopant	Refractive index
22	N contact	InP	200	1×10^{18}	Si	3.169
21	Transition	$(Al_{.9}Ga_{.1})_{.47}As_{.53}In$	40	Si		3.224
20	SCH	$(Al_{.7}Ga_{0.3})_{.47}As_{.53}In$	75			3.278
9×6	Barrier	$(Al_{.35}Ga_{0.65})_{.51}As_{.49}In$	10			3.385
8×6	QW	$(Al_{.25}Ga_{0.75})_{.3}As_{.7}In$	6			3.629
7	Barrier	$(Al_{.35}Ga_{0.65})_{.51}As_{.49}In$	10			3.385
6	SCH	$(Al_{.7}Ga_{0.3})_{.47}As_{.53}In$	75			3.278
5	Transition	$(Al_{.9}Ga_{.1})_{.47}As_{.53}In$	40			3.224
4	Cladding P	InP	500	$\sim 1\times10^{17}$	Zn	3.169
3	Cladding P	InP	1000	$\sim 1\times10^{18}$	Zn	3.169
2	P contact	InGaAs	100	$\sim 1\times10^{19}$	Zn	3.6
1	P contact	InGaAs	100	$> 1\times10^{19}$	Zn/C	3.6

In this work, a waveguide platform consisting of a 400 nm crystalline Si device layer on a $2\,\mu m$ thick buried oxide layer is used for the laser demonstration. The waveguide circuits are fabricated through 193 nm deep UV lithography, and a 180 nm single etch step using dry etching. The resulting waveguide structure is planarized using a SiO_2 chemical mechanical polishing (CMP) process down to the Si device layer.

2.1.3 III-V-on-Si DFB laser design

To date, a wide variety of heterogeneously integrated lasers have been demonstrated on different Si photonic platforms based on different techniques. These lasers can be divided into two major categories based on the mode distribution in the III-V/Si hybrid waveguide. The first type of laser is called evanescent laser. In this laser, a relative thick Si device layer is used and the bonding layer is usually very thin [13, 14, 30]. Therefore the transverse optical mode is mainly confined in the Si layer, leaving a small portion of optical field evanescently spreading into the overlaying III-V layers. Due to a low optical confinement factor in the III-V active layers and a weak coupling strength of the Bragg grating, a long laser cavity is usually required to provide sufficient gain to balance the cavity loss. In contrast, for the second type of DFB lasers, the optical mode is mostly confined in the III-V region. This mode distribution can be realized by using a Si waveguide with smaller cross-sectional geometry [15, 22, 31]. Apparently, this design provides a higher optical gain and potentially a shorter device. Moreover, the thickness of the

bonding interface can be above 100 nm, while as a trade-off, a longer adiabatic taper structure is required to ensure an efficient mode conversion. For instance a 185 µm long adiabatic inverted taper structure is used in [15].

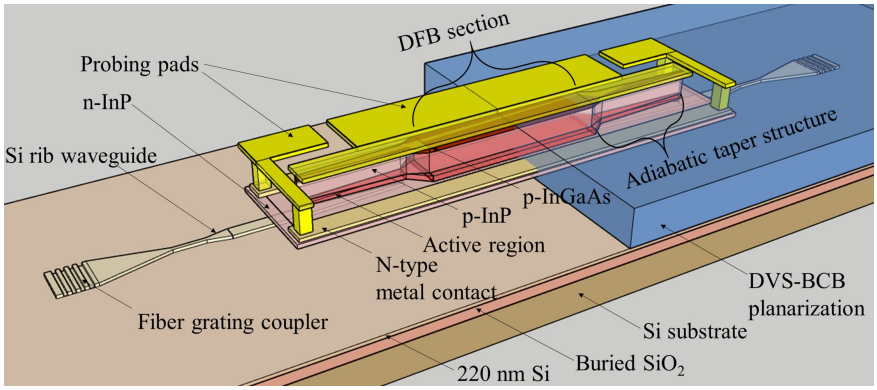


Figure 2.1: Schematic layout of a heterogeneously integrated III-V-on-Si DFB laser

Fig. 2.1 shows a schematic layout of a typical heterogeneously integrated III-V-on-Si DFB laser structure [15]. It consists of a hybrid waveguide structure where a III-V waveguide is overlaid on top of a Bragg grating with a thin DVS-BCB bonding layer in between and a pair of two-level adiabatic inverted taper structures to convert the optical mode to the underlying Si waveguide, which is then terminated with fiber grating couplers (GCs) to interface with optical fibers.

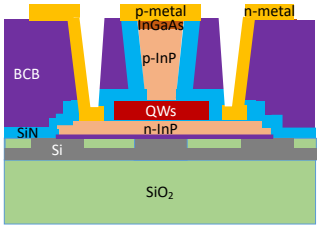


Figure 2.2: Schematic layout of a cross-section of the III-V-on-Si laser

Besides the optical coupling between the III-V layer and Si waveguide, care has to be taken in the design of the hybrid waveguide cross-section. One thing, as already mentioned, is the optical mode distribution on the cross-section of the hybrid waveguide, which greatly determines the strength of the grating and modal gain and thus the performance of the laser in terms of the threshold, output power, high-speed performance *et al.*. The other concern is the non-radiative recombination on the exposed III-V surface. That can significantly degrade the performance

of the lasers, in terms of a higher threshold and poor efficiency, especially for the Al containting III-V materials (e.g., AlGaInAs), as they easily oxidize at room temperature. Surface passivation using $(SH_4)_2$ together with a dielectric encapsulation is verified to be an effective route to address this issue [32–37]. An alternative way to reduce this impact is by confining carriers and photons in a region away from the III-V surfaces. For example, a mesa structure with a wide QW but relative narrower InP mesa can be used for this purpose. Fig. 2.2 shows a schematic cross-section of a classic heterogeneously integrated III-V-on-Si laser based on the technology developed in the Photonics Research Group of Ghent University.

Following the successes in the III-V-on-Si integrated DFB laser demonstrations by our research group, a $3.5\,\mu m$ wide Si rib waveguide is used in our work to pattern the Bragg grating (including a quarter wave shift) on the top of the silicon waveguide. And the InP mesa is designed to be $2\sim3\ \mu m$ wide to confine the current flow as well as the optical mode field in the center of a $6\,\mu m$ wide active region. The bonding of the III-V epitaxial material on the PIC is realized using a thin layer of DVS-BCB adhesive. Beside the widths of laser mesa and the underlying Si waveguide, the thickness of the bonding layer also determines the mode distribution over the cross-section of the III-V/Si hybrid waveguide, providing more flexibility in the laser design. The current bonding techniques already allow for the III-V-on-Si integration with ultra-thin DVS-BCB layers. As reported in [38], a 10 nm thick DVS-BCB bonding layer is used to optimize the optical mode distribution and the coupling strength to achieve a high modulation bandwidth of the DFB lasers. Fig. 2.3 shows the intensity profile of the fundamental TE mode in a hybrid III-V/Si waveguide. As can be seen, most of the optical power is confined in the Si rib waveguide and a small fraction of the optical power spreads into the III-V layer. Fig. 2.4 shows the simulated optical mode profiles for a hybrid waveguide with a DVS-BCB bonding layer of 10 nm, 40 nm, 70 nm, and 100 nm, respectively. The width of the InP mesa and the active region are set to be a $2.5\,\mu m$ and $6\,\mu m$, respectively, in the simulation.

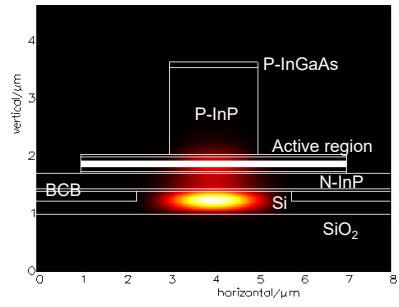


Figure 2.3: The electric intensity profile of the fundamental optical mode in the hybrid III-V/Si waveguide

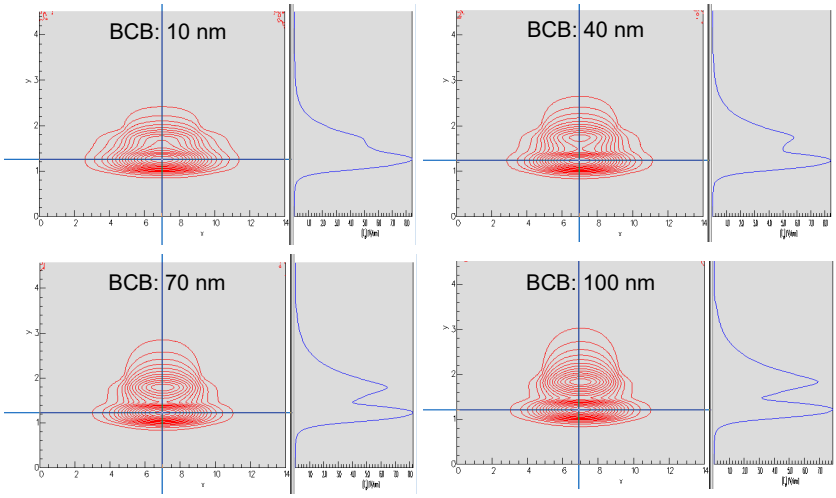
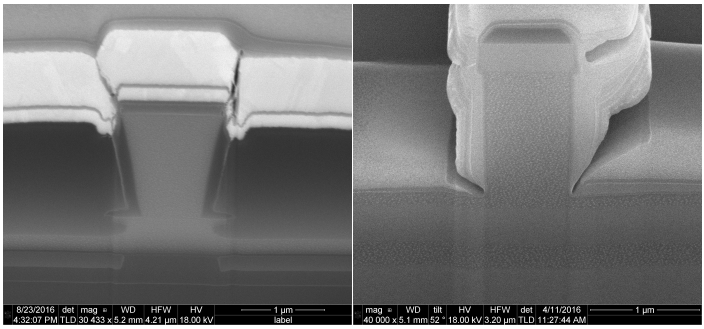


Figure 2.4: Lateral electric field distribution of the fundamental optical mode with different DVS-BCB thickness.

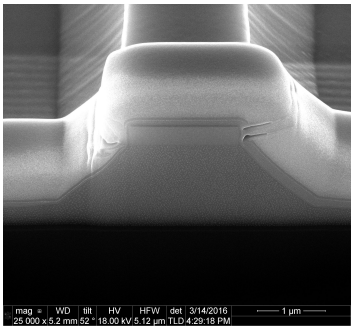
2.1.4 Coupling between III-V and Si

As already discussed an adiabatic taper structure is needed to realize an efficient mode conversion. As the schematic layout shows in Fig. 2.1, the lasing mode emitted from the DFB laser cavity first travels through a III-V waveguide, whose dimensions are the same as those of the laser body but without underlying Si rib waveguide. Since the cross-section of the III-V waveguide is large and so the mode field, a short III-V taper is first used to reduce the width of the mode profile. The coupling occurs in the second section where the III-V is gradually tapered down to a narrower cross-section, while the Si rib waveguide is inversely tapered. Here, two factors need to be taken care of. One is that the index difference between the fundamental mode in the uncoupled III-V and Si waveguides at the ends of the taper has to be sufficiently large so that the optical modes can be decoupled and the fundamental mode is confined in the waveguide with higher effective index. That means narrow taper tips are required in both of the III-V and Si layer. In the taper, the mode field gradually shifts from one waveguide to the other and eventually is fully confined in the neighboring waveguide. To achieve this a long taper with gradually narrowed cross-section is needed to achieve adiabatic coupling.

As mentioned above, the Si PICs are fabricated in the CMOS pilot line at imec using 193 nm deep UV lithography, which allows for structures with a minimum feature size around 200 nm. As the post-processing was carried out at Ghent University, the III-V taper tip is limited to 700 nm width by using 320 nm contact optical lithography. Fortunately, with the help of HCl based anisotropic wet etch-



(a) (b)



(c)

Figure 2.5: Anisotropic etching behavior of InP in HCl based etchant. The long side of the InP mesas is oriented along the direction of (a) $[011]$,(b) $[0\bar{1}1]$, (c) $[00\bar{1}]$.

ing, negative angle sidewalls can be formed along the P-InP mesa structure and thus a much narrower width at the bottom of the mesa can be obtained. To obtain this V-shape cross-section, the III-V waveguide has to be oriented along the $[011]$ direction, otherwise, it will be rectangular or trapezoidal, as shown in Fig. 2.5. As well, a thin QW taper tip can be obtained by careful control of wet undercut etching. Besides the aspects discussed above, the mode coupling behavior is also determined by the thickness of the DVS-BCB bonding layer.

In this section, we study the influence of the DVS-BCB thickness and the width of the III-V taper tip on the coupling efficiency and to decide the shape and length of the taper structure. As shown in Fig. 2.7, the maximal coupling efficiency is determined by the width of the III-V taper tip. When a 400 nm wide III-V taper tip is used in the simulation, the mode conversion is almost lossless. The coupling efficiency dramatically drops to less than 80% when the width of the taper tip is increased to $1.2\,\mu\mathrm{m}$ (as the mode has not fully coupled to the silicon waveguide yet).

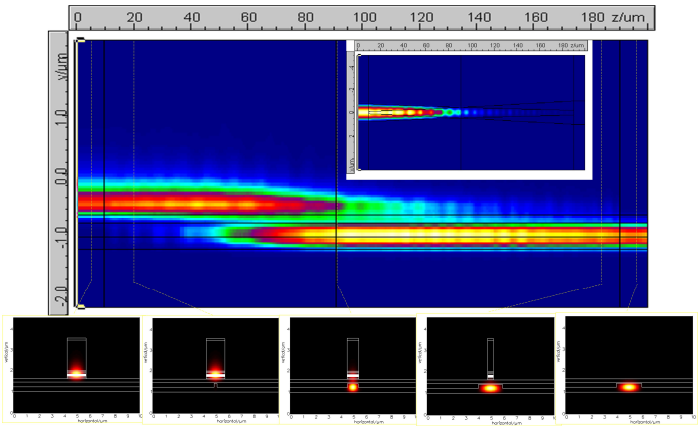


Figure 2.6: Simulated optical mode conversion over the adiabatic taper structure

On the other hand, a long taper is required to achieve adiabatic coupling if a thicker DVS-BCB layer is used. Fig. 2.6 shows a simulated optical mode propagation of the fundamental TE mode through an optimized III-V/Si taper structure.

2.2 III-V Epitaxial layer stack for μTP-based integration

For μTP based integration, in contrast to the III-V epitaxial layer stack dedicated for the bonding-based integration, these epitaxial layers have to be reversely stacked on the substrate(which in this work is InP). Moreover, a sacrificial layer is required beneath the device layers to enable the release of the coupons/devices from the native substrate by selective wet etching. Note that the bottom surface of the released devices will interface with the target substrate, however, with a thin adhesive bonding agent (DVS-BCB in our case) that can relax the requirement for the flatness and smoothness of the interface. As already demonstrated in [39, 40], an InGaAs layer can be used as a sacrificial layer. In the fabrication, a photoresist layer will be used to encapsulate the coupons and to define the tether structures, therefore the etchant should not be aggressive against photoresist. According to the investigation carried out by De Groote *et al.* [39], aqueous $FeCl_3$ behaves the best among several tested etchants, exhibiting a selectivity of 500 to InP at room temperature and an increased selectivity at lower temperature (e.g. over 2000 at 5 °C). The temperature dependence of the selectivity is also reported in [41]. Attributed to such a high selectivity, the bottom layer of the released coupon shows around 15

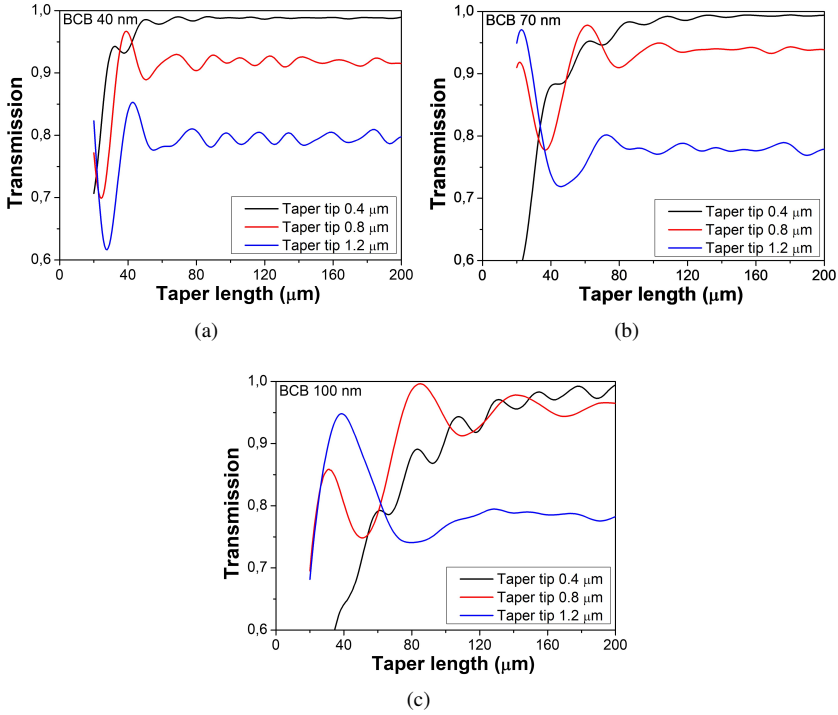
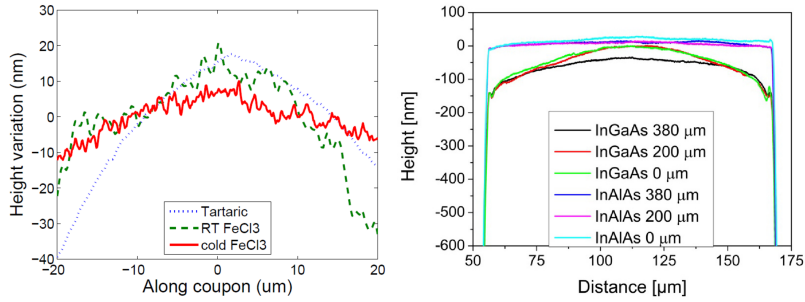


Figure 2.7: Simulated coupling efficiency of the III-V/Si taper structure as a function of taper length,(a) with 40 nm thick DVS-BCB bonding layer,(b) with 70 nm thick DVS-BCB bonding layer, (c) with 100 nm thick DVS-BCB bonding layer.

nm height variation across the $40\,\mu\mathrm{m}$ wide coupon, which is sufficiently flat for the DVS-BCB adhesive bonding, as shown in Fig. 2.8. Similar work was also carried out by Ruggero Loi, *et al.* from Tyndall National Institute, where it was found the etching of InGaAs in aqueous $FeCl_3$ exhibits a significant crystallographic dependence. The etching of InGaAs along the (001) and the (010) crystal planes goes faster, and the selectivity to InP achieves the maximum of 735 at $5\,^{\circ}\mathrm{C}$ [40]. It was found in their work that the etch rate of InGaAs along the $[011]$ crystal direction, and the $[0\bar{1}1]$ crystal direction is similar, around 300 nm/min. To obtain a V-shape cross-section of the InP mesa through HCl based anisotropic wet etching, the III-V coupon is preferably orientated with the long side along the $[\,011\,]$ crystal axis (perpendicular to the major flat of the InP wafer). Further study shows that AlInAs is more suitable for use as a release layer. It exhibits an isotropic underetch with higher etch rate around 1200 nm/min and an improved selectivity of 2900 to InP [42].



(a) (b)

Figure 2.8: Height variation along coupon after undercutting (a) a 1 µm thick InGaAs release layer using different etchant and, (b) different release layers using aqueous $FeCl_3$.

The epitaxial layer stack used for this demonstration is provided by Tyndall National Institute, grown by MOVPE on a (100) oriented InP substrate. As listed in Table. 2.2, it consists of a 200 nm thick highly-doped InGaAs p-contact layer, a 1.5 µm p-InP cladding, a pair of 75 nm InGaAsP SCH layers, a pair of 40 nm AlInGaAs transition layers, an active region with 6 AlInGaAs quantum wells separated by AlInGaAs barriers, and a 200 nm n-InP contact layer with 60 nm intrinsic InP underneath. A 1 µm thick intrinsic InGaAs layer is incorporated as the release layer. A 100 nm thick InP cap layer is deposited on top of the p-InGaAs layer to safeguard it from contamination in the processing. The overall thickness of the III-V layer stack that will be printed onto the target PICs is around 2.3 µm.

2.3 Overview of the fabrication of III-V-on-Si DFB lasers based on the µTP of III-V material

In this section, we present a brief description of the process flow of the integration of III-V-on-Si DFB lasers based on the µTP integration of III-V material in terms of III-V coupons on Si PICs. A description in detail will be presented in the following sections. As shown in Fig. 2.9 the fabrication consists of three major steps: the release of the III-V coupon array from its native substrate, µTP of III-V coupons on the Si PIC, and post-processing in the printed III-V material. Firstly III-V coupons with the desired dimension are patterned on the native substrate in a dense array(Fig. 2.9(a)). The coupons are then encapsulated using a thick photoresist layer with a set of surrounding tethers standing on the substrate where the release material is etched locally(Fig. 2.9(b)). After undercutting the coupons via a selective wet etch process, the coupons are ready for the µTP integration(Fig. 2.9(c)). A

Table 2.2: III-V laser epitaxial layer stack with $1\,\mu m$ thick InGaAs release layer.

Layer	Layer type	Material	Thickness (nm)	Doping level (cm^{-3})	Dopant	Index
26	Cap layer	InP	100	nid		
25	Contact P	InGaAs	100	$> 1\times10^{19}$	Zn/C	3.6
24	Contact P	InGaAs	100	$\sim 1\times10^{19}$	Zn	3.6
23	Cladding P	InP	1000	$\sim 1\times10^{18}$	Zn	3.169
22	Cladding P	InP	500	$\sim 1\times10^{17}$	Zn	3.169
21	Transition	$(Al_{.9}Ga_{.1})_{.47}As_{.53}In$	40			3.224
20	SCH	$(Al_{.7}Ga_{0.3})_{.47}As_{.53}In$	75			3.278
9×6	Barrier	$(Al_{.35}Ga_{0.65})_{.51}As_{.49}In$	10			3.385
8×6	QW	$(Al_{.25}Ga_{0.75})_{.3}As_{.7}In$	6			3.629
7	Barrier	$(Al_{.35}Ga_{0.65})_{.51}As_{.49}In$	10			3.385
6	SCH	$(Al_{.7}Ga_{0.3})_{.47}As_{.53}In$	75			3.278
5	Transition	$(Al_{.9}Ga_{.1})_{.47}As_{.53}In$	40			3.224
4	Cladding N	InP	200	1×10^{18}	Si	3.169
3	Etch stop N	InP	60	2×10^{18}	Si	3.169
2	SAC	InGaAs	1000	nid		
1	Buffer	InP	150	nid		
0	Substrate	InP		n-type		

thin DVS-BCB layer is spin-coated on the PIC chip(Fig. 2.92(d)) as an adhesive bonding agent to ensure a high-quality bonding, as shown in (Fig. 2.9(e)). After a short pre-bake, the PIC and the III-V wafer are loaded in the μTP system for the next operation. As shown in Fig. 2.9(f), the coupons are printed on the areas where the DFB gratings are defined. Then the III-V taper structures are patterned via optical lithography, and a combination of dry and wet etching (Fig. 2.9(f)). After planarizing the III-V mesas (Fig. 2.9(g)), the processing is finished by a definition of metal contact pads via a lift-off process (Fig. 2.9(h) and (i)).

2.4 Definition of coupon array on native substrate

2.4.1 Dimensions of the coupons

As explained before, the cross-section of the III-V/Si hybrid waveguide consists of a $\sim 6\,\mu m$ wide active region and a n-type metal contact about $5\,\mu m$ separated from the active region to prevent short circuit. The n-type metal contacts are designed to be $12\,\mu m$ wide, which together with the laser mesa leads to a minimum required coupon width of $40\,\mu m$. A typical laser structure consists of a Bragg

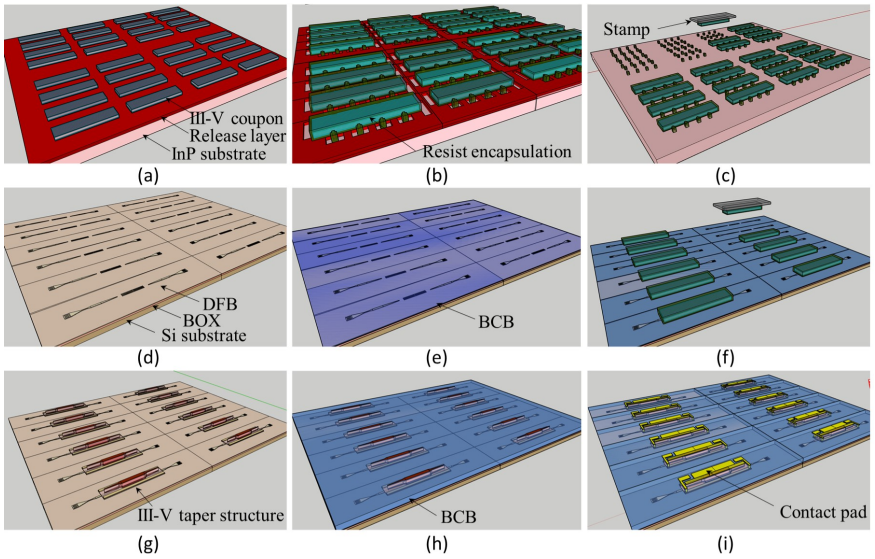


Figure 2.9: Process flow of the III-V-on-Si DFB laser fabrication based on the tranfer printing of III-V material coupons on PIC.(a) Definition of III-V coupon array on source material, (b) Coupon with resist encapsulation and tethers, (c) Picking up the released coupon using a PDMS stamp, (d) DFB grating defined on the 400 nm platform, (e) Spin-coating a thin DVS-BCB layer, (f) µTP III-V coupons onto the target PIC, (g) Definition of the III-V taper structure, (h) DVS-BCB planarization/passivation, (i) Fabricated lasers with metal contact pads.

grating section whose length is typically ranging from $200\,\mu m$ to $600\,\mu m$ depending on the coupling coefficiency of the grating, and a pair of $180\,\mu m$ adiabatic taper structures. The tapers usually are placed $50\,\mu m$ away from the Bragg grating. Therefore the overall length of the III-V structure is ranging from $660\,\mu m$ to $960\,\mu m$. Therefore the width and length of the coupon are decided to be $40\,\mu m$ and $970\,\mu m$, respectively, to satisfy different designs.

2.4.2 III-V coupon definition and release

The release process is described in Fig. 2.10. The III-V coupon is fabricated by first defining the mesa structure through multiple steps of wet and dry etching using a Silicon Nitride (SiN) hard mask – after removing the 100 nm thick InP sacrificial layer (Fig. 2.10(b)). After etching into the n-InP layer, a second mesa is defined, as shown in (Fig. 2.10(c)) using a photoresist mask and dry etching. The release layer is etched through 300 nm into the InP substrate (Fig. 2.10(d)). Then the coupons are encapsulated by a $2.5\,\mu m$ thick photoresist layer patterned in such a

way that the device coupon is protected, the release layer is locally exposed, while also tethers are defined that will anchor the coupon to the substrate during and after release. A top-view of the coupon after photoresist encapsulation is shown in (Fig. 2.10(f)). The under-etching of the InGaAs release layer is performed using an aqueous $FeCl_3$ solution(Fig. 2.10(e)). Detailed fabrication steps developed in the Ghent University cleanroom will be presented in the rest of this section.

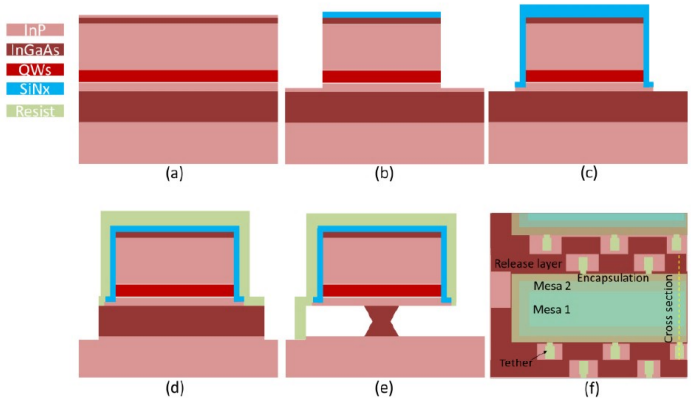


Figure 2.10: Process flow of coupon patterning and release. (a) The initial III-V layer stack, (b) Sacrificial layer removal and first mesa definition, (c) Second mesa definition, (d) Etching of the release layer, (e) Resist encapsulation and under etch of the release layer, (f) Layout of the device coupon after photoresist encapsulation.

According to the designed process flow, four layers of contact masks are required in the fabrication. Fig. 2.11 shows the schematic layout of the contact mask design. The first layer(Mesa-1) is used to define the shape of coupons. The mesa-2 is $2.5\,\mu m$ wider in each direction compared to Mesa-1, resulting a size of $975\,\mu m \times 45\,\mu m$. The third layer with surrounding rectangular teeth is used to expose the substrate, allowing the tethers to sit on the substrate and to anchor the coupons during and after release. The main body of this layer is $5\,\mu m$ wider than the second mesa. The last and also a critical part is the tether design. Rigid tether with good adhesion to the native InP substrate is necessary to anchor the released coupon on the substrate and avoid a collapse after release, while it will result in a failure in picking up if the tether is too strong. Fig. 2.11(b) shows five different tether designs. A big foot is used to enhance the adhesion to the substrate, and a $5\,\mu m$ narrow neck is designed to facilitate the pick-up. While a well-functioning tether design is dependent on the coupon size, topography and stress, it turns out that all five designs used in this design-of-experiment were successful. Next to

the design also the thickness of the tethers plays an important role and needs to be optimized.

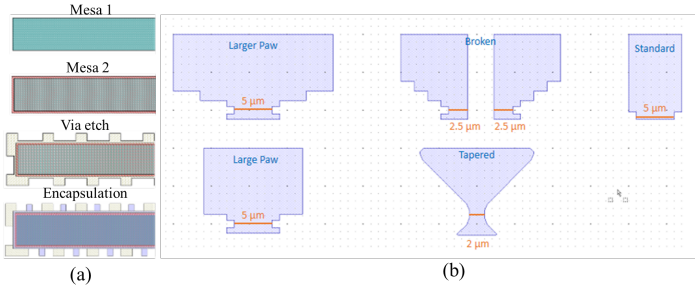


Figure 2.11: Schematic layout of the contact mask design. (a) The coupon definition, (b) Different tether designs.

A piece of III-V material is cleaved from a 2 inch III-V epitaxial wafer for the coupon definition. Before that, a thin photoresist was spin-coated on the wafer to protect the top surface from contamination. Firstly, the III-V die is cleaned through a standard cleaning sequence (Acetone, IPA and DI water), followed by a short wet etching in pure HCl to remove the top InP sacrificial layer. Then a 400 nm SiN layer was deposited in a plasma-enhanced chemical vapor deposition (PECVD) tool as the hard mask to pattern and define the coupon mesa. The deposition is carried out at 270 °C. Note that the SiN deposited with high and low RF frequency show strong tensile and compressive stress, respectively. To strike a balance and obtain a low-stress SiN layer, the RF frequency is alternating during the deposition [43]. Note that the long side of the coupons has to be oriented along the [011] crystal axis to ensure the V-shape cross-section. The shape of the coupon is patterned through a 320 nm optical lithography process using AZ 5214 photoresist. Then an RIE dry etch with a gas mixture of H_2, CF_4 and SF_6 is performed to transfer the pattern to the SiN layer. After removing the photoresist mask, the sample is loaded into an ICP etching tool to etch the p-InGaAs into the p-InP layer. Then a room temperature 1:1 HCl:H_2O solution is used to etch the 1.5 µm thick p-InP layer and stop on the active region. The etch rate of InP is found to be around 120 nm/min in the first immersion, while it decreases dramatically in the second immersion. Therefore a careful topography check is needed to decide whether the etching is finished. When the p-InP is completely removed, the sample is immersed into 1:1:20 H_3PO_4:H_2O_2:H_2O to etch the AlGaAsIn active region. This step takes about 2 minutes. The first mesa definition is completed with a short immersion in 1:1 HCl:H_2O to slightly etch into the n-InP layer. Fig. 2.12 shows a zoom-in microscope image of a group of coupons after the first mesa definition. The bright corners at the coupon ends indicate an undercut of p-InP, resulting from

the HCl anisotropic wet etch.

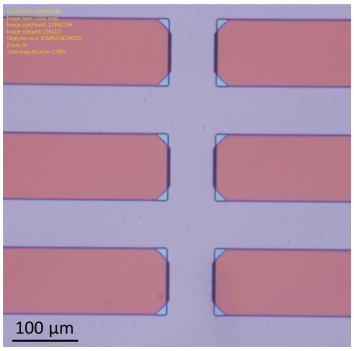
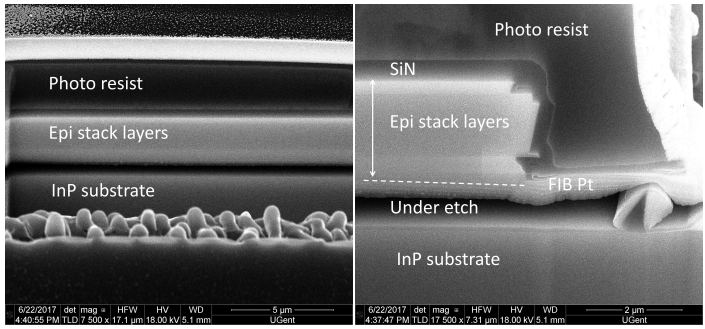


Figure 2.12: A microscope image of a coupon array after the first mesa definition.

The second Mesa definition is similar to the first one. A 200 nm thick PECVD mixed frequency SiN layer is deposited to protect the sidewall of the mesa and, at the same time, it acts as a hard mask to define the second mesa. After the hard mask is patterned, the sample is immersed in a 1:1 HCl:H_2O solution to etch the n-InP and stop on the InGaAs release layer. Note, there is a 60 nm thick intrinsic InP layer beneath the n-InP layer. It was found that the etch rate of the intrinsic InP in 1:1 HCl:H_2O is very slow ($<$20 nm/min), which makes it difficult to decide whether the etching is complete. Fortunately, it does no harm if there is some residual InP.

In the third step, a set of vias will be opened into the InP substrate, where the tethers will sit on and anchor the coupon during and after the release process. Ti 35E photoresist, which provides a $> 3.5\,\mu\mathrm{m}$ thick resist layer by spin coating at 3000 rotations per minute (rpm), is used in the optical lithography. After the contact lithography, the sample is baked at $120\,^{\circ}\mathrm{C}$ for 5 minutes to prevent the photoresist mask from burning in the following residual InP removal by a short ICP dry etching. The sample is then immersed in a 1:1:18 H_2SO_4:H_2O_2:H_2O solution to etch the InGaAs release layer. The etching takes about 4 minutes, after that the sample is again loaded in an ICP tool to etch around 300 nm into the InP substrate. The photoresist mask is removed by sequentially rinsing in Acetone, IPA and water and, a short RIE oxygen-plasma etch to ensure a clean surface.

A $2.5\,\mu\mathrm{m}$ thick Ti35E photoresist layer (spin-coated at a speed of 4000 rpm for 40 seconds) is used to encapsulate the defined coupon and meanwhile define tethers through an optical lithography process. The under-etch of the InGaAs release layer is realized by immersing in an aqueous $FeCl_3$ solution which is bathing in circulating water in a chiller. The chiller is set at $3\,^{\circ}\mathrm{C}$, while the actual temperature of the aqueous $FeCl_3$ solution is measured to be around $7\,^{\circ}\mathrm{C}$. The undercut takes



(a) (b)

Figure 2.13: (a) FIB cross section image showing a suspended coupon, (b) Zoom-in image of the edge of the coupon.

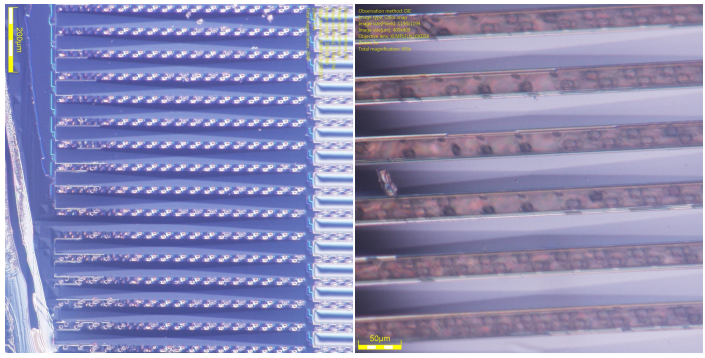
about 8 hours. After the release, the chip is dipped into a beaker of DI water and then rinsed in flowing DI water for a few minutes to get rid of the residual $FeCl_3$. The sample is then gently dried using a N_2 gun.

As the focused ion beam (FIB) cross-section image shows in Fig. 2.13(a), the InGaAs release layer is completely etched away, leaving the coupon suspended over the InP substrate and the sidewall of the coupons(Fig. 2.13(b)), is well protected by the SiN hard mask, which prevents the penetration of $FeCl_3$ to the active region and p-InGaAs contact layer during the release. Fig. 2.14 shows the InP source substrate and the bottom surface of the coupons after a manual pick-up test using a piece of scotch tape. A pyramidal topography is observed on both sides, caused by the limited selectivity of the $FeCl_3$ etch.

2.5 μTP of III-V coupons on the target substrate

A brief overview of the μTP process is described in Fig. 2.15. The stamp is laminated to the source substrate and then accelerating away from the substrate such that the velocity of the stamp is high enough to break the tethers and therefore pick-up the coupons. In the printing process, the stamp with coupons is laminated against the target waveguide circuit - onto which a DVS-BCB bonding layer was spin-coated - such that a good contact and hence a high-quality adhesive bonding is obtained. Then the coupon is detached from the stamp by slowly lifting the stamp after applying a shear force, leaving the III-V coupon attached to the target waveguide circuit.

The first μTP of the III-V coupons was carried out at X-Celeprint. As an initial test, the coupons were directly printed on a glass substrate without DVS-BCB. As shown in Fig. 2.16, most of the coupons are printed on the target substrate



(a) (b)

Figure 2.14: (a) Surface of the InP substrate after picking up an array of coupons, (b) Bottom surface of the coupons picked up using a scotch tape.

except for one failed printing because of the tether debris. Fig. 2.16(b) shows the microscope image from the backside through the glass substrate. The bright region shown in the middle of the coupon indicates an imperfect contact caused by the pyramidal profile of the bottom surface of the InP layer, as already shown in Fig. 2.14. However, with the help of a thin DSV-BCB adhesive layer, high-quality bonding still can be obtained.

For process development purposes III-V coupons are printed on a passive Si PIC which is planarized using SiO_2 down to the Si device layer. This test is carried out in the Ghent University cleanroom. A DVS-BCB: mesitylene 1:6 solution is spin-coated at 3000 rpm for 40 seconds on the Si PIC, followed by a soft bake on a hot plate at $150\,^{\circ}\mathrm{C}$ for 10 minutes and subsequently cooled down to room temperature naturally.

A PDMS stamp with a 1000 $\times$ 60 $\mu\mathrm{m}^2$ post was selected to pick up and transfer print the 970 $\times$ 40 $\mu\mathrm{m}^2$ coupons to the desired locations on the PIC. After the source and target substrates were loaded in the X-Celeprint µTP-100 tool(Fig. 2.17), the source and target stages were carefully mapped such that the devices have the best angular alignment possible. The µTP process was carried out at room temperature. An example of an array of printed III-V coupons is shown in Fig. 2.18(a) before the removal of the photoresist encapsulation. A $40\,\mu\mathrm{m}$ wide tiling free area, showing as the bright bars is used to define the printing area. A cross-section image of the III-V-on-Si coupon at the end and in the middle of the coupon after the photoresist encapsulation removal and DVS-BCB curing are shown in Fig. 2.18(b) and (c), respectively. No air voids or delamination was observed, illustrating the high quality of the bonding interface. As can be seen from

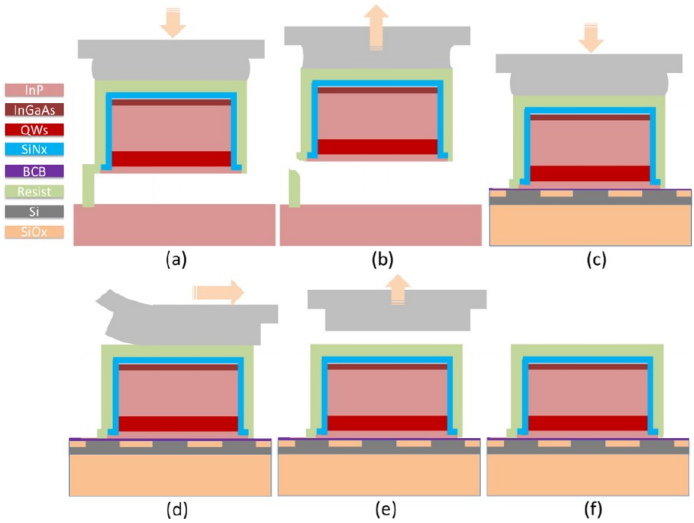


Figure 2.15: μTP of the III-V coupons: (a) Laminating the PDMS stamp to the released coupon on the source substrate, (b) Picking up the III-V coupon by rapidly lifting up the stamp, (c) Laminating the III-V coupon against photonic target substrate with a slight overdrive, (d) Applying a shear force to detach the III-V coupon from the stamp, (e) Lifting up the stamp, (f) The transfer printed III-V coupon on the target photonic circuit.

the cross-sections, the thickness of the DVS-BCB bonding layer is uniform along the integrated coupon. It is mainly because of the use of the elastic PDMS stamp, which makes the pressure uniformly distributed along the coupon when the stamp is laminated against the target waveguide circuit in the printing process. Moreover, it was found that any DVS-BCB:mesitylene solution with a dilution ratio between 1:4 to 1:8 resulted in a 10 nm to 30 nm ultra-thin and uniform bonding layer in the printing test. Not much data exists today on the sample to sample uniformity. This needs to be studied further in order to assess the impact on the grating coupling strength of the resulting DFB lasers.

2.6 First generation DFB laser

2.6.1 Overview of the post-process flow

The process flow of the first generation DFB laser is described in Fig. 2.19. The stack layer of the SOI with transfer printed III-V coupon is schematically shown in Fig. 2.19(a). Firstly, the photoresist encapsulation is removed by RIE oxygen plasma. Then the DVS-BCB bonding layer is fully cured at 270 °C. Note that the exposed DVS-BCB layer is also removed by the oxygen plasma, as indicated in

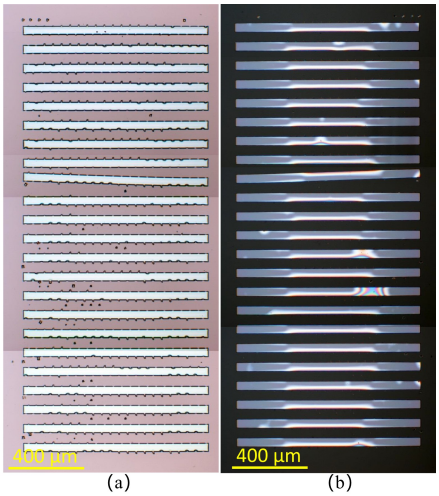


Figure 2.16: µTP of the III-V coupons on a glass substrate.(a) Top-view of an array of transfer-printed coupons,(b)A microscope image from the backside through the glass substrate

Fig. 2.19(b), leaving the Si waveguides exposed. Therefore, a DVS-BCB layer is spin-coated on the sample to cover the exposed waveguide circuits. Then an RIE dry etch is performed to thin down the DVS-BCB layer and the SiN hard mask layer to expose the InGaAs contact layer Fig. 2.19(c)). Again, a SiN layer is deposited and patterned using 320 nm UV lithography as a hard mask to define the laser mesa and taper structures, accurately aligned (<300 nm [44]) to the underlying Si waveguide circuit. A combination of ICP dry etching and HCl-based wet etching is used to form the V-shape waveguide cross-section (Fig. 2.19(d)). In this fabrication the QW is patterned with a resist soft mask and is etched by immersing in a 1:1:20 H_3PO_4:H_2O_2:H_2O solution. A Ni/Ge/Au metal stack layer is deposited on the n-InP layer at sides of the laser mesa through a lift-off process, as shown in the Fig. 2.19(e). After exposing the AlInGaAs active region to H_2SO_4:H_2O_2:H_2O and 1:10 BHF:H_2O to remove the surface oxides, 50 nm room temperature SiN together with a thick normal temperature SiN are deposited to passivate the active region (Fig. 2.19(f)). The device structure is then planarized using a thick DVS-BCB layer and etched back (together with the SiN) to expose the InGaAs contact layer for Ti/Au metal deposition (Fig. 2.19(g)). After opening the via to reach the n-contact metal(Fig. 2.19(h)), the process is finished by a thick Ti/Au deposition (Fig. 2.19(i)).

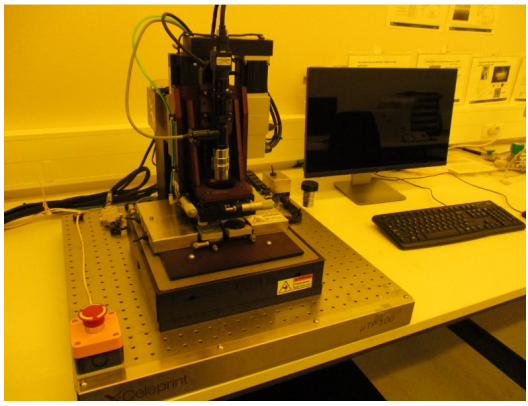


Figure 2.17: µTP-100 µTP system.

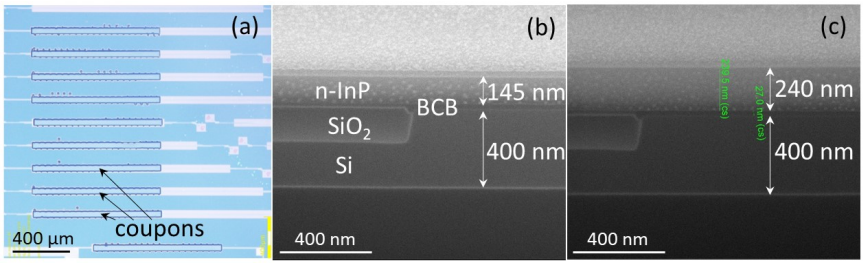


Figure 2.18: (a) Array of printed III-V coupons on a Si PIC (before photoresist encapsulation removal). (b) Cross section image at end of the coupon; (c) Cross section image in the middle of the coupon.

2.6.2 µTP of III-V coupons on photonic circuits

The Si waveguide circuit is fabricated at imec using 193 nm deep UV lithography. It consists of a 400 nm Si device layer on a 2 µm thick buried oxide layer, etched 180 nm to define the waveguide structures and planarized using SiO_2 down to the Si device layer through a chemical mechanical polishing (CMP) process. After fabrication, the SOI wafer is post-processed in the Ghent University cleanroom. As the received SOI wafer was not diced, the first task is to dice out the desired part. Before that, a thin layer of photoresist is spin-coated on the wafer to protect the PICs from contamination, especially from the particles created during dicing. The size of the dies used for this demonstration is 1.5×2.5 cm^2. The SOI dies together with a few bare Si dies for dummy tests are then delivered to X-Celeprint for the µTP of the III-V coupons. The SOI chip with transfer-printed III-V coupons is shown in Fig. 2.20(a). The first step is to remove the resist encapsulation layer. As the DVS-BCB bonding layer has not been cured yet, an RIE oxygen plasma

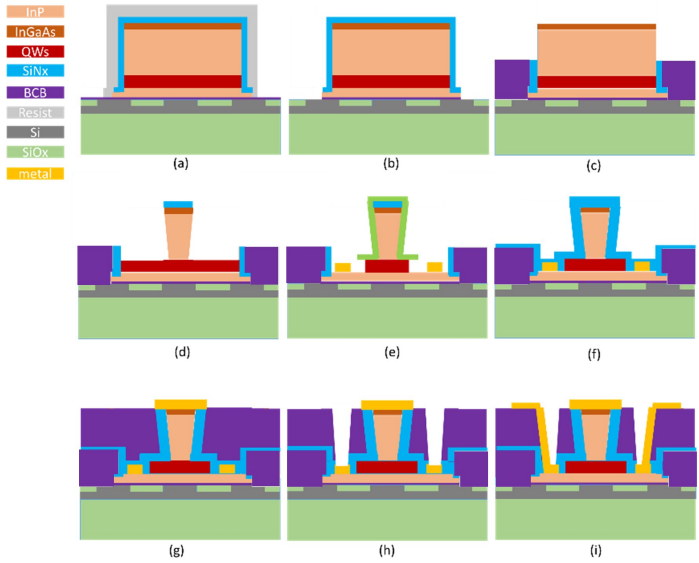


Figure 2.19: Schematic illustration of the post-process flow of the III-V mesa structure in the μTP coupon

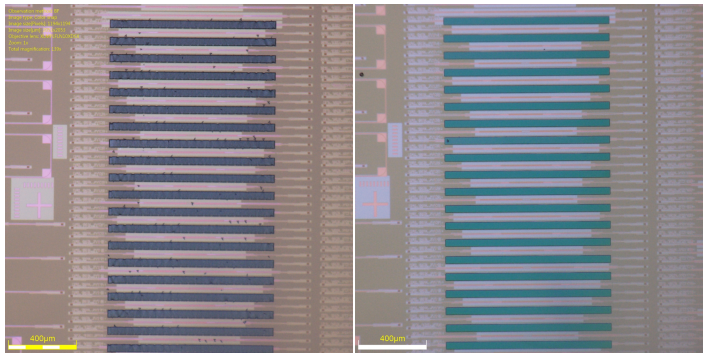
etching is preferable in this step. The DVS-BCB layer is cured in an oven through a standard curing procedure, which includes a slow ramping from room temperature to 270 °C. After stabilizing at 270 °C for 1 hour the temperature slowly drops to room temperature. Fig. 2.20(b) shows the sample after DVS-BCB was fully cured.

2.6.3 Post-processes

This fabrication follows the process flow described in Fig. 2.19. Several issues came up during the fabrication, which resulted in failed devices. These issues and the suspected reasons for them will be discussed.

2.6.3.1 Si waveguide circuit protection

As discussed before, the Si waveguide circuit is exposed after removal of the photoresist encapsulation layer. Therefore a protection layer is needed in the following processes. For this purpose, pure DVS-BCB (CYCLOTENE 3022-46) is spin-coated at 2000 rpm for 40 seconds on the sample, followed by a curing procedure at 270 °C. The thickness of the resulting DVS-BCB protection layer is around 3.8 μm. Then the DVS-BCB layer and the SiN hard mask on the coupon are subsequently removed in an RIE tool to expose the InP sacrificial layer. Fig. 2.21 shows a microscope image of the sample after DVS-BCB and SiN etch back. The



(a) (b)

Figure 2.20: Si photonic circuit with an array of transfer-printed III-V coupons.(a)Before resist encapsulation removal,(b)After resist encapsulation removal and DVS-BCB curing.

colorful fringes around the coupon array result from the topography of the DVS-BCB protection layer, indicating a thicker DVS-BCB layer over the device region.

2.6.3.2 Mesa definition

Firstly the InP sacrificial layer is removed by immersing in pure HCl for 20 seconds. The shape of the InP mesa is patterned in a 300 nm thick SiN hard mask via optical contact lithography with MIR 701 photoresist which allows for a minimum feature size of 700 nm under a good vacuum contact condition. Fig. 2.22(a) shows the sample with patterned SiN hard mask. Then the sample is immersed in a 1:1 HCl:H_2O solution to define the p-InP mesa. It exhibits significant crystallographic dependence in this wet etching, as the microscope image shows in Fig. 2.22(b) and Fig. 2.22(c) and the p-InP etching at the ends of the coupons goes very slow. The etching was stopped with a bit p-InP left at the ends of the coupons to avoid a deep undercut in the mesa taper. Fig. 2.22(d) shows the coupons after the p-InP mesa definition. A distinct topography is observed at the ends of the coupons, indicating an undercut of n-InP in this step.

2.6.3.3 Active region definition

The QWs active region was defined using a $7\,\mu\mathrm{m}$ thick photoresist soft mask (such a thick mask was initially chosen to make sure the III-V mesa is covered, in a later stage, the thickness of the resist was reduced to $1.7\,\mu\mathrm{m}$). After lithography, a 3 minutes soft bake at $120\,^{\circ}\mathrm{C}$ is performed to prevent the photoresist from being

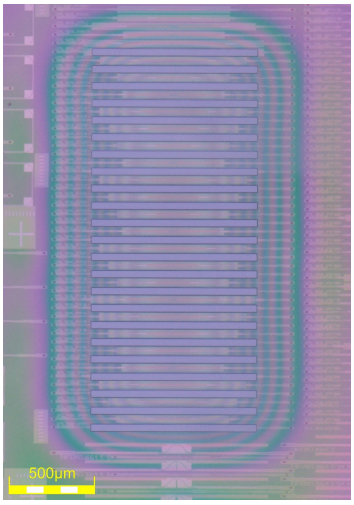
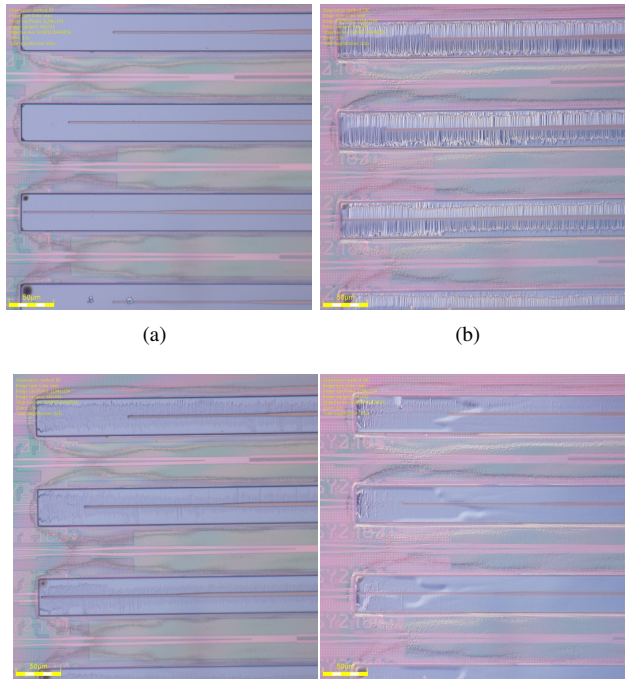


Figure 2.21: Microscope image of the sample with a DVS-BCB protection layer.

damaged in the following processes. A few cycles (usually 3 or 4 cycles) of ICP etching is performed to remove the residual p-InP and expose the AlGaAsIn active region. As the p-InP left at the coupon ends is too thick to be completely removed, it might result in external feedback to the laser. After ICP dry etching, the QW layers are etched down in a 1:1:20 H_3PO_4:H_2O_2: H_2O solution, which provides an etch rate of 200 nm/minute. The active region includes the SCH, QWs, and barriers, having an overall thickness around 400 nm. Therefore this wet etching takes about 2 minutes. A profilometer can be used to trace the etching progress by measuring the topography. Once the step shows no obvious variation anymore, the active region is completely etched. Usually, a short over-etching is performed to introduce some lateral undercut to narrow down the tapers. A microscope image of the sample after the active region definition (with photoresist mask) is shown in Fig. 2.23. The dark blue area at the coupon ends indicates the undercut of n-InP in previous p-InP mesa definition. When the QW definition is complete, the photoresist is removed through a standard cleaning procedure and a short RIE oxygen plasma cleaning.

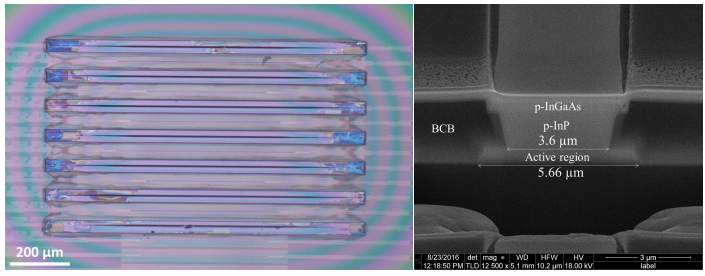
More etching tests were carried out to investigate the undercut of the n-InP. Fig. 2.24(a) shows a microscope image of a test sample after the definition of the active region, where a clear circular boundary is observed. This boundary matches well with the colorful fringes resulting from the topography of the DVS-BCB protection layer. The thickness of the DVS-BCB layer inside of this boundary is more uniform, and no visible undercut of n-InP is found over this area. It is observed that tensile stress is accumulated in the area where the thickness of the



(a) (b)

(c) (d)

Figure 2.22: Microscope image of the p-InP mesas,(a)before HCl etching,(b)after 6 minutes HCl etching,(c) after the other 6 minutes HCl etching,(b) another two times 6 minutes HCl etching.



(a) (b)

Figure 2.23: (a)A microscope image of an array of coupons after the active region definition,(b) A SEM image showing a V-shape cross section laser mesa.

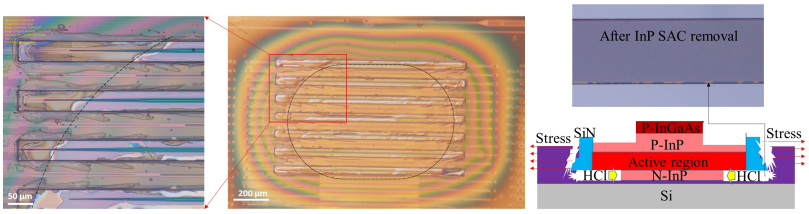


Figure 2.24: (a)A microscope image of a test sample after active region definition,(b)A schematic illustration of the n-InP under etching.

DVS-BCB layer has a distinct variation. This stress results in a detachment of the DVS-BCB from the coupon sidewall, leaving the n-InP exposed to HCl in the p-InP mesa definition, as a schematic shows in Fig. 2.24(b). As can be seen in the above microscope image, the discontinuous line along the edge of the coupon indicates the crevices between the SiN hard mask and the DVS-BCB layer.

2.6.3.4 N-metal contact deposition

An image reversal lithography with two steps of optical exposure using Ti 35E photoresist is performed to open the area where the metal contact will sit on. The photoresist is developed in a 1:3 H_2O: AZ 400 diluted developer. Then a 30 seconds RIE oxygen plasma cleaning is performed to remove the remaining resist in the recesses. To remove the native oxides and ensure a good ohmic contact, the sample is dipped in a 1:1:20 H_2SO_4: H_2O_2: H_2O piranha etchant for 5 seconds. After this surface treatment, the sample is immediately loaded in a Leybold Univex thermal evaporation/sputtering system to prevent the InP from oxidizing again. A 30 nm/20 nm/50 nm Ni/Ge/Au metal layer stack to form an ohmic contact with n-InP and an extra 40 nm/100 nm Ti/Au is deposited. After that, the sample is immersed in a bath of acetone to lift-off the unwanted metal. A microscope image of the sample after lift-off is shown in Fig. 2.25.

2.6.3.5 Passivation and planarization

As known, Al-containing III-V material can rapidly oxidize when it is exposed to air. The native oxide will introduce a lot of surface states over the exposed surface and therefore enhance non-radiative surface recombination, resulting in a reduction of a the carrier lifetime and an increase of the laser threshold. To prevent the oxidation, a short immersion in 1:1:20 H_2SO_4: H_2O_2: H_2O and 1:10 HF:H_2O is performed to remove the native oxides, after which the sample is immediately loaded in a PECVD tool for a 50 nm room temperature SiN deposition. When this

Figure 2.25: A microscope image of an array of devices with N contact metal.

deposition is finished, the temperature is raised from room temperature to 270 °C. Then a 5 nm thick SiO_2, which is used to enhance the adhesion between the SiN layers, and a 450 nm thick mixed frequency SiN are sequentially deposited. After SiN passivation, the devices are planarized using a thick DVS-BCB layer. In this step, a pure Cyclotene 3022-46 DVS-BCB resin is spin coated on the sample at a rate of 2000 rpm for 40 seconds, followed by a BCB full cure procedure. The resulting DVS-BCB layer is around 3.8 µm thick with about 120 nm topography. An RIE dry etch with a 5 sccm:50 sccm SF_6:O_2 mixture is performed to thin down the DVS-BCB to expose the SiN layer, which is then etched in the same tool using another recipe (80 sccm:3 sccm:7 sccm CF_4:SF_6:H_2) to expose the p-InGaAs contact layer for the p-contact metal deposition. The etch rates of DVS-BCB and SiN are around 300 nm/min and 70 nm/min, respectively. Due to a good selectivity, it is easy to decide whether the SiN layer is exposed by checking the variation of the topography over the III-V taper structure using a profilometer. When thinning down the SiN layer, a microscope can be used for the same purpose by checking the color of the devices, which is also more time-saving.

2.6.3.6 P-contact metallization

The topography can be controlled within 400 nm in the previous step. Therefore a thin photoresist (AZ 5214 E) is used to define the patterns of the p-metal contact via an image reversal lithography. After the resist development, a 30 seconds RIE oxygen plasma etch is performed to remove the potentially remaining resist

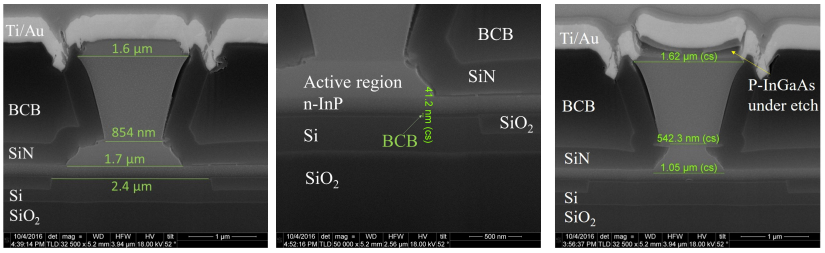
in the recesses. Then the sample is dipped in a 1:1:20 H_2SO_4:H_2O_2:H_2O diluted piranha solution for 5 seconds to remove the native oxide. Again, the sample is immediately loaded in a Leybold Univex sputtering system to prevent oxidation of the p-contact layer. A (40 nm/100 nm) Ti/Au layer stack is sequentially deposited via sputtering and thermal evaporation, respectively, followed by a lift-off process to get rid of unwanted metal.

2.6.3.7 Final metallization

Before the final metallization, a group of vias is opened to reach the n-type metal contact layer, which was covered by passivation/planarization layers (SiN and DVS-BCB) with an overall thickness around $2\,\mu m$. A $3.5\,\mu m$ thick photoresist soft mask (Ti 35E) is used to define these vias. After optical lithography, the sample is loaded in an RIE tool to etch through the DVS-BCB layer using a gas mixture of SF_6 and O_2, followed by a SiN etching using another recipe (CF_4:SF_6:H_2) till the n-type metal contact layer is exposed. Again a combination of microscopy and profilometer are used to trace the etching progress. Next, the photoresist mask is removed by rinsing in acetone, IPA, and water. If necessary, a short RIE oxygen plasma can be used to clean the residual resist. A $3.5\,\mu m$ photoresist (Ti 35E) is used in an image reversal lithography to define the patterns of the metal contact pads. Same as for the n- and p-contact metal deposition, a 30 seconds RIE oxygen plasma is performed to ensure a clean exposed metal layer. Again, to have good electrical contact to the n-metal contact at the bottom of the vias and solid pads for probing or wire bonding, a 40 nm Ti and an 800 nm thick gold layer are used in this metallization process. The deposition is realized using a Leybold Univex sputtering system, followed by a lift-off process.

Fig. 2.26(a) shows a top-view of an array of fabricated DFB lasers. Fig. 2.26(b) and Fig. 2.26(c) show SEM images of the cross-sections of a fabricated device at $10\,\mu m$ and $50\,\mu m$ from the taper tip, respectively. The mesa and QWs waveguide are both well aligned ($<$200 nm misalignment) to the underlying Si waveguide. Together with a 30 nm step from the planarized side SiO_2 cladding, the DVS-BCB adhesive bonding layer between the III-V mesa structure and Si waveguide is measured to be 40 nm (Fig. 2.26(c)). The bottom width of the QWs waveguide is observed to be $1.7\,\mu m$ in Fig. 2.26(b). Although the width of the active region decreases to $1.05\,\mu m$ at the very taper tip (Fig. 2.26(d)), it is still too wide (should be less than 500 nm) to allow an efficient adiabatic coupling and might introduce some reflection to the laser cavity. As shown in the microscope image, the QW waveguide is well aligned with the InP mesa at the taper tip. It means the resist mask did not cover the mesa taper tip and leaves the p-InP mesa as mask in the QWs etching.This is also verified by the undercut in the p-InGaAs layer as the H_3 PO_4:H_2O_2:H_2O solution, which is used to etch the active region also attacks p-InGaAs. Moreover, a wide InP taper tip ($1.62\,\mu m$) is observed in the microscope

(a)



(b) (c) (d)

Figure 2.26: (a) Microscope image of the fabricated devices,(b) an SEM image of the III-V taper structure at $50\,\mu m$ from the taper tip,(c) a zoom-in SEM image shows a 40 nm thick DVS-BCB adhesive bonding layer,(d) an SEM image of the III-V taper structure at $10\,\mu m$ from the taper tip.

images. That is caused by a poor vacuum contact in the lithography due to a high edge bead left in the DVS-BCB planarization\protection procedure. Usually, less than $1\,\mu m$ lines can be achieved using 320 nm optical lithography under a perfect vacuum contact condition with MIR 701 photoresist. Besides these imperfections in the laser mesa definition, an air gap is found between the p-InP and the SiN passivation layer. These issues discussed above will be addressed in the next section.

2.6.4 Characterization

The laser characterization was carried out on a temperature-controlled stage (with a Peltier element). A Keithley 2401 low noise current source was used to bias the device through a pair of DC probes. In the characterization, the optical power was collected by a standard single mode fiber through a GC and was split by a 3 dB coupler with one branch feeding an HP power meter and the other one connected to an optical spectrum analyzer. The optical power coupled to the waveguide was obtained by calibrating out the loss introduced by the GC and the fiber-optics. Fig. 2.27(a) shows the I-V curve of a DFB laser with a $400\,\mu m$ long grating at room temperature with a differential resistance of $5\,\Omega$ under a bias current of 100 mA. The output power of the laser coupled to the Si waveguide is obtained by calibrating the loss of the GC at 1575 nm, which is around -7.2 dB, from the power

collected by the fiber probe. The DFB laser has a second order DFB grating with a phase-shift in the middle with grating period of 485 nm and duty cycle of 75%. The κL of the laser is around 5. The waveguide coupled power is up to 4.5 mW (Fig. 2.27(b)) at 150 mA, which is comparable to the DFB lasers fabricated via bonding in our group [15, 45]. The threshold current is found to be less than 50 mA. Fig. 2.27(c) shows an output of the DFB spectrum at room temperature. The spectrum was recorded using an Agilent 86142B OSA, showing single mode operation with a minimal side mode suppression ratio (SMSR) of 41 dB. The output spectra at different bias currents are shown in Fig. 2.27(d). It reveals four mode hops during the sweeping of the bias current, corresponding to the optical power jumps seen on the recorded PI curve. When the bias current is below 120 mA, the lasing line occurs within the stopband of the Bragg grating, while it jumps to the band edge with an increase of bias current and shows obvious multiple modes at 160 mA. This can be attributed to external reflections or spatial hole burning.

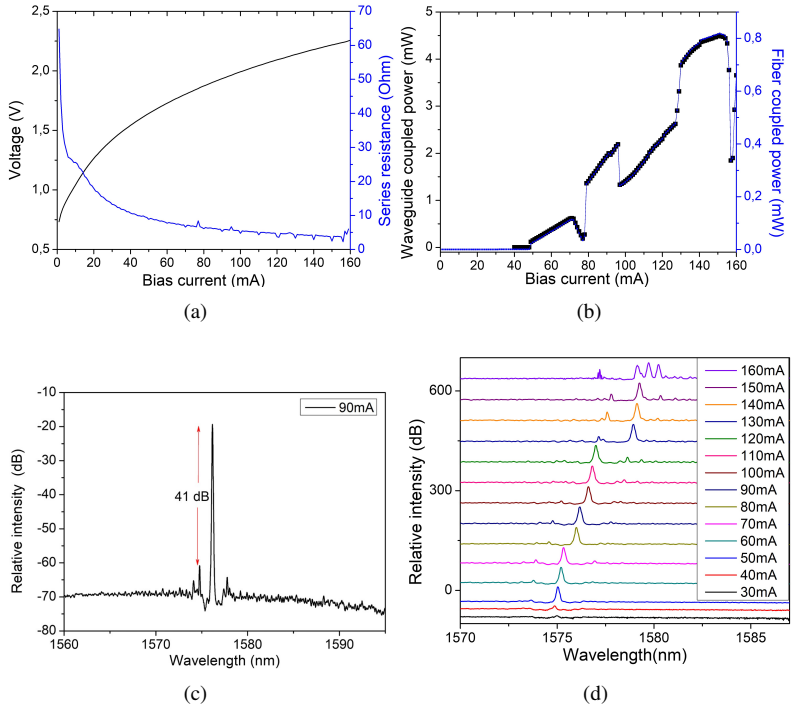


Figure 2.27: Performance of the fabricated DFB laser. (a) V-I curve and differential resistance, (b) P-I curve at different temperatures, (c) Output spectrum at bias current of 90 mA (d) Output spectra at different bias currents.

The mode hops are attributed to parasitic external reflections from the wide III-V taper tip due to the imperfect processing conditions and the fiber GCs. Fig. 2.28 shows a transmission spectrum of a reference waveguide. An obvious interference pattern is observed on the long wavelength side. The modulation depth increases at longer wavelength, indicating a higher reflection from the GCs.

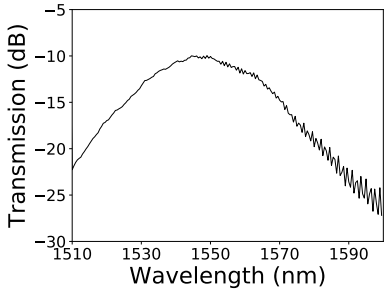


Figure 2.28: Transmission spectrum of a reference waveguide.

2.7 Second generation DFB laser

In this run, a second order Bragg grating with shorter period (477 nm) is used to blue shift the lasing wavelength to the center of the gain spectrum. Meanwhile, so-called tilted focusing GCs [46, 47] with low back-reflection are designed to reduce the external feedback to the laser cavity. On the other hand, the coupons used in this generation are fabricated in the Ghent University cleanroom. In our process flow, the InP sacrificial layer is removed in the coupon definition. In this way, the risk of the under etch of n-InP can be reduced because of the less frequent use of HCl. As discussed in the previous section, a few issues were faced in the post-processing, including the undercut of the n-InP, residual p-InP left at the coupon ends and a wide laser mesa taper tip. To address these issues and improve the performance of the DFB laser, several fabrication steps are modified and optimized in this run.

2.7.1 μTP of III-V coupons on photonic circuit

To have a better control of the thickness of the bonding layer and thus the coupling strength, the diced photonic chip is first dipped in BHF to thin down the side SiO_2 cladding to the same level of the Si layer. Then a 15 nm SiO_2 is deposited over the Si waveguide circuits, followed by spin-coating a 1:6 diluted DVS-BCB solution to achieve a 35 nm thick bonding layer. Before the μTP process, the sample is pre-baked at $150\,^{\circ}\mathrm{C}$ for 10 minutes and then cooled down to room temperature.

As before, a PDMS stamp with a $1000 \times 60\ \mu m^2$ post was selected to pick up and transfer print these coupons to the PIC. The μTP process was carried out using an X-Celeprint μTP-100 tool in the Ghent University cleanroom.

2.7.2 Post-processes

2.7.2.1 Overview of the optimized post-process flow

The optimized process flow is schematically described in Fig. 2.29. In order to protect the n-InP from attacking in the following processes, a SiN layer is deposited (Fig. 2.29(c)). Then the transfer-printed III-V coupons are planarized using photoresist (instead of DVS-BCB to avoid the time-consuming and high-temperature BCB full curing process) (Fig. 2.29(d)), followed by an RIE dry etch to expose the p-InGaAs contact layer (Fig. 2.29(e)). Again, a SiN layer is deposited and patterned using 320 nm optical lithography as a hard mask to define the laser mesa and taper structures. Instead of a complete HCl based wet etching, ICP dry etching with a short HCl cleaning are used to create the V-shape p-InP waveguide cross-section (Fig. 2.29(f)). A room temperature SiN is used to passivate the p-InP mesa, and also used as a hard mask to etch the active region. After the definition of the active region, n-contact metal (Ni/Ge/Au) is deposited on the n-InP layer through a lift-off process, as shown in Fig. 2.29(g). Again, the devices are passivated by SiN (Fig. 2.29(h)), after which the device structure is planarized using DVS-BCB(Fig. 2.29(i-j)). After opening the vias to reach the n-contact metal (Fig. 2.29(k)), the process is finished by a thick Ti/Au deposition (Fig. 2.29(l)). These fabrication steps will be presented in detail in the rest of this section.

2.7.2.2 Si waveguide protection

Similar to the first fabrication run, a 50 minutes RIE oxygen plasma is performed to remove the photoresist encapsulation, followed by a DVS-BCB curing procedure. Then a 300 nm thick SiN layer is deposited to encapsulate the coupon and protect the exposed Si waveguide circuits from being attacked in the following III-V post-processes, e.g. ICP etching of p-InGaAs and p-InP. As the InP sacrificial layer was already removed, this SiN protection layer can be used as a hard mask for the p-InP mesa definition. As already discussed, the edge bead left after the DVS-BCB planarization step will result in a poor vacuum contact in the following lithography and thus a wide taper tip. In this fabrication, a $7.5\,\mu m$ thick photoresist layer (AZ 9260) rather than DVS-BCB is used to planarize these coupons. After spin-coating the photoresist, the sample is baked at $150\,^{\circ}C$ for 5 minutes to let solvent molecules evaporate. RIE dry etching is performed to expose the InGaAs contact layer. Firstly, a gas mixture of 5 sccm:50 sccm SF_6:O_2 is used to thin down the photoresist layer. This recipe provides an etch rate of 300 nm/minute. Once the SiN protection layer is exposed, another recipe (80 sccm:3 sccm:7 sccm SF_6:CF_4:

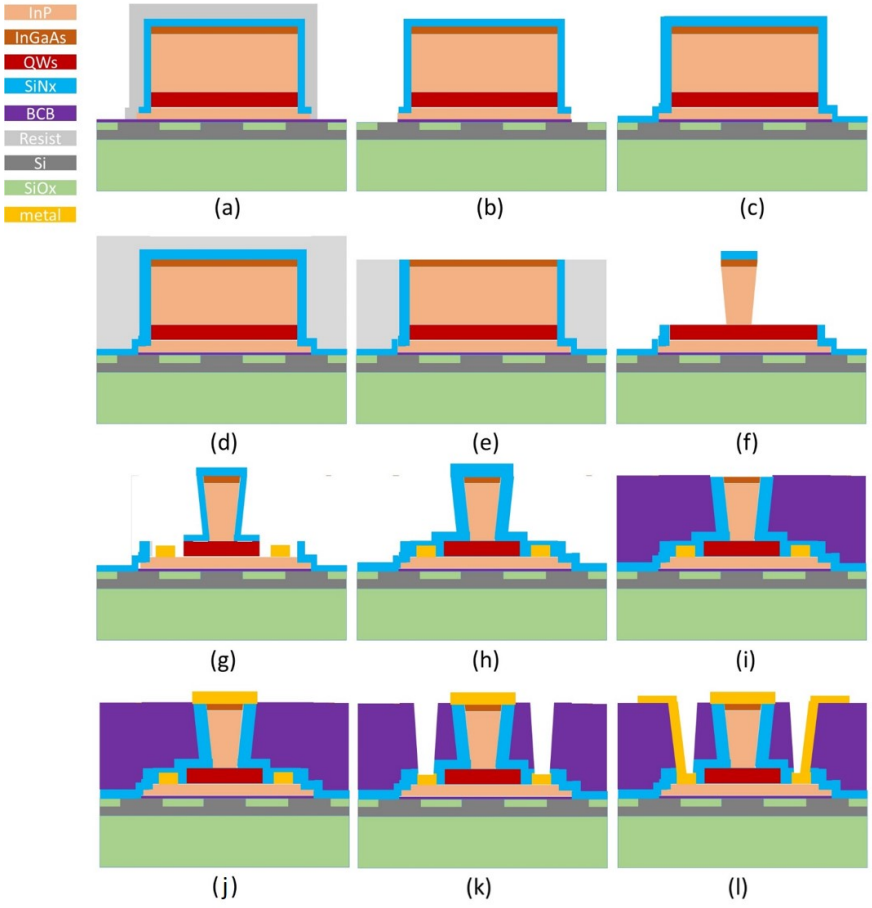
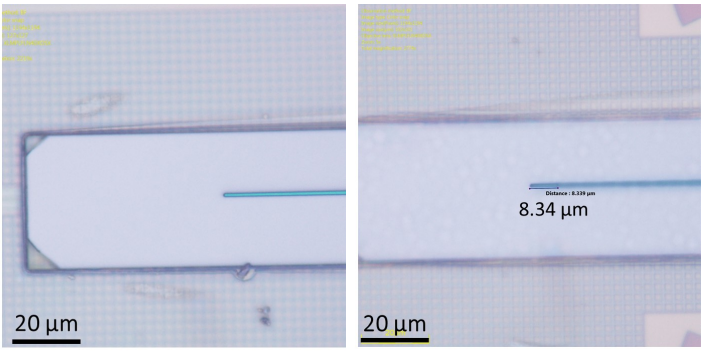


Figure 2.29: Process flow for the definition of the III-V mesa structure in the transfer-printed coupon. (a) Transfer-printed III-V coupon onto Si PIC, (b) Resist removal, (c) SiN deposition, (d) Resist planarization, (e) Etching back to expose the p-InGaAs layer, (f) Laser mesa and taper definition, (g) QW patterning and n-contact metal deposition, (h) SiN passivation, (i) DVS-BCB planarization, (j) p-contact metal deposition, (k) n-via opening, (l) Final Ti/Au metallization.

H_2) is used to expose the p-InGaAs contact layer. After the RIE dry etching, it is difficult to remove the AZ 9260 photoresist using acetone. Therefore an extra RIE oxygen plasma cleaning is executed to remove the residual photoresist after a standard cleaning procedure (acetone, IPA and DI water).

2.7.2.3 Mesa definition

By applying a photoresist planarization no edge bead is left on the PIC. Just as in the previous run, a 300 nm thick SiN layer is deposited and patterned using 320 nm UV lithography as a hard mask to define the InP mesa. Fig. 2.30(a) shows a zoom-in microscope image of a successfully patterned SiN hard mask. Attributed to a good vacuum contact in the lithography, a 800 nm wide taper tip is obtained.



(a) (b)

Figure 2.30: (a)A SiN mesa mask with 800 nm wide taper tip,(b) after InP mesa definition.

To get rid of the residual p-InP at coupon ends resulting from the HCl based anisotropic etching, ICP etching is performed to etch the p-InGaAs and the p-InP. The etch rate of InGaAs and InP in the ICP tool is around 40 nm/cycle and 70 nm/cycle respectively. 25 cycles are applied in this ICP etch. The sample is then dipped in a 1:1 HCl:H_2O solution to remove the residual p-InP over the QW layers and to create the V-shape cross-section at the same time. Owing to the ICP anisotropic dry etch, the depth of the undercut of p-InP from the taper tip inwards is reduced to $10\,\mu m$, as shown in a Fig. 2.30(b).

2.7.2.4 Active region definition

To prevent the p-InGaAs layer from being attacked in piranha solution a SiN hard mask rather than resist soft mask is used to pattern the active region. Moreover, a redesigned hard mask structure with shorter tapers is used to relax the alignment

accuracy, while the already defined mesa taper together with the SiN on top serves as a hard mask for the taper section. When the mesa definition is complete, the sample is dipped in 1:1:20 H_2SO_4:H_2O_2:H_2O and 1:10 BHF:H_2O to remove the surface oxide. Then the sample is rinsed in running DI water to remove the remaining acids. After drying the sample using a nitrogen gun, the sample is immediately loaded in a room temperature PECVD chamber. After depositing a 50 nm thick room temperature SiN, the chamber temperature is set back to 270 °C. Once the temperature of the chamber stabilizes at 270 °C, a 150 nm thick mixed frequency SiN is deposited. To improve the resolution of the contact optical lithography, a 1.7 µm thick photoresist layer (AZ 5214) is used to pattern the shape of the active region (1 µm resolution is sufficient for this purpose). Fig. 2.31 shows the sample with photoresist mask. No obvious damages are observed in the microscope image, and no residual n-InP is left at coupon ends. The rest of the fabrication steps follow the process flow used in the first run.

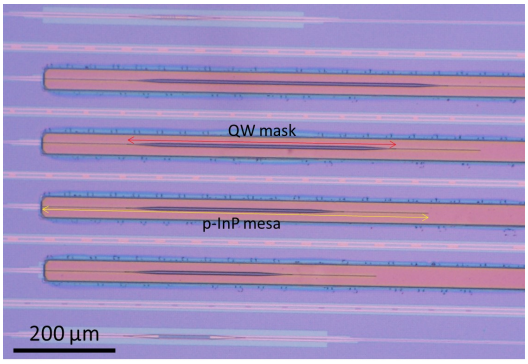
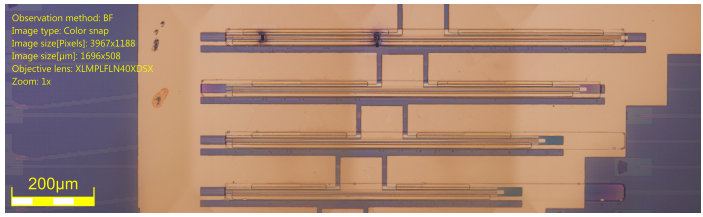


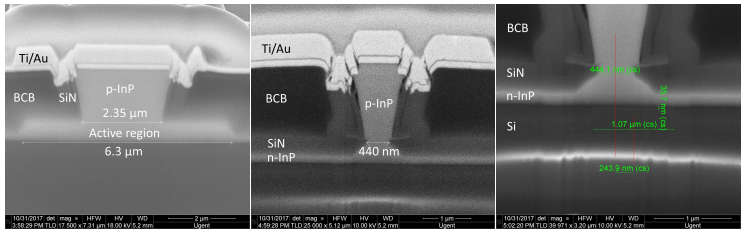
Figure 2.31: A microscope image of an array of coupons with resist mask.

2.7.3 Fabricated devices

Fig. 2.32(a) show a microscope image of the fabricated devices. Fig. 2.32(b) and Fig. 2.32(c) show SEM images of the cross-sections in the middle of the DFB laser and at 90 µm from the III-V/Si taper tip, respectively. Due to a strong charging induced by DVS-BCB and SiN, the Si waveguide is not visible in the first two images. The QW active region is 6.3 µm wide in the laser mesa (while the p-InP mesa is 2.35 µm at the bottom), while it is narrowed down to 440 nm at the top of the AlInGaAs layers close to the taper tip, as shown in Fig. 2.32(c). As this cross-section is made 90 µm from the taper tip a even narrow taper tip can be expected. As can be observed in a zoom-in image (Fig. 2.32(d)), an alignment accuracy better than 250 nm (the typical alignment accuracy is less than 300 nm)



(a)



(b) (c) (d)

Figure 2.32: Top-view microscope image of an array of transfer-printed DFB lasers, (b) FIB cross section image in the middle of the DFB laser, (c) FIB cross section image near the III-V/Si taper tip, (d) a zoom-in SEM image shows a misalignment of less than 250 nm.

is obtained and the III-V/Si separation (SiO_2+DVS-BCB) is around 35 nm.

2.7.4 Characterization

Firstly the coupling behavior of the GC is characterized by measuring the transmission spectrum of a reference waveguide. A Tunics tunable laser is used as the optical source. The optical signal is launched onto a fiber-grating-coupler through a standard single mode fiber. The transmitted optical power out coupled from the GC is collected using the other single mode fiber and guided to a HP power meter. Before sweeping the lasing wavelength, the transmission is maximized at 1550 nm. Fig. 2.33 shows a transmission spectrum of a 700 µm long reference waveguide. Neglecting the loss introduced by the waveguide it reveals a maximum coupling efficiency of -8 dB/GC at 1550 nm. Compared with the transmission spectrum of normal GCs (Fig. 2.28), no obvious interference pattern is observed, indicating a significant reduction of reflection from the GCs.

The setup for the laser characterization is the same as the one presented in the previous section. Fig. 2.34(a) shows the I-V curve of a typical DFB laser with 300 µm long grating at room temperature. It has a differential resistance of 15 Ω at 70 mA, which is larger than that of the laser fabricated in the first run. It was found that the higher resistance is caused by an imperfect contact between p-metal

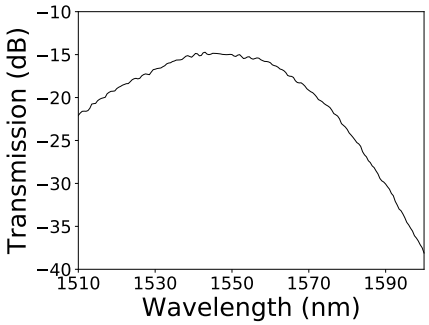


Figure 2.33: Transmission spectrum of a reference waveguide with low reflection GCs.

contact and p-InGaAs, which will be discussed in the next chapter. Fig. 2.34(b) shows the recorded PI curves at different stage temperature. As the temperature increases from 20 °C to 50 °C the threshold current increases from 18 mA to 30 mA. The maximum single-sided waveguide-coupled output power is above 2.2 mW at room temperature. Fig. 2.34(c) shows a superposition of the DFB spectra at 25 °C showing single mode operation up to 70 mA drive current with a minimum side mode suppression ratio (SMSR) of 40 dB. The stopband of the Bragg grating is observed to be 4.8 nm, which corresponds to a κL of 5.16. This high coupling strength, together with a high differential gain at 1555 nm which is close to the gain peak, results in a relatively low threshold. As shown in the inset of Fig. 2.34(c), the lasing wavelength shows 3.5 nm redshift with the bias current increasing from 20 mA to 70 mA. The wavelength shift as a function of the dissipated power is calculated to be 26 nm/W, which is much higher than that of the first generation device (6.4 nm/W over the bias current range from 50 mA to 70 mA). The laser experiences a redshift of 2.5 nm when the stage temperature increases by 30 °C. The SMSR shows no obvious variation when the stage temperature is increased (Fig. 2.34(d)). From these measurements, we can estimate a thermal impedance of the III-V-on-Si DFB around 300 K/W, which is almost three times of that of a typical heterogeneously integrated III-V-on-Si DFB laser [14, 48]. The reason for such a high thermal impedance is still not very clear but probably results from an imperfect bonding quality.

In order to further improve the wall-plug efficiency of these devices, improvements should be made on different fronts. First of all the laser waveguide cross-section needs to be improved (number of quantum wells, modal losses due to doping) as well as the κL of the laser structure. This work is carried out in the framework of the PhD of Bahawal Haq. Further work should be done on reducing the series resistance and the heat sinking of the devices, e.g. by flip-chip mounting them on a AlN heat spreader.

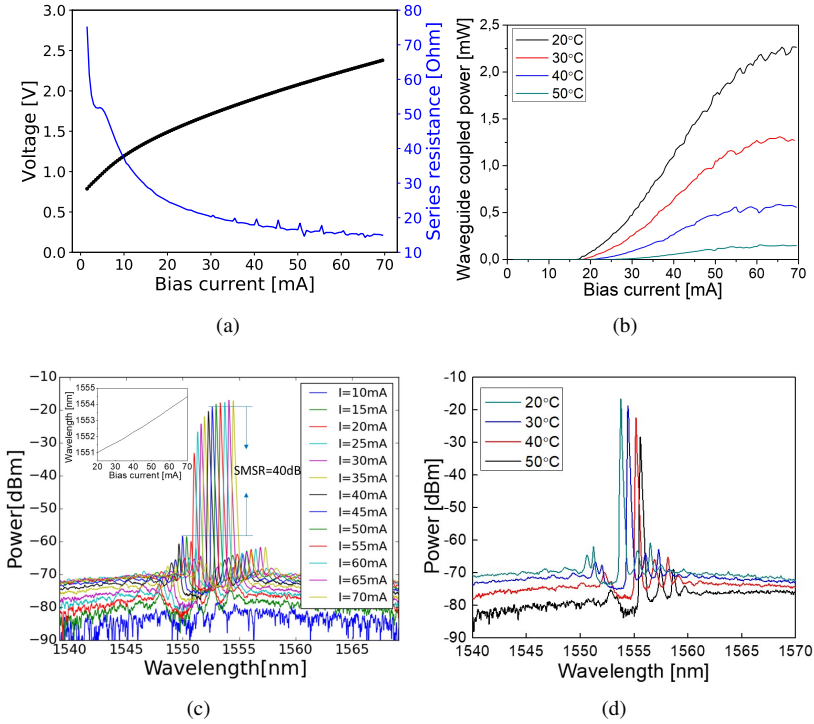


Figure 2.34: Performance of the fabricated DFB laser. (a) V-I curve and differential resistance, (b) P-I curve at different temperatures, (c) Superposition of the output spectra at different bias currents, the inset shows the lasing wavelength evolution as a function of current (d) Wavelength shift as a function of the stage temperature.

2.8 Conclusion

This chapter described the design and fabrication of III-V-on-Si heterogeneously integrated DFB lasers based on the micro-transfer-printing integration of III-V material on Si PICs. This work includes the design of III-V eptaxial layer stack dedicated for the µTP-based integration, fabrication of the III-V coupons on the native III-V substrate, the release process and the development of the post-processing of the III-V laser mesa in the transfer-printed III-V coupons. The released coupons show a pyramidal shape bottom surface due to the long release etch of the $1\,\mu m$ thick InGaAs release layer. Nevertheless, almost 100% printing yield was achieved with the help of a thin DVS-BCB adhesive layer in the tests. Ultra-thin DVS-BCB bonding layers (<20 nm) are achieved by using a DVS-BCB solution with a concentration between 1:4 and 1:8. The post-process flow of the first generation DFB laser is similar to that of the III-V-on-Si integrated devices based on DVS-BCB ad-

hesive bonding in the Photonic Research Group of Ghent University. Single mode operation at 1575 nm with decent waveguide-coupled output power (4.5 mW) and 40 dB SMSR is achieved. Mode hops were observed in the characterization, which is attributed to parasitic external reflections of the fiber GCs and the mesa taper tips due to the imperfect processing conditions.

In the second run, a second-order Bragg grating with a period of 477 nm is used to blue shift the operation wavelength to 1550 nm, close to the gain peak. Meanwhile, GCs with less reflection are used to reduce external reflections. On the other hand, several fabrication techniques were utilized to avoid the fabrication imperfections revealed in the first run. For example, by using the ICP dry etch in the laser mesa definition, the residual p-InP at the coupon ends is successfully removed, and the under etch at the taper tip is also reduced. The fabricated DFB laser shows a single mode operation with more than 40 dB SMSR and a single-sided waveguide-coupled power up to 2.2 mW for bias currents up to 70 mA. In general, a process flow for the integration of III-V-on-Si DFB lasers based on the μTP-based integration of III-V material is successfully developed. This process flow can also be used for the realization of other types III-V-on-Si integrated lasers or even other devices using different III-V materials. It reveals the great potential that μTP has in the field of integrated III-V-on-Si devices/circuits.

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3

Integrated photonic transceivers for FTTH access networks

In the second chapter, we presented a III-V-on-Si DFB laser in which the III-V material is integrated with micro-transfer-printing (μTP). Compared with the conventional wafer/die-to-wafer-bonding approach, the μTP technique could significantly reduce the waste of expensive III-V materials (compared to the efficiency of material use in the case of die-to-wafer bonding, where the smallest die that can be bonded is typically in the millimeter range) . However, it still required a time-consuming post-process. To explore the potential that μTP has for the integration of III-V-on-Si devices, we developed a new process flow for the μTP integration of III-V-on-Si devices. Different from the previous approach, here we move most of the processes onto the III-V wafer, thereby pre-fabricated devices with contact metals rather than material coupons are transfer printed onto the target substrate. In this way the post-processing can be significantly simplified. As a proof of concept, two different transceivers for Point-To-Point (P2P) Fiber-To-The-Home (FTTH) optical networks at the central office (CO) side are realized by μTP of pre-fabricated O-band III-V PDs. The first one is a 4×10 Gbit/s silicon photonic transceiver array, which is based on a complex Si PIC realized on the imec's iSiPP25G photonic platform and an array of μ-transfer-printed PDs. The second one is a single channel transceiver, which consists of a C-band directly modulated DFB laser and a O-band PD. This chapter starts with a brief introduction of FTTH networks. Then the pre-fabrication, release, and transfer printing of the III-V O-band "transparent" PD will be presented. After that, the design,

fabrication, and characterization of the above mentioned transceiver array will be discussed. Finally the single channel DFB-based transceiver will be discussed.

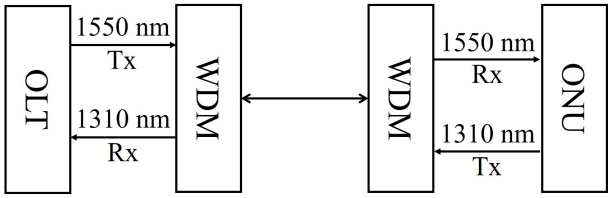


Figure 3.1: Schematic layout of a 1550/1310 nm P2P system architecture.

3.1 P2P transceiver with O-band transparent photodiode

In the early days the P2P networks consisted of two fiber links, with one for upstream signal transmission and the other one for downstream transmission. A single wavelength (1310 nm) is used for both of the up- and downstream.To simplify the layout of the optical systems and cut the cost, today different wavelengths are used for the up-(1310 nm) and down-stream (1490 nm and/or 1550 nm) directions and by duplexing the up- and downstream signals using a 1310/1550 nm WDM only a single fiber is needed for the connection. Fig. 3.1 depicts a bi-directional WDM P2P FTTH scheme [1], which has the most simple layout. In some cases three wavelengths (1550 nm, 1490 nm and 1310 nm) are used in a P2P system, for example, the transceiver demonstrated by Diedrik Vermeulen from the Photonics Research Group [2]. 1490 nm signal carries both voice and data to the home and 1550 nm is used for broadcasting the video signal (TV). Whereas 1310 nm is used for sending upstream digital signals for voice and data from the home back to the CO. In this transceiver a so-called O-band transparent PD (TPD) is used to receive the upstream O-band signal and also to duplex the C-band downstream signal, so that the complexity of the receiver and also the cost are significantly reduced. This TPD is realized with a III-V epitaxial material, whose absorption spectrum has a steep cut-off at $1.37\,\mu\mathrm{m}$, as shown in Fig. 3.2. The O-band signal can be effectively absorbed in the InGaAsP absorbing region while the C-band signal experiences a negligible loss through it. The concept of this transceiver is schematically illustrated in Fig. 3.3, where a TPD is integrated on a grating coupler (GC) via the die-to-wafer bonding technique with a $1\,\mu\mathrm{m}$ thick DSV-BCB layer as an adhesive bonding agent. Downstream signals are coupled out of the plane of the Si PIC and then collected by a single mode fiber after passing through the TPD, while the incoming upstream O-band signal is detected by the same O-band TPD. There is no

polarization dependence attributed to the surface detection of the O-band signal. The sensitivity of the integrated TPD at 1310 nm was about 0.4 A/W. Thanks to the rapid roll-off of the responsivity at 1370 nm, a 40 dB crosstalk at 1550 nm is achieved. The receiver was afterward assembled with external laser sources, Si modulators and a TIA array on a PCB with electronic supporting circuits. 1.25 Gbit/s bi-directional operation was successfully demonstrated [3].

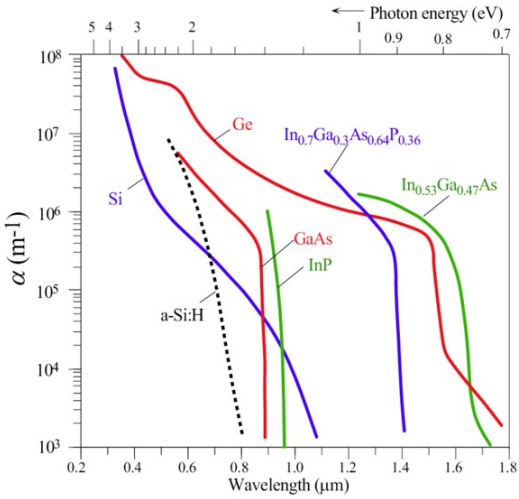


Figure 3.2: Absorption spectra of different materials. Reproduced from [4]

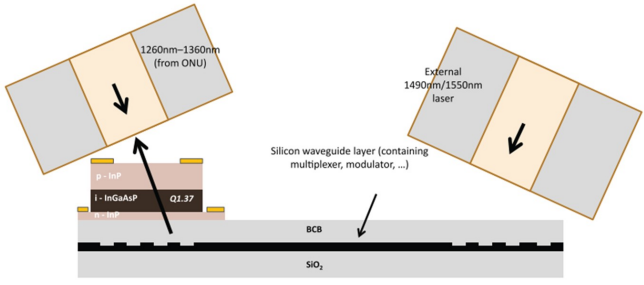


Figure 3.3: Schematic cross-section of the III-V/SOI transceiver with O-band TPD. Reproduced from [3]

Although considerable success has been achieved in the pioneering demonstrations, there is still substantial room for the cost reduction of the III-V-on-Si devices/circuits. More in detail, constrained by the die-to-wafer or wafer-to-wafer

bonding techniques, it is challenging to co-integrate different III-V epitaxial layer structures at the same time or heterogeneously integrate III-V devices on a complex Si PIC, where integrated Ge PDs and Si modulators are included, with a thick back-end layer stack [5–8]. In this work, we demonstrated two integrated optical transceivers based on the TPDs but integrated by means of μTP. Moreover, rather than transfer printing of raw III-V materials, here we integrated pre-fabricated devices with metal contacts. Thereby only simple post-processing steps (planarization and collective wiring of the devices) are needed after the transfer printing procedure. With this approach, the packaging and co-integration issues faced in bonding techniques can be adequately addressed.

3.2 Transfer printing based integration of O-band TPD

In this section, I will present the detailed fabrication steps of the integration of TPDs through μTP, which includes pre-fabrication of the TPDs on the native III-V epitaxial wafer, releasing and μTP of TPDs, and post-processes.

3.2.1 III-V epitaxial layer stack

To realize the duplexing of the 1310 nm and 1550 nm wavelength, a $1\,\mu\mathrm{m}$ thick quaternary intrinsic III-V material, $In_{0.7}Ga_{0.3}As_{0.64}P_{0.36}$, which has a cut-off wavelength of $1.37\,\mu\mathrm{m}$ is incorporated as the absorbing material for the detection of the O-band signal. A 300 nm thick p-InGaAs layer and a 300 nm thick n-InP layer are used for the p- and n-contacts, respectively. This III-V epitaxial device layer stack is the same as that used in [2]. The thickness of each layer is optimized for a maximal transmission of C-band signal. To enable the release of the fabricated device, a $1\,\mu\mathrm{m}$ thick InGaAs sacrifical layer is incorporated beneath the n-InP contact layer.

3.2.2 Overview of the process flow

Fig. 3.4 describes the process flow of the μTP based integration of III-V-on-Si devices/circuits. The process starts from the full layer stack of the source wafer, as shown in Fig. 3.4(a). Firstly the top sacrificial layer is removed by a short etch in HCl. After the p-contact metal deposition through a lift-off process, the TPD mesa is defined by ICP dry etching with a SiN hard mask. After the n-contact layer is exposed, a second mesa is defined by patterning the n-InP layer. Then a n type metal layer stack (Ni/Ge/Au) surrounding the PD mesa is deposited. With a second SiN hard mask, the InGaAs release layer is etched through slightly into the InP substrate, as shown in Fig. 3.4(f). Then the PD structures are encapsulated with a photoresist layer ($\sim 2.5\,\mu\mathrm{m}$ thick) with narrow tethers anchored to the substrate

Table 3.1: III-V epitaxial layer stack for the O-band TPD.

Layer	Layer type	Material	Thickness (nm)	Doping level (cm^3)	Refractive index
7	SAC	InP	100		
6	P-contact	InGaAs	300	1×10^{19}	3.6
5	P-contact	InP	300	5×10^{17}	3.6
4	Absorbing	InGaAsP	1000	n.i.d.	3.442
3	N-contact	InP	240	1×10^{18}	3.169
2	Etch stop	InP	60	n.i.d.	3.169
1	Sacrificial	InGaAs	1000	n.i.d.	
0	Substrate	InP			

Fig. 3.4(g). At this moment, the TPDs are ready for releasing. An aqueous $FeCl_3$ solution at $5\,^{\circ}\mathrm{C}$ is used to undercut the pre-fabricated PDs (Fig. 3.4(h)). A DVS-BCB layer is spin-coated on the planarized SOI waveguide circuit, followed by a $150\,^{\circ}\mathrm{C}$ soft-bake. Now the PDs on the III-V wafer and the target substrate (SOI) are ready for the transfer printing integration. In this process, a PDMS stamp with a $50 \times 50\,\mu m^2$ post was used to pick-up and transfer the PDs using an X-Celeprint μTP-100 tool (Fig. 3.4(i-j)). After transfer printing, the photoresist on top of the TPDs is removed by oxygen plasma using RIE, and the DVS-BCB was cured at $270\,^{\circ}\mathrm{C}$. To passivate the device, another DVS-BCB layer is spin-coated and is then fully cured (Fig. 3.4(k)). After thinning down the DVS-BCB layer to the p-metal contact and opening vias to expose the n-metal contact, the process is completed by a thick Ti/Au deposition to wire the PD contacts to a bond pad array (Fig. 3.4(l)).

3.3 Pre-fabrication of PDs on the native substrate

3.3.1 Geometry of the TPD and the contact mask design

Fig. 3.5 shows an overlaid mask design for the TPD. The U-shape pattern (pink) represents the n-metal contact, where a $17\,\mu m$ wide window between these two arms allows the reception of the upstream and the transmission of the downstream signal from and to the same fiber, respectively. The other U-shape pattern with opposite orientation is used for the p-metal contact definition. The TPD mesa and the coupon mesa are designed to be $30 \times 40\,\mu m^2$ and $60 \times 60\,\mu m^2$, respectively. As the image reversal lithography always results in an enlarged pattern, a $3\,\mu m$ margin is adopted among each layer to prevent possible failures, e.g., a short circuit in the fabrication. As shown in Fig. 3.5(a), four tethers are connected to the coupon mesa to anchor the released devices to the InP substrate. The TPDs are arrayed with a pitch of $100\,\mu m$ in two dimensions (Fig. 3.5(b)). Same as for the III-V

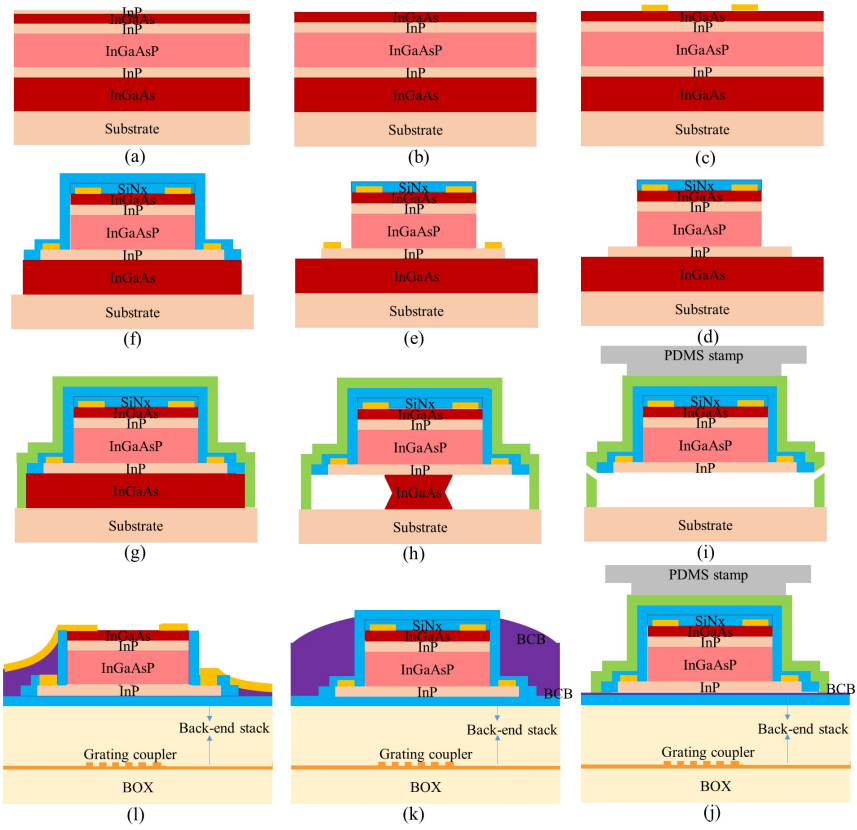


Figure 3.4: Process flow of transfer-printing-based integration of O-band III-V TPDs on silicon photonic integrated circuits.

coupon definition presented in the second chapter, different tether designs are used in this fabrication to decrease the risk of failure in the release process. However, it was found that all these designs work well with a $2.5\,\mu\mathrm{m}$ thick encapsulation layer. Moreover, owing to its small size and rectangular shape, the release time is not dependent on the orientation of the PD.

3.3.2 N-contact metal deposition

An epitaxial die with a size of 1×1 cm^2 is cleaved from a 3 inch wafer for the PD pre-fabrication. Before cleaving a thin layer of photoresist was spin-coated on the III-V epitaxial wafer followed by a 5 minutes softback at $120\,^{\circ}\mathrm{C}$ to protect the wafer surface from particle contamination. Firstly, the III-V die is sequentially rinsed in acetone, IPA, and DI-water to remove the photoresist protection layer.

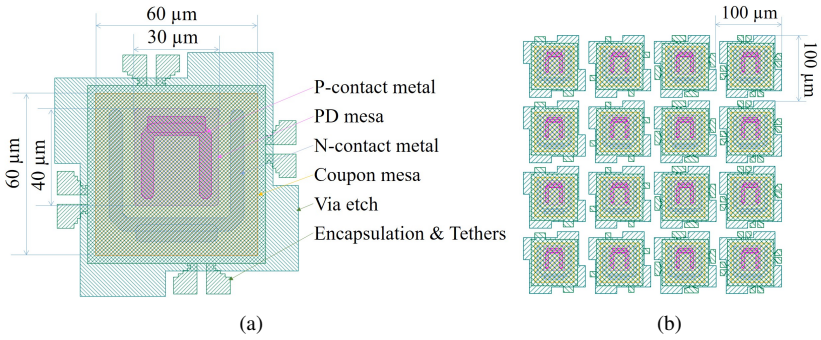


Figure 3.5: Schematic layout the PD design, (a) An overlaid contact mask layers of a PD, (b) A design of a dense PD array with 100 µm pitches.

Then the chip is immersed in a 37% HCl for 20 seconds to remove the InP sacrificial layer. An image reversal lithography procedure is performed to pattern the shape of the p-metal contact using AZ 5214 photoresist. Then 30 seconds RIE oxygen plasma is performed to clean the opened area where the n-contact metal will sit on. To achieve a low series resistance, an oxide removal by a short immersion in a diluted piranha solution (1:1:20 H_2SO_4:H_2O_2:H_2O) is carried out, after which the chip is immediately loaded in a Leybold Univex sputtering system for the n-type metal (40 nm/150 nm Ti/Au) deposition. The whole procedure takes about 3 hours. When the deposition is finished, the chip is immersed in a bath of acetone to lift-off the metal. This step usually takes 10 to 15 minutes. Fig. 3.6 shows a zoom-in microscope image of the deposited p-metal contact.

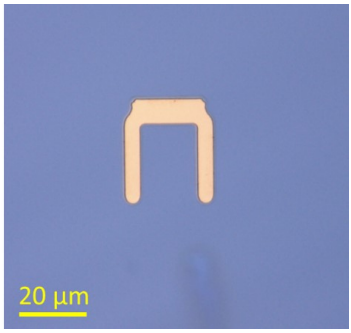
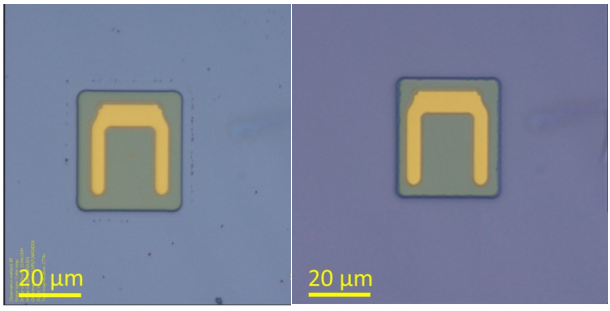


Figure 3.6: Microscope image of the sample after p-contact metal disposition.

3.3.3 PD mesa definition

When the lift-off process is complete, the sample is loaded in a PECVD tool for a 200 nm thick SiN hard mask deposition. Contact lithography using AZ 5214 photoresist is performed to define the shape of the hard mask. After developing the exposed photoresist, RIE dry etching using a gas mixture of SF_6:CF_4: H_2(80 sccm:3 sccm:7 sccm) is performed to transfer the pattern from the resist soft mask to the SiN layer. The sample is then rinsed in acetone, IPA and DI water to thoroughly remove the possible photoresist residues. The TPD mesa is defined by a combination of ICP dry etching and wet etching. Firstly a 25 cycles ICP dry etching is performed, which is supposed to etch through the p-InGaAs, p-InP and about 900 nm into the i-InGaAsP layer. Fig. 3.7(a) shows a microscope image of a device after the ICP dry etching. After the ICP dry etching, the sample is immersed in a bath of 1:1:10 H_2SO_4:H_2O_2:H_2O to remove the remaining InGaAsP and expose the n-InP for the following n-metal deposition. Note the sidewall of the InGaAs contact layer is also exposed in the etchant, so the etching time has to be well controlled to prevent the p-contact layer from being damaging. This step is carried out by first 1 minute etching and a series of short immersion (20 seconds). After each etch the height of the mesa is measured using a profilometer to check the etching progress. Fig. 3.7(b) shows a microscope image of a device after the piranha etching, revealing around 700 nm deep undercut of the InGaAsP layer.



(a) (b)

Figure 3.7: A zoom-in microscope image of a TPD device in the mesa definition, (a) after ICP etching and, (b) after wet etching.

3.3.4 N-contact metal deposition

The n-type metal contact is patterned through an image reversal lithography process using Ti 35E photoresist. After the resist development, the sample is checked under a microscope. The development is stopped when the patterned photoresist

exhibits a blurred edge under the microscope (Fig. 3.8), which indicates that an undercut has been formed. As a large margin is left between the p-contact metal and the TPD mesa, over developing is not harmful to the following metal lift-off process. Before metal deposition, a 30 seconds oxygen plasma cleaning and a native oxide removal by a short dip in a piranha solution are performed. The n-metal contact consists of a layer stack of 30 nm/20 nm/50 nm Ni/Ge/Au and an extra 40 nm/100 nm Ti/Au overlay layer. After metal deposition, a lift-off procedure is performed by immersing the sample in an acetone bath to remove the unwanted metal.

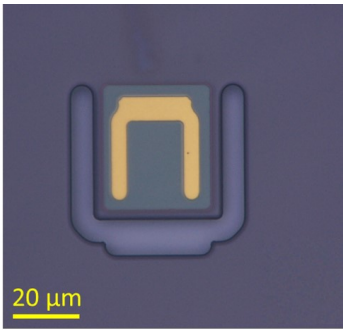
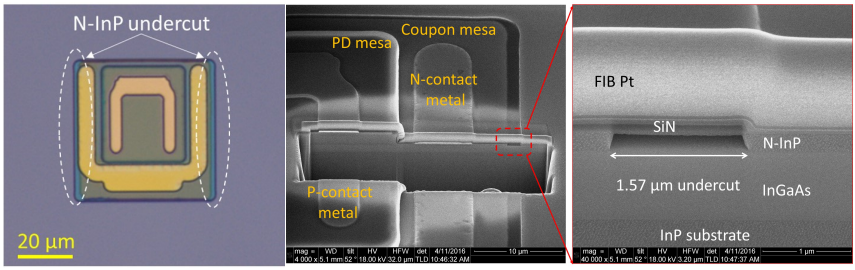


Figure 3.8: Microscope image of a device after the image reversal lithography.

3.3.5 Coupon mesa definition

To minimize dark current, a native oxide removal followed by a SiN deposition should be performed to passivate/encapsulate the sidewall of the device. This step was skipped by mistake in the fabrication. A 200 nm thick SiN layer is deposited on the sample as a hard mask and then patterned with a photoresist soft mask followed by RIE dry etching. Fig. 3.9(a) shows a microscope image of a device with the SiN mesa mask. After the photoresist is removed, the sample is immersed in a 1:1 HCl:H_2O to etch the n-InP layer. As already mentioned in the second chapter, the etch rate of intrinsic InP in 1:1 HCl:H_2O is very slow ($<$20 nm/min). Same as in the PD mesa definition, the etching is carried out in multiple steps to avoid too much undercut. Firstly a 2 minutes etch is performed, that is supposed to thin down 200 nm n-InP. Then the etching time is shortened to 20 seconds to avoid over etch. Nevertheless, a $1.57\,\mu\mathrm{m}$ deep undercut on the n-InP layer is observed when the InGaAs sacrificial layer is exposed, as a FIB cross-section image shows in Fig. 3.9(b).

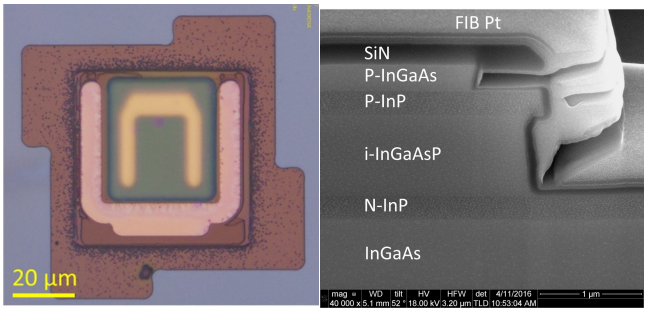


(a) (b)

Figure 3.9: (a) A microscope image of a TPD device after coupon mesa definition. (b) An SEM image of a device, showing a 1.57 µm deep undercut.

3.3.6 Release layer patterning

A 200 nm thick SiN hard mask is used in this step. The InGaAs release layer is etched using a 1:1:18 H_2SO_4:H_2O_2:H_2O diluted piranha solution, which provides an etch rate of 500 nm/min. When it stops on the InP substrate, the sample is rinsed under DI water and dried using a nitrogen gun. Then 4 cycles of ICP dry etching is performed to etch around 300 nm into the InP substrate. Fig. 3.10(a) shows the top view of a device after release layer patterning. As an SEM cross-section image shows in Fig. 3.10(b), the device is well encapsulated by the SiN hard mask layer, preventing the device from being damaged in the following release procedure.

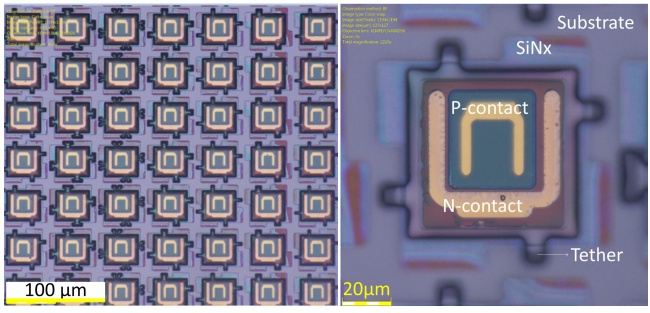


(a) (b)

Figure 3.10: (a)A microscope image of a device after release layer patterning. (b)SEM cross-section image of the PD mesa.

3.3.7 Resist encapsulation and release

Ti 35E photoresist is spin-coated at 3000 rpm for 40 seconds and patterned to encapsulate the fabricated TPDs, resulting in a $\sim 3.5\,\mu m^2$ encapsulation layer. After stripping the residual photoresist by RIE oxygen plasma for 30 seconds, the sample is ready for releasing. Similar to the process presented in the second chapter, the release of the pre-fabricated TPD is realized by immersing the sample in a bath of 1 mg:2 ml $FeCl_3$:H_2O solution, whose temperature is stabilized at $5\,^{\circ}C$ in a chiller. This procedure takes about 100 minutes. Fig. 3.11(a) and Fig. 3.11(b) show the microscope images of the fabricated TPD array and a zoom-in image of a TPD after the release etching, respectively. As can be seen, the TPDs are well anchored to the InP substrate.



(a) (b)

Figure 3.11: (a) Microscope image of a pre-fabricated TPD array after release, (b) A zoom-in image of one TPD on the source wafer.

3.4 Picking and printing test

3.4.1 First printing test

Before heading for the integration on a real PIC, some tests were carried out on dummy SOI chips which exhibit less than 40 nm surface topography. A thin DVS-BCB layer is used to planarize the target substrate (given the small topography) and at the same time it serves as as an adhesive to improve the bonding strength. After a soft bake at $150\,^{\circ}C$ for 10 minutes, the SOI is ready for the printing test. I found that most of the TPDs can be picked up, except the one with the tether design with $16\,\mu m$ wide waist. After picking up, a clean substrate surface is observed. Some tethers did not break but rather detached from the native substrate and transferred with the coupon, as shown in Fig. 3.12(a). The µTP of these TPDs seems to work well, as shown in Fig. 3.12(b). But after exposing in RIE oxy-

gen plasma for 50 minutes (resist encapsulation removal) and DVS-BCB curing at 270 °C, an obvious displacement was found for two of these transfer-printed TPDs (Fig. 3.12(c)). Fig. 3.12(d) shows a FIB cross-section image of a micro-transfer-printed TPD on another dummy chip. It reveals that these unbroken tethers hinder the contact between TPD and the SOI.

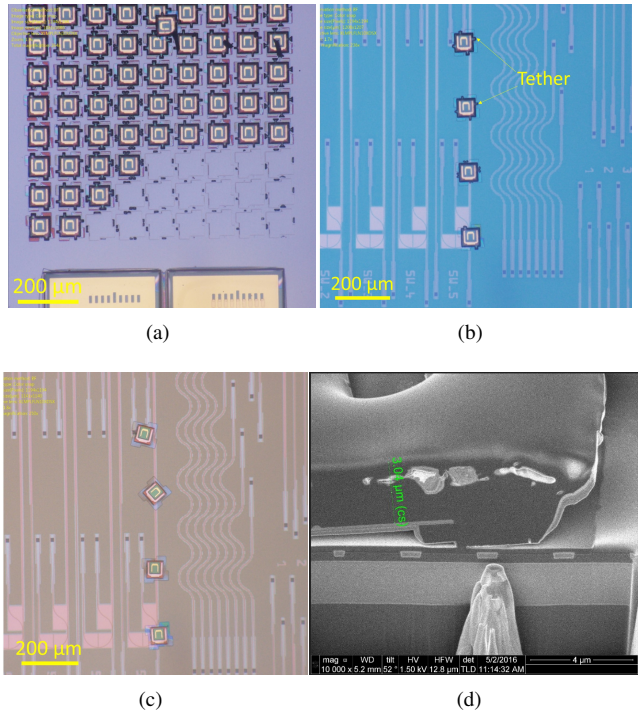
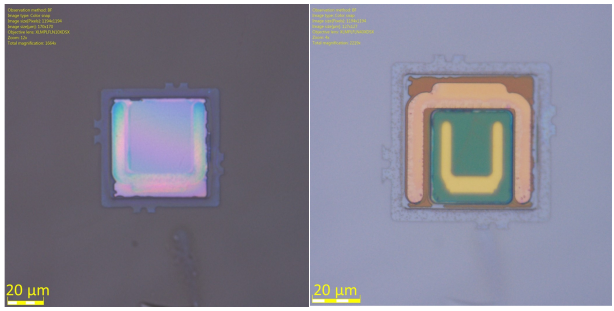


Figure 3.12: Transfer printing of TPDs on an SOI target substrate. (a) Microscope image of the source chip after picking a group of PDs,(b) An array of transfer-printed pre-fabricated TPDs on an SOI target (before photoresist encapsulation removal). (c) The test sample after photoresist encapsulation removal and DVS-BCB curing, (d)A zoom-in SEM image of a photoresist tether that did not break properly.

3.4.2 Second printing test

To weaken the tether and enable the picking up of the TPDs with a proper breaking of the tethers, RIE oxygen plasma etching is performed to thin down the photoresist encapsulation layer by 600 nm. After that a short RIE etching using a gas mixture of SF_6:CF_4:H_2 (80 sccm:3 sccm:7 sccm) is performed to remove the remaining SiN hard mask. A glass substrate is used in the second printing test to



(a) (b)

Figure 3.13: Microscope image of a single transfer-printed TPD on a glass substrate.(a) Through the glass substrate from bottom, (b) Top view.

check the bonding quality. The preparation of the target glass substrate and the µTP of TPD were carried out in the same way as in the first test. Fig. 3.13 shows a microscope image through the glass substrate after the photoresist encapsulation removal and DVS-BCB curing as well as a top view. A good bonding quality is obtained and no obvious delamination is observed at the bonding interface.

3.5 A 4-channel transceiver array

In this section, we will present a 4×10 Gbit/s Si photonic transceiver array for P2P FTTH optical networks. An array of TPDs was integrated with the silicon photonics circuit. The concept of using such III-V TPD for the FTTH transceiver has been demonstrated by Dr. D. Vermeulen from the Photonic Research Group. The integration of TPDs on a passive PIC was realized through the DVS-BCB adhesive bonding technique. In our demonstration, the PIC is realized on the iSiPP25G platform. An array of Si micro-ring modulators is adopted to imprint the C-band downstream signal. The metal bond pads are distributed on top of the back-end layer of the PIC and, resulting in a non-flat surface, which is not suitable for wafer bonding or die bonding based integration. Here the III-V TPDs are integrated by means of µTP of pre-fabricated devices. It showcases the capability that µTP has for the integration of III-V optoelectronic components on a complex Si PIC with a non-flat backend stack.

3.5.1 Design of the 4 channel transceiver array on the imec iSiPP25G platform

3.5.1.1 Imec iSiPP25G platform

The imec iSiPP25G platform involved the most advanced photonic technologies at the time and provided not only a variety of common used passive building blocks, e.g., fiber GCs, MMIs, AWG*etc.*, but also active devices such as Si modulators (Mach-Zehnder interferometer and micro-ring), Ge PDs and Ge EAMs, enabling fully functional PIC with ultra-compact size. Fig. 3.14 illustrates the layer stack of the imec iSiPP25G photonic platform. This platform consists of a 220 nm thick crystalline Si device layer on a $2\,\mu\mathrm{m}$ buried silicon dioxide layer. Three choices of etch depths, 70 nm, 150 nm, and 220 nm, are available for the definition of PICs via 193 nm DUV lithography and dry etching. The fabrication continues with a deposition of a 160 nm thick poly-Si layer which is also patterned with 193 nm DUV lithography and dry etching. This overlaid poly-silicon layer together with the underlying 220 nm Si device layer not only introduces additional flexibility in the optimization of fiber GCs but also facilitates the integration of III-V-on-Si devices. Silicon modulators and resistors are realized by implanting p- and n-dopants in the Si device layer. Three different implant levels are included in the fabrication for different purposes, e.g., PN junctions, a low-resistivity path in 60 nm Si slabs, and low-resistance ohmic contacst to silicide. Implants in the overlaid poly-Si are also possible but carried out in extra fabrication steps. The integration of Ge on Si is realized by selective growth in pre-defined shallow silicon trenches using vapor phase epitaxy. A detailed description of the germanium growth can be found in [9]. After the Ge deposition, a CMP process is performed to planarize the Ge to its desired thickness. Then PN junction is realized by implanting n- and p- doping. The electrical contacts which include the Tungsten vias and the Cu/Al bond pads are defined in a $2\,\mu\mathrm{m}$ thick back-end layer stack, as shown in Fig. 3.14.

Today, the iSiPP25G Si photonic platform has been updated to a 50G version, which provides active devices (e.g., Ge PDs, Ge EAMs and Si modualtors) with bandwidth up to 50G and more possibilities to interface with optical fiber. More information about the iSiPP50G platform is released on the website of Europractice [6].

3.5.1.2 Design of the 4-channel transceiver array

A schematic layout of the proposed 4-channel transceiver array is depicted in Fig. 3.15(a). A 1550 nm continuous wave external laser is coupled to the SiPh transceiver, and it is split to four channels through cascaded 1×2 MMIs. Each channel has a silicon ring modulator, which serves as a downstream transmitter, to imprint data on the 1550 nm optical carrier. The signal is then coupled to fiber through the GC and the integrated O-band TPD, as shown in Fig. 3.15(b). By se-

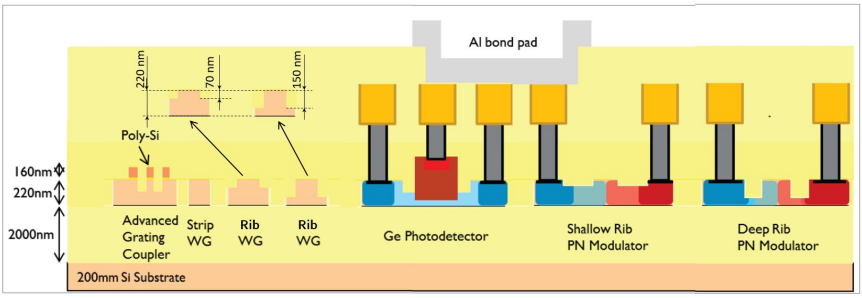


Figure 3.14: Schematic cross section of imec's iSiPP25G full-platform.

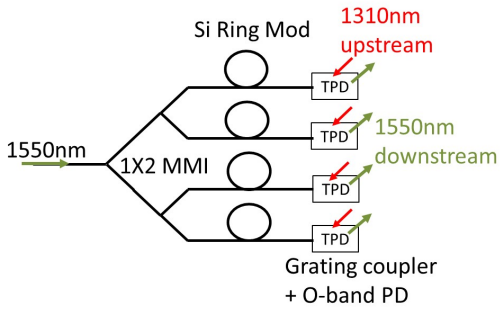
lecting the cut-off wavelength of the III-V absorbing material to be $1.37\,\mu m$, the TPDs are 'transparent' (four orders of magnitude smaller responsivity) for the C-band signal, which enables the duplexing of the C-band and O-band signals that are sent and received through the same fiber.

Fig. 3.16(a) shows a microscope image of the received SOI die, whose size is 5×5 mm^2 and the areas marked by the red and yellow boxes are where the transceivers are located. A zoom-in image of this 4-channel transceiver is shown in Fig. 3.16(b). Although the transfer printing technique is expected to enable the integration of III-V PDs on a complex PIC, the small die will induce some practical issues during the fabrication, which will be discussed in detail in the rest of this chapter.

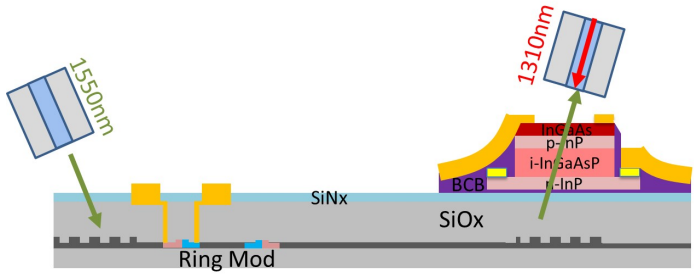
3.5.2 Transfer printing of pre-fabricated TPDs on iSSIP25G PIC

3.5.3 Spin-coating of DVS-BCB

A sample with an area of $1.5 \times 1.5\,cm^2$ or bigger is usually used in the fabrication of III-V-on-silicon circuits. It is difficult to handle the chip if its size goes down to $0.5 \times 0.5\,cm^2$. The edge bead resulting from spin-coating becomes problematic in the planarization process. It will also result in a poor vacuum contact and thus an imperfect optical lithography, which will increase the risk of failure in the following lift-off process. Fig. 3.17 shows two samples which are spin-coated with 1:4 diluted DVS-BCB: Mesitylene solution at 3000 rpm for 40 seconds, which results in a 70 nm thick DVS-BCB layer in the center of the sample. $650\,\mu m$ and $750\,\mu m$ wide DVS-BCB edge beads are observed on the two samples. Spin coating a 450 nm thick DVS-BCB layer, which is expected to allow a maximal transmission of the C-band signal through the PD, will result in an even thicker and wider edge bead. Therefore a thick DVS-BCB layer is not recommended here, e.g., to planarize the μTP TPDs.



(a)



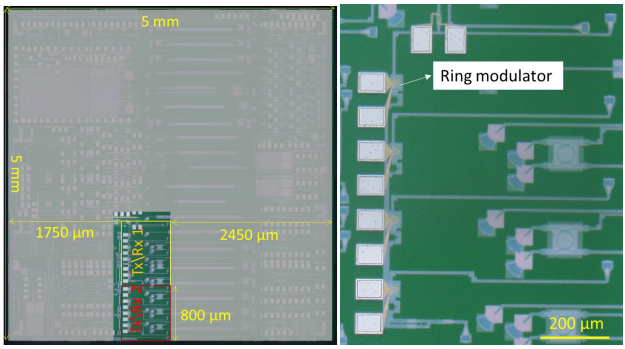
(b)

Figure 3.15: (a) Schematic layout of the III-V-on-silicon FTTH transceiver array, (b) Schematic cross-section of one transceiver.

Given this situation, a 400 nm thick SiO_2 layer is first deposited on the sample, followed by spin-coating a 50 nm thick DVS-BCB layer (1:8 DVS-BCB:Mesitylene). In this way, the overall thickness of the spacer layer (DVS-BCB + SiO_2) is close to the expected optimal bonding layer thickness. Then the sample is baked on a hot plate at $150\,^{\circ}\mathrm{C}$ for 15 minutes and then cools down to room temperature naturally. By now, the sample is ready for the transfer printing procedure.

3.5.4 μTP of pre-fabricated TPD

A PDMS stamp with a $50 \times 50\ \mu\mathrm{m}^2$ post was used to pick-up and transfer the TPDs using an X-Celeprint μTP-100 tool. This system can realize automatic alignment with COGNEX image recognition software. In the printing process, the software first analyzes and finds out the center of the captured images of the alignment markers. Then the post, together with the attached device, is transferred and printed onto the target substrate according to the already known relative position. This procedure takes about 45 seconds, and the alignment accuracy is down



(a) (b)

Figure 3.16: (a) Microscope image of the SOI chip, (b) Zoom-in microscope image of the 4 channel transceiver.

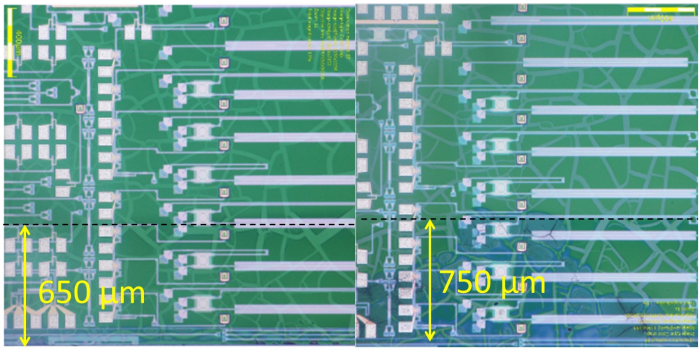


Figure 3.17: Microscope images of SOI chip with spin-coated DVS-BCB layer, showing a wide edge bead.

to $\pm 1.5\,\mu\mathrm{m}$ ($3\,\sigma$). It is also possible to set an offset to the 'center' that was found by the pattern recognition software when the co-designed markers are designed not to be center-to-center aligned [10, 11]. As we already discussed, the transmission aperture of the pre-fabricated TPD ($17 \times 25\ \mu\mathrm{m}^2$) is much bigger than the mode field out coupled from the fiber GC (around $10\,\mu\mathrm{m}$ in diameter), which leaves up to $3.5\,\mu\mathrm{m}$ alignment margin. In this printing, the U-shaped p-metal contact and the GC itself are used as markers to enable the automatic alignment. As the center of the GC is off from that of the out coupled-mode field, the reference position was adjusted to be $5\,\mu\mathrm{m}$ away from the first grating line, as shown in Fig. 3.18. Note one needs to guarantee that only one GC could be seen in the field of view, otherwise, the pattern recognition system will get confused and hardly find the correct destination. This procedure includes five major steps. Firstly, we analyze the

markers for both of the source device and target substrate and set them as the references for the following automatic alignment operation. Then the stamp is visually aligned to pick up the device of interest. After that the stamp with TPD is moved close to the target fiber GC. The pattern recognition procedure is started when the target GC and the TPD are clearly seen in the field of view. When the alignment is completed, we can print the TPD. Before starting another cycle of printing , the post needs to be cleaned by laminating the post to a sticky surface. To further accelerate the integration process, one can drive the system using a script.

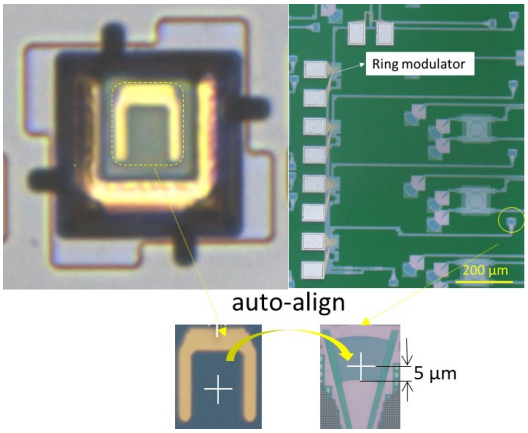


Figure 3.18: Schematic illustration of the automatic alignment of a PD with a target fiber GC.

3.5.5 Encapsulation removal and DVS-BCB curing

After µTP of TPDs, the sample is baked at 130 °C for 1 minute to reflow the encapsulation photoresist to ensure a good contact of the device to the target die. Thereafter the photoresist is completely removed by RIE oxygen plasma, followed by a DVS-BCB curing procedure. Fig. 3.19 shows the sample with an array of transfer-printed TPDs after DVS-BCB curing.

3.5.6 DVS-BCB planarization

Usually, a thick DVS-BCB layer is adopted to planarize the printed III-V devices so that the p- and the n-contacts can be isolated. Also, the metal wires and contact pads are isolated from the Si waveguide, which prevents additional loss from metal absorption. As already discussed, a thin DVS-BCB is preferable for the planarization on a small die to avoid a thick edge bead. Fig. 3.20 shows a FIB cross-section image of a dummy sample spin-coated with a 1:6 DVS-BCB: Mesitylene solution.

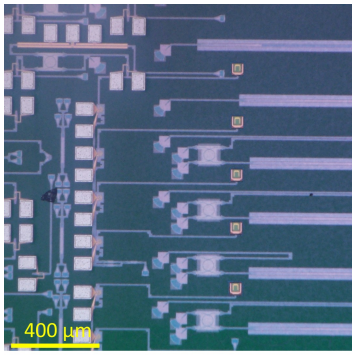


Figure 3.19: Microscope image of the photonic circuits with transfer-printed TPDs after DVS-BCB curing.

A 1.6 µm high feature is used to mimic a transfer-printed photodetector. As can be seen, the sidewall of the dummy structure is well covered by a 3 µm long BCB ramp, which is sufficiently thick to isolate the p- and n- contacts of the transfer-printed TPDs.

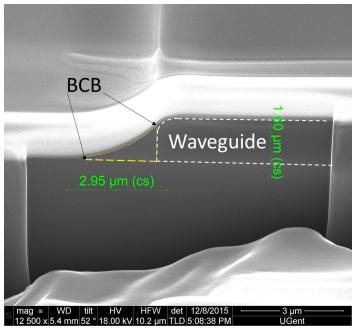


Figure 3.20: SEM image of a 1.6 µm high structure mimicking the photodiode with spin-coated 50 nm thick DVS-BCB layer.

3.5.7 Via opening

Before the spin-coating of DVS-BCB, a 400 nm thick SiN layer is first deposited on the sample to ensure good electrical insulation between the n- and the p- metal contacts. Then a 50 nm thick DVS-BCB layer is spin-coated on the sample, followed by a curing procedure. Both the n- and p- contact metal are locally exposed by RIE etching with photoresist soft mask (AZ 5214E). The SiN layer over the transmission window is also removed in this step. Although the p-InGaAs contact layer will induce additional loss to both of the C- and the O-band signal, it was not

removed in this fabrication to avoid potential damage of the integrated devices.

3.6 Final metallization

A 3.5 µm thick (Ti 35E) photoresist is used as an image reversal photoresist to define the pattern of the metal wires and probing pads. After a short RIE oxygen plasma cleaning, a p-type metal contact Ti/Au 40 nm/800 nm is deposited using a Leybold Univex system, followed by a lift-off procedure to remove the unwanted metal. By now most of the sample surface is still covered by the planarization layer (400 nm thick SiN and $\sim$ 50 nm thick DVS-BCB), therefore additional lithography and RIE need to be performed to expose the bond pads of the ring modulators. Fig. 3.21 shows a microscope image of the fabricated 4 channel transceiver whose overall size is 1×1 mm^2.

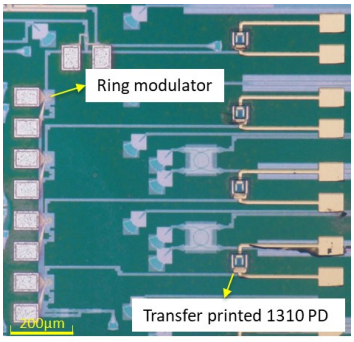


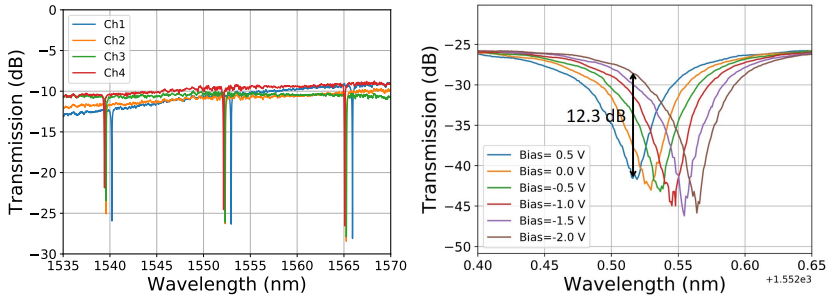
Figure 3.21: Microscope image of the fabricated transceiver array with bond pads.

3.7 Characterization of the 4-channel transceiver

3.7.1 Static characterization

The characterization was carried out on a temperature-controlled stage to stabilize the temperature at 20 °C. Two Keithley 2401 current sources were used to bias the TPD and tune the Si micro-ring modulator through high speed GS probes (K band). C-band and O-band Santec 510 tunable lasers together with a few HP power meters were used to characterize the transmission of the transceiver array. Fig. 3.22 shows the transmission of all channels with various colors. The loss of the fiber GCs was calibrated out from the measured spectra to extract the insertion loss induced by the integrated O-band PDs. Except for $\sim$ 6.5 dB loss from the cascaded 1×2 MMIs in each channel, the insertion loss of the O-band PDs for the C-band signal is found

to be 3.5 dB, which is mainly attributed to the absorption of the p-contact layer (∼0.9 dB), the reflections at the interfaces between p-contact layer and air (∼1.67 dB) and between the DVS-BCB and n-contact layer (0.55 dB). Together with the 4 dB insertion loss from each GC the overall insertion loss for each channel is 18 dB. It can be reduced to less than 14 dB if optimized GCs are used [6, 12]. Fig. 3.22(b) shows a DC characterization of the p-i-n micro-ring modulator, revealing a 12.3 dB extinction ratio for 2.5 Vpp voltage swing.



(a) (b)

Figure 3.22: (a)The loss of the transcevier (micro-ring modulator, cascaded MMIs and O-band TPD) in C-band excluding the loss from GCs, (b) The ring modulator resonance wavelength shift versus bias voltage.

Firstly the dark current of the transfer-printed TPDs was investigated. Fig. 3.23 shows the IV response of an integrated PD. In the measurement, the bias voltage was swept from 0.5 V to -3.0 V with a step of 0.1 V. The dark current was found to increase with the bias voltage and reached $\sim 0.7\,\mu$A at -3 V. The high dark current (up to $1\,\mu$A at -3 V) might be attributed to surface leakage current on the sidewalls because of a poor passivation. This, however, is not expected to impact the system performance when integrated with a trans-impedance amplifier(TIA) [13].

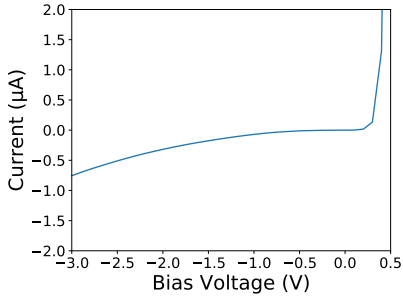


Figure 3.23: IV response of a micro-transfer-printed TPD.

The responsivity for the O-band signal is 0.39-0.49 A/W at -3 V bias voltage (Fig. 3.24(a)) and it is constant over the wavelength range from 1270 nm to 1350 nm (Fig. 3.24(b)), while that for the C-band signal is 0.025-0.03 mA/W, which is over four orders of magnitude smaller (Fig. 3.24(c)). The responsivity can be further improved by applying an anti-reflective coating on top of the photodiode, removing the InGaAs contact layer in the aperture of the photodiode and increasing the InGaAsP absorption layer thickness.

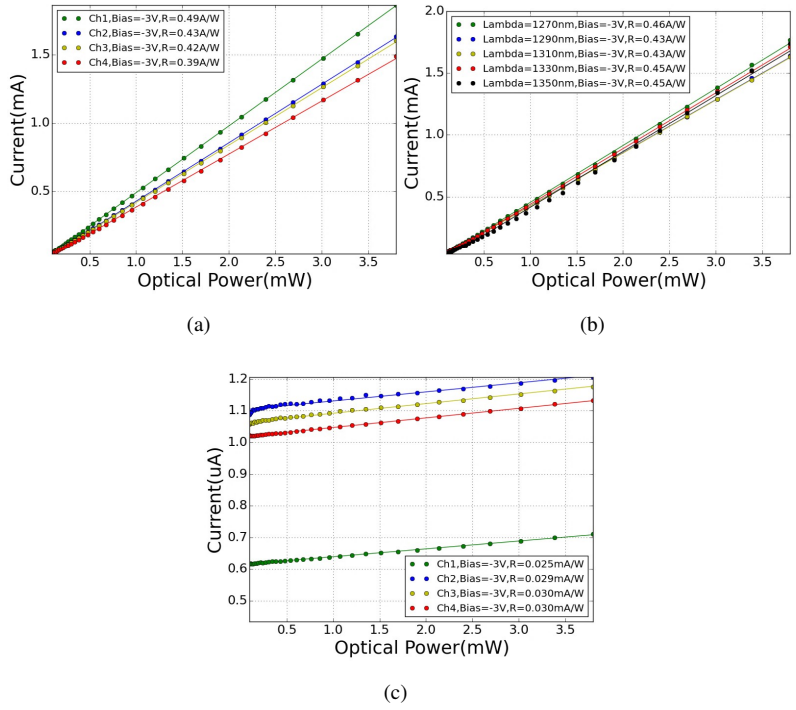


Figure 3.24: Photocurrent of the transfer-printed O-band TPDs (a) at 1310 nm, (b) over the range of 1270 nm-1350 nm, (c) at 1550 nm (including the photodetector dark current.

3.7.2 Dynamic characterization

To study the high-speed performance of the integrated transceivers, a small-signal characterization was done using a Vector Network Analyzer (VNA). Fig. 3.25(a) shows the measured frequency response of the ring modulators at -1 V bias. The 3 dB bandwidth is found to be 15 GHz. On the other hand, the 3 dB bandwidth of the transfer printed O-band TPDs is measured to be 11.5 GHz with good uniformity

over these four devices, as shown in Fig. 3.25(b)

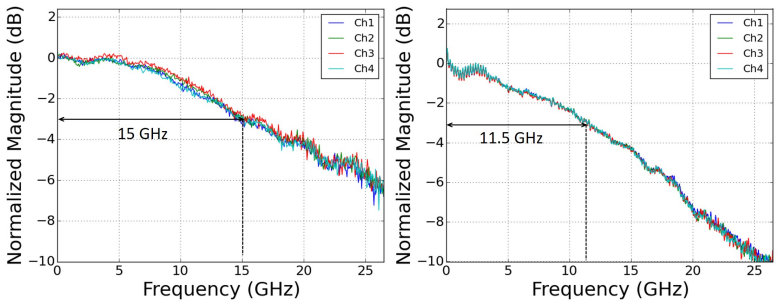


Figure 3.25: Small-signal response. (a) Measured $|S_{21}|^2$ curves of ring modulators. (b) Measured $|S_{21}|^2$ curves of O-band TPDs.

Fig. 3.26 depicts a schematic layout of the measurement setup used for large signal modulation. Back-to-back characterization was performed, where the downstream and upstream optical carrier was provided by a C-band and an O-band Santec tunable laser, respectively. The Si micro-ring modulator and an O-band commercial modulator were simultaneously driven by a Pulse Pattern Generator (PPG) to imprint the data signal onto the optical carriers. Non-Return-to-Zero (NRZ) pseudo-random-bit-sequence signals with different pattern length were investigated in the following demonstration. The O-band and C-band signals were duplexed using a 1310 nm/1550 nm fiber wavelength multiplexer. Next to the fiber optic duplexing, an erbium-doped fiber amplifier is used to boost the transmitted C-band data signal, which is then filtered by a bandpass filter to suppress the noise. A commercial high-speed photodetector with 40 GHz bandwidth is used to detect the signal. The bias voltage was applied through a bias tee using high-speed probes. Variable optical attenuators were used to adjust the optical power in fiber. The optical power launched to the integrated O-band TPD and the C-band optical receiver was monitored by an inline power meter and an HP power meter (connected to a -20 dB power tap), respectively. Finally, the detected electric signals were fed to a digital serial analyzer for eye-diagram analysis.

In the measurement, the transmitter (Ring MOD) and receiver (TPD) were operating simultaneously at 10 Gbit/s. The operation wavelength and output power of the C-band laser were set to be 1550 nm and 0 dBm respectively. Because of the loss induced by the GC and the cascaded MMIs, the optical power coupled to the ring modulator is estimated to be around -15 dBm. The output power of the O-band laser was set to be 13 dBm. A -1 V bias voltage was applied to the ring modulator through a Bias-Tee and a high speed GS probe. The applied voltage swing was 1.6 V, which provided the optimized performance. With an average optical power of

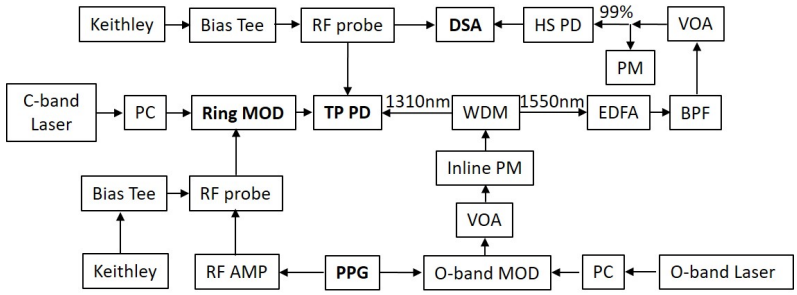


Figure 3.26: Schematic layout of the characterization setup for the transceiver operating with upstream and downstream signal simultaneously applied. DSA: digital serial analyzer; HS PD: high-speed photodetector; VOA: variable optical attenuator; PM: power monitor; MOD: modulator; TP TPD: transfer printed transparent photodetector; WDM: wavelength division multiplexer; EDFA: erbium doped fiber amplifier; BPF: band pass filter; PPG: pulse pattern generator; PC: polarization controller.

0 dBm feeding to the HS PD, the C-band eye diagrams exhibit an extinction ratio over a range from 9.2 to 9.75 dB and a Q factor around 10 for these four channels. Fig. 3.27 shows overlaid eye diagrams of the upstream (O-band) and downstream (C-band) signals. By varying the polarization of the upstream signal, a small peak-to-peak amplitude variation of 6% could be observed for the O-band PDs. This is attributed to the non-vertical position (13 degrees off-vertical) of the fiber. To check the wavelength dependence of the printed TPDs, the operation wavelength was swept from 1270 nm to 1350 nm. Fig. 3.28(a)-Fig. 3.28(c) show the eye diagrams for 1270 nm, 1310 nm and 1350 nm data signals, respectively. Clean and open eyes were obtained for all the TP PDs over the entire wavelength range. A narrower eye was observed at 1350 nm due to the high loss of the wavelength multiplexer at this wavelength.

As the bandwidth of the ring modulators and the O-band TPDs are both above 10 GHz, up to 20 Gbit/s operation should be possible. While being limited by the maximum speed (12.5 Gbit/s) of the PPG, the BER was only investigated at 10 Gbit/s and 12.5 Gbit/s with different pattern lengths. Firstly, the received optical power on the O-band TPDs was adjusted through the VOA, while having the upstream link operational. As shown in Fig. 3.29, the receivers behaved uniformly and error free operation was achieved at a received power of 0 dBm for a pattern length of 2^7-1. This high demanded average power is due to the lack of integrated TIA. When a longer pattern length (2^{15}-1) or higher speed (12.5 Gbit/s) was used, the required input power for error free operation increased to 1 and 2.7 dBm, respectively, because of the bandwidth limitation of the devices. Vice versa, the BER

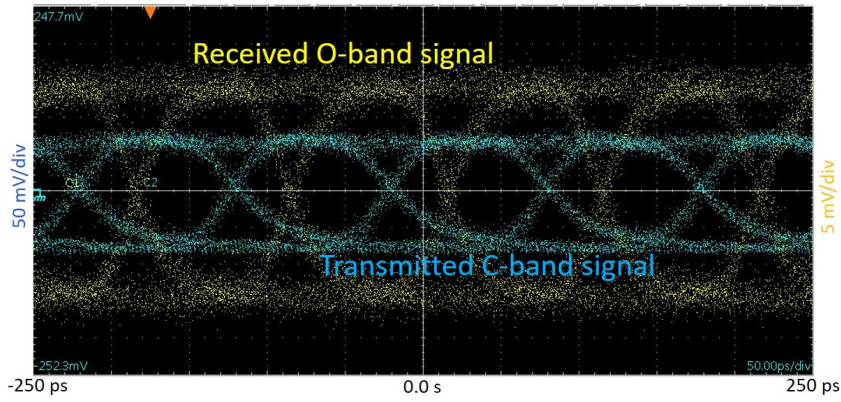
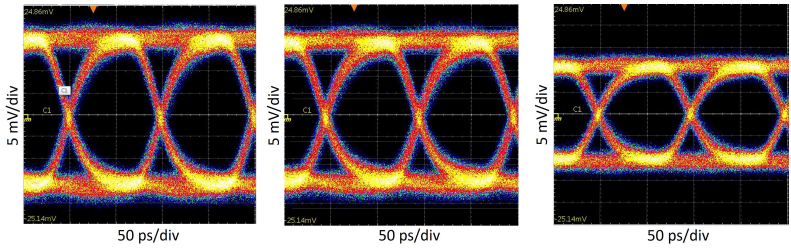


Figure 3.27: Overlaid 10 Gbit/s eye diagrams of the upstream (O-band) data signal and downstream (C-band) data signal.



(a) (b) (c)

Figure 3.28: Received 10 Gbit/s NRZ-PRBS upstream signal at (a) 1270 nm, (b) 1310 nm and (c) 1350 nm. The vertical scale is identical in all plots.

of the downstream link was studied and error-free operation was realized with an input power of -11 dBm for 10 Gbit/s operation (2^7-1). In order the check the C-band/O-band crosstalk in the O-band PD in a straight forward way, a comparison between bit error rate results with the ring modulator on and off was made and no obvious change was observed from the curves shown in Fig. 3.30. Again, indicated by the widely open eyes at 12.5 Gbit/s, this transceiver is expected to be able to operate at a higher bit rate.

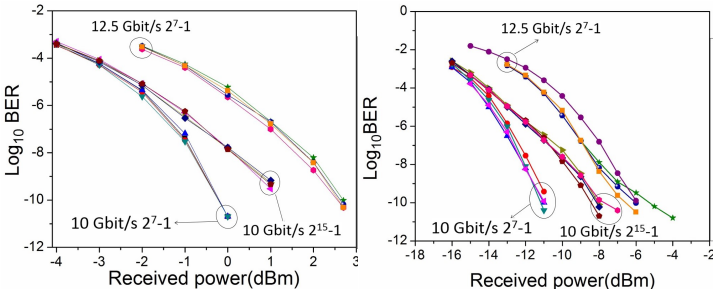


Figure 3.29: Measured BER versus received optical power for (a) the upstream data signal, (b) the downstream data signal.

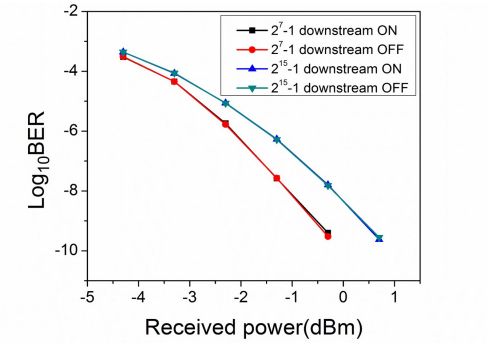


Figure 3.30: Measured BER of the upstream data signal at 10 Gbit/s with the downstream link operational or off.

3.8 A FTTH transceiver based on a III-V-on-Si integrated directly modulated laser and a co-integrated O-band TPD.

In the previous sections, we demonstrated a 4-channel FTTH transceiver array based on the μ-transfer-printed O-band TPDs. Owing to the duplexing function brought by the TPDs, this transceiver array exhibits a small footprint ($1\times1\ \mathrm{mm}^2$). More importantly, this demonstration shows the great potential of the μTP technique for the realization of III-V-on-Si PICs. Nevertheless, the requirement of an external optical source leads to a high cost of the transceiver because of the time consuming active alignment required in the packaging process. Considerable efforts have been devoted to the integration of III-V-on-Si devices on a complex PIC, e.g., in the iSiPP25G/50G platform, but no mature technology is available yet. To

address this issue, an alternative approach is proposed to realize a fully functional transceiver, where the Si PIC is realized on imec's passive photonic platform with 400 nm Si device layer. This transceiver consists of a III-V-on-Si integrated DFB laser and an O-band TPD, which are both integrated on the PIC via μTP. The DFB laser is directly modulated to imprint the down-stream signal on the C-band laser emission. Owing to the use of a directly modulated laser (DML), the cost, the size, and the power consumption of the transceiver can be significantly reduced. This section starts with a brief introduction on the DFB based DML. Then the design and fabrication of the transceiver will be presented. In the end, the measurements, including the static and dynamic characterizations, will be reported.

3.8.1 Directly modulated laser

The electrically pumped laser is actually an EO converter, whose output optical power is mainly determined by the bias current (or voltage) level. In other words, an electric signal which carries data can be directly applied to the laser diode to output a corresponding modulated output optical signal. These lasers are named DMLs and have been widely adopted as transmitters in optical communication systems. In comparison with other types of transceivers with separated modulators, DMLs are more favorable for applications in optical networks because of their simple electrical circuit configuration, small footprint, and easy fabrication [14]. However due to severe inherent chirp caused by the parasitic frequency modulation and a relatively low extinction ratio, performance of a DML degrades for longer reaches (>10 km) [15, 16]. An effective way to extend the reach of the fiber link is by applying a chirp management technique. An optical filter, e.g., micro-ring resonator, is incorporated with the DML to reshape the amplitude as well as the instantaneous frequency profile of the modulated optical signal and therefore enhance the transmission [17–19].

Direct modulation can be realized using different types of lasers. Amongst the existing candidates, VCSELs have very compact size, with a diameter of few tens of μms [20]. However, it is challenging to integrate VCSELs on a complex photonic circuit. The integration of III-V-on-Si DFB lasers is much easier. Besides VCSELs and DFBs, direct modulation of tunable lasers was also demonstrated in [21–23]. In the case of P2P FTTH transceivers used at the central office side, DFB based DMLs are more favorable over other candidates because of their high output power, single-mode output, and simple layout. Together with the advantages provided by Si PICs, the III-V-on-Si integration offers a cost-effective solution for a communication system in access networks. Currently, the integration of III-V-on-Si devices/circuits is mainly realized via bonding techniques. As an example, Dr. Amin Abbasi demonstrated a 28 Gbit/s DFB laser in [24]. This laser was fabricated through the standard DVS-BCB adhesive bonding technology

developed in Ghent University's cleanroom. Later on, the operation speed was improved to 43 Gbit/s and also 56Gbit/s by using an optimized laser structure [25]. The modulation bandwidth of DFB lasers can be further extended by introducing an external feedback to the laser cavity to excite a strong side mode and therefore create a photon-photon resonance [26, 27].

3.8.2 Layout of the transceiver

The layout of the proposed FTTH transceiver is schematically depicted in Fig. 3.31. The C-band transmitter is realized by using a III-V-on-Si integrated DFB laser, which is the transfer-printed DFB laser presented in the second chapter. The O-band upstream signal is received using a micro-transfer-printed O-band TPD. As both the DFB laser and the TPD are integrated through µTP, the overall use of III-V materials is further enhanced. Moreover, the use of the passive SiPh platform rather than the iSiPP25G platform again leads to a reduction in the cost of the transceiver.

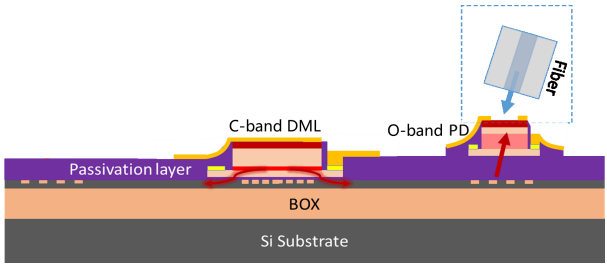


Figure 3.31: Schematic cross-section of the transceiver based on a C-band DML and an O-band TPD.

3.8.3 µTP of pre-fabricated TPDs on a 400 nm passive Si PIC

A thin DVS-BCB layer is first spin-coated on the SOI chip with the already integrated DFB lasers, followed by 10 minutes soft bake on a hot plate at 150 °C. Before transfer printing, the TPD is orientated to be in line with that of the reflectionless GC to simplify the alignment, as depicted in Fig. 3.32. After the encapsulation photoresist was removed, the sample is loaded in an oven to cure the DVS-BCB bonding layer. Different from the integration on a tiny iSiPP25G sample, here a 2 µm thick DVS-BCB layer is spin-coated over the PIC to planarize the micro-transfer-printed TPD. After etching back and opening the p- and n-metal

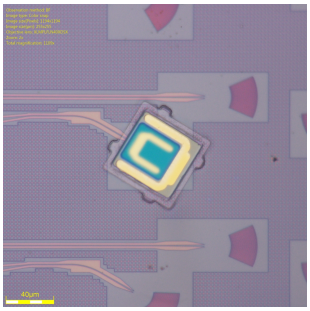
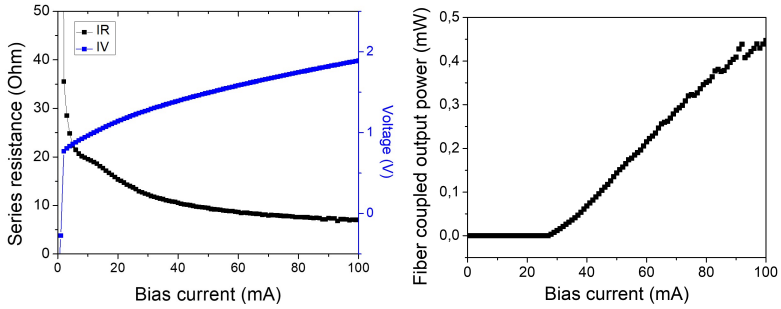


Figure 3.32: Microscope image of a micro-transfer-printed TPD on a low reflection fibre GC.

contacts, a final metallization is performed to define probing pads. The fabrication is finalized by exposing the contact pads of the DFB laser by RIE dry etching.



(a) (b)

Figure 3.33: Performance of the DFB laser. (a) V-I response and differential resistance (b) P-I curve.

3.8.4 Static characterization

A static characterization at 20 °C was carried out on a vertical setup to investigate the performance of the fabricated transceiver. Firstly the performance of the DML (DFB) is investigated. Fig. 3.33(a) shows the obtained IV curve. It reveals a significantly reduced series resistance of 8 Ω at 70 mA, which used to be 15 Ω before the O-band TPD integration. The origin of this decrease in resistance is not well understood. Thanks to this reduced series resistance and therefore less Joule heat, no obvious thermal roll-off is observed in the recorded PI curve (Fig. 3.33(b)). The maximal optical power collected in the optic fiber probe is about 0.45 mW at a bias current of 100 mA. As the properties of the DFB laser are changed during

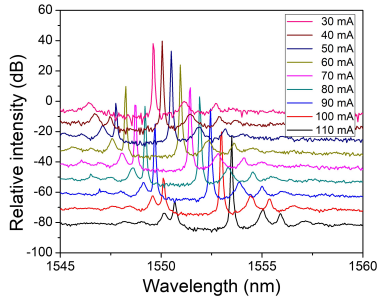


Figure 3.34: Optical spectra of the DFB at different bias current.

the μTP integration, it is difficult to estimate the insertion loss induced by the integrated O-band TPD. However, given a -8 dB insertion loss from the GC at 1550 nm and neglecting the additional loss from the integrated TPD, the waveguide coupled power is at least 4.5 dBm (2.8 mW). As revealed in the recorded spectrum in Fig. 3.34, the threshold current shows an increase of 10 mA and the side mode is much stronger. These changes of the performance might be attributed to the changed external feedback by integrating the TPD. However, it is not expected to impact the application of this transceiver, as no WDM/DWDM device or other wavelength sensitive elements are involved in the P2P communication system.

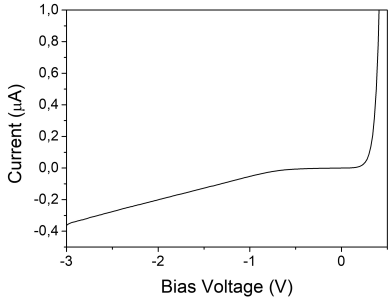
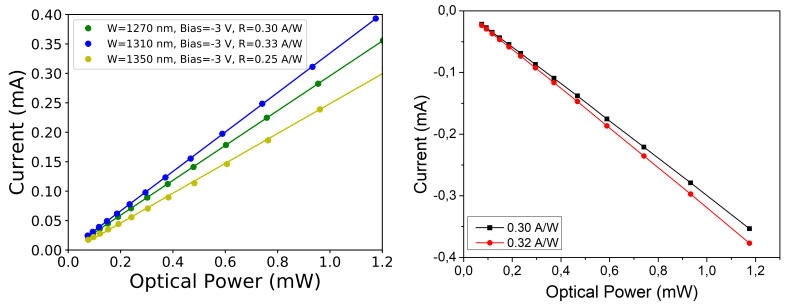


Figure 3.35: Recorded VI response of the transfer-printed O-band TPD.

On the other hand, the responsivity and dark current of the micro-transfer-printed O-band TPD was investigated. Fig. 3.35 shows a recorded V-I response of the integrated O-band TPD. As presented in Fig. 3.23, it reveals an evident increase of the dark current with the increase of the bias voltage, which reaches $0.36\,\mu A$ at -3 V. The responsivity of the integrated TPD is found to be 0.25-0.33 A/W over the entire O-band, as shown in Fig. 3.36(a).The polarization dependence of the PD at 1310 nm is about 6.6% (Fig. 3.36(b)), which agrees well with what has been observed in the previous demonstration (6%).



(a) (b)

Figure 3.36: Photocurrent of the micro-transfer-printed O-band TPD (a) over the range of 1270 nm-1350 nm, (d) at 1310 nm under different polarization conditions.

3.8.5 Dynamic characterization

A back-to-back high-speed measurement was carried out at 20 °C. In the characterization, the μ-transfer-printed TPD and the DFB laser were biased at -3 V and at 100 mA (which corresponds to a bias voltage of 1.9 V), respectively. A resulting laser spectrum is shown in Fig. 3.37, which reveals a 30 dB side mode suppression. A voltage swing of 1.8 V was applied to the DFB laser via a bias tee. As the resistance of the DFB laser is much less than 50 Ω (8 Ω), the voltage swing applied on the device is significantly reduced because of the RF reflection due to a large impedance mismatch.

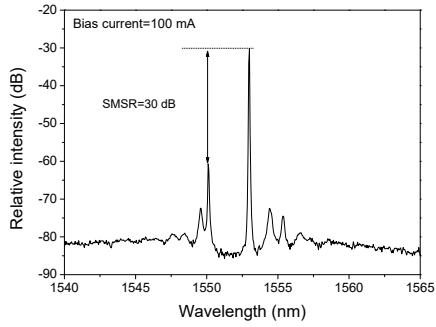


Figure 3.37: Optical spectrum of the DFB laser at a bias current of 100 mA.

The transceiver was demonstrated at 10 Gbit/s and 12.5 Gbit/s. In the measurement, the downstream transmitter (DFB laser) and the upstream receiver (transfer-

printed O-band TPD) were simultaneously operating at the same speed. Fig. 3.38 shows overlaid eye diagrams of the upstream (O-band), and the downstream (C-band) signals at 10 Gbit/s with average received optical power of 0 dBm on each receiver.

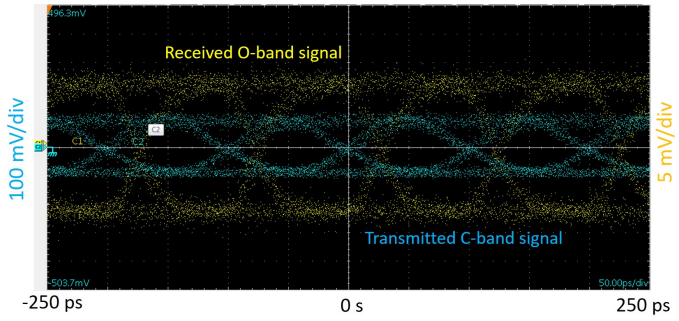


Figure 3.38: Overlaid 10 Gbit/s eye diagrams of the upstream (O-band) data signal and downstream (C-band) data signal.

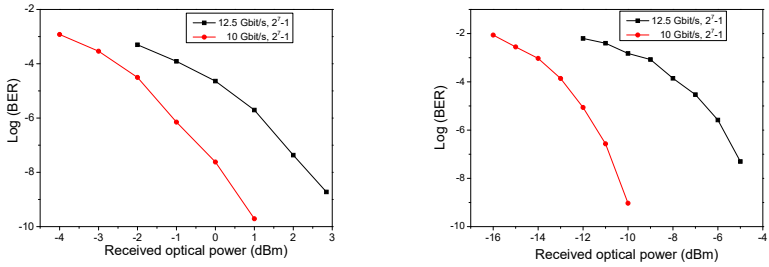
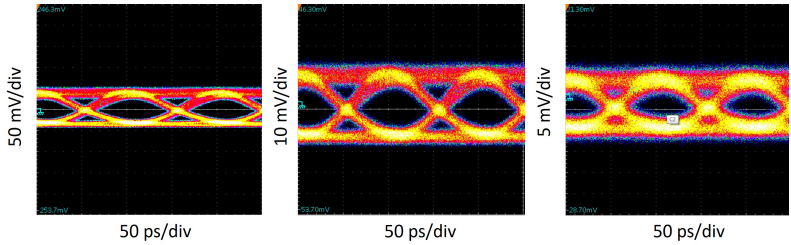


Figure 3.39: Measured BER versus received optical power for (a) the upstream data signal, (b) the downstream data signal.

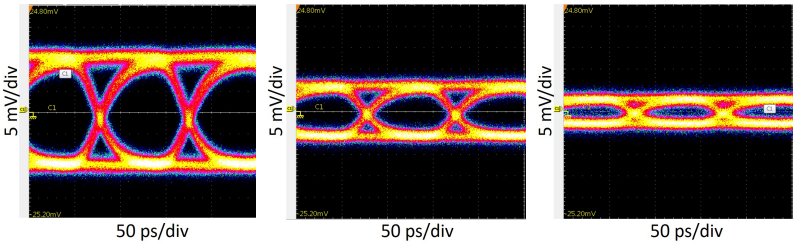
Fig. 3.39 shows the recorded BERs at 10 Gbit/s and 12.5 Gbit/s with a pattern length of 2^7-1. Compared with the performance of the 4-channel transceiver presented in the previous section, a higher averaged input power (1 dBm) is required for error-free operation at 10 Gbit/s for the upstream receiver(micro-transfer-printed O-band TPD). While it remained the same (2.8 dBm) when operating at 12.5 Gbit/s. Vice versa, error-free operation for the downstream signal was realized at an input power of -10 dBm and -5 dBm for 10 Gbit/s and 12.5 Gbit/s operation (2^7-1), respectively. Fig. 3.40 shows the eye diagrams of the 1550 nm downstream signal with -4 dBm, -8 dBm and -12 dBm received optical power, while that of the

1310 nm received downstream signal with 0 dBm, -3 dBm and -6 dBm received power is shown in Fig. 3.41.



(a) (b) (c)

Figure 3.40: Measured 10 Gbit/s downstream signal at 1550 nm with average received optical power of,(a) -4 dBm,(b) -8 dBm,(c) -12 dBm.



(a) (b) (c)

Figure 3.41: Measured 10 Gbit/s upstream signal at 1310 nm with average received optical power of,(a) -0 dBm,(b) -3 dBm,(c) -6 dBm.

3.9 Conclusion

In this chapter, we presented two different transceivers for P2P FTTH networks on the CO side. In both of the demonstrations, the III-V material and/or III-V devices were integrated on Si PICs through µTP. In the first phase, we successfully demonstrated a 4-channel transceiver array by taking advantage of high-speed Si micro-ring modulators realized on the imec iSiPP25G platform. The upstream (O-band) receivers were demonstrated using an array of µ-transfer-printed O-band III-V TPDs. To our best knowledge, this is the first III-V-on-Si PIC realized by µTP of pre-fabricated III-V devices. A responsivity of 0.39-0.49 A/W was obtained for the O-band signal, with four orders of magnitude lower responsivity for the C-band

signal. Such a high responsivity contrast allows a low cross-talk between upstream and downstream data signals. Error-free operation for a NRZ 2^7-1 data stream at 10 Gbit/s was realized at a received power of 0 dBm and -11 dBm for upstream (without TIA) and downstream (with TIA) data signals, respectively. In the second part, we demonstrated a single channel FTTH transceiver based on a C-band III-V-on-Si integrated DFB laser and an O-band III-V TPD, which are both integrated on a Si PIC through μTP. Despite a lower sensitivity ($\sim$ 0.3 A/W) of the integrated TPD for the O-band signal and a degraded SMSR of the C-band DFB laser, the transceiver was successfully demonstrated at 10 Gbit/s and 12.5 Gbit/s. Thanks to the compact size and potentially low cost brought by the μTP technique, the demonstrated transceivers reveal a great opportunity for practical applications. On the other hand, they showcase the feasibility and enormous potential that μTP has for the integration of non-compatible components, notably III-V structures and/or devices on a Si PIC with significant flexibility.

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4

Micro-transfer-printed III-V-on-Si widely tunable narrow linewidth lasers

In the second chapter, we presented III-V-on-Si integrated DFB lasers based on the micro transfer printing (μTP) of III-V material on Si photonic integrated circuits (PICs). In this way the efficiency of the use of III-V material is significantly improved. Nevertheless, a time-consuming post-processing is required to define the III-V taper structures in the μ-transfer-printed III-V material coupons. To simplify the fabrication and to pursue an ultimate low-cost solution, we propose to transfer print pre-fabricated devices rather than material coupons in this work. As a proof of concept, two different fiber-to-the-home (FTTH) transceivers were successfully demonstrated, as presented in the third chapter. Following the success of the μTP of pre-fabricated TPDs, in this chapter we aim at demonstrating III-V-on-Si widely tunable and narrow linewidth lasers, suitable for coherent communication (<500 kHz intrinsic linewidth) [1, 2], through the same approach : μTP of pre-fabricated SOAs on Si PICs, which are realized on the imec 400 nm Si photonic platform. To accommodate the alignment accuracy (± 1.5 μm, 3σ) that can be obtained by the μTP system (X-Celeprint μTP-100 tool) and to achieve an efficient mode conversion between the III-V layer and the underlying Si waveguide, an alignment-tolerant III-V/Si taper structure is proposed. In the first section, we will investigate a few components that will be used in the laser cavity design. To investigate the laser cavity design and to verify the feasibility of the integration of widely tunable lasers on the imec 400 nm photonic platform, we first fabricated tunable lasers through the standard DVS-BCB adhesive die-to-wafer bonding. The

design, fabrication and characterization of the tunable laser will be discussed in the second section. Following the success of the first tunable laser demonstration, we proposed an alignment-tolerant III-V taper structure (SOA) that will facilitate the μTP-based integration of III-V-on-Si lasers. The design and pre-fabrication of this proposed SOA on the native III-V wafer will be discussed. In the last section, we will demonstrate widely tunable III-V-on-Si lasers by μTP of pre-fabricated SOAs.

4.1 Widely tunable narrow linewidth laser

In order to cope with the ever-growing demand for higher bandwidth, coherent transceivers for metro-network communication systems have attracted a lot of attention in recent years. These transceivers are complex and expensive so that they were mostly deployed in long-haul communication networks, where the ultra-long fiber links take most of the cost. With shorter fiber links, the cost weight of coherent transceivers is notably increased, which leads to an urgent need for a cost-effective solution for realizing coherent transceivers. Si photonics is emerging as a key photonic integration platform which is able to satisfy this demand, because of its compatibility with CMOS fabrication technology which allows for a low-cost high-volume production of such circuits. As Si does not provide efficient light generation due to its indirect bandgap, there is a need to integrate light sources onto the Si photonic platform. In case of coherent transceivers, narrow linewidth lasers are required not only at the transmitter side to provide the optical carrier, but also at the receiver side as an absolute phase reference to demodulate the phase and intensity of the incoming signal [3, 4]. Moreover, wide wavelength tuning range, typically over the entire C-band and/or L-band, is desired for implementing WDM/DWDM systems. The spectral linewidth of a semiconductor laser is one of the most concerning aspects for a coherent system. The intrinsic results from the spontaneous emission in the gain medium. With a broadening effect attributed to the coupling of phase and intensity, the spectral linewidth is given by [5]:

$$\Delta\nu_{laser} = \frac{\upsilon_g^2 \hbar\nu g_{th} n_{sp} \alpha_m}{8\pi P}(1+\alpha^2) \tag{4.1}$$

$$\alpha_m = -L^{-1} ln(r_m) \tag{4.2}$$

where υ_g represents the group velocity, $\hbar$ is the Planck′s constant and $\hbar\nu$ denotes the photon energy, g_{th} is the threshold gain, n_{sp} is the spontaneous emission factor, α_m is the facet loss and P is the output power from this facet. The laser linewidth can be reduced by using a long laser cavity with low loss (or a high Q-factor laser cavity) [6, 7]. Besides the use of a long and low loss laser cavity, a significant linewidth reduction can be achieved by introducing a negative optical feedback to the main cavity [8–11]. A long laser cavity will result in a small FSR

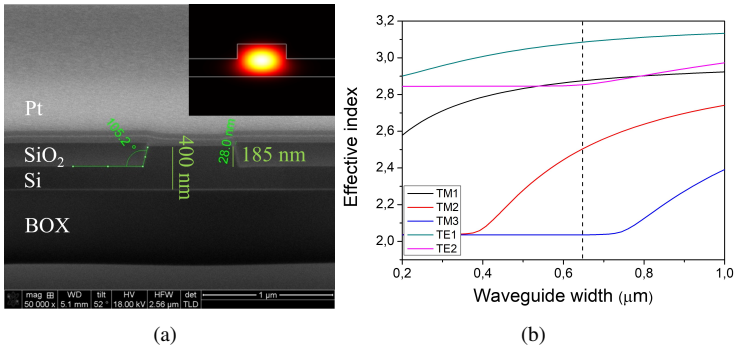
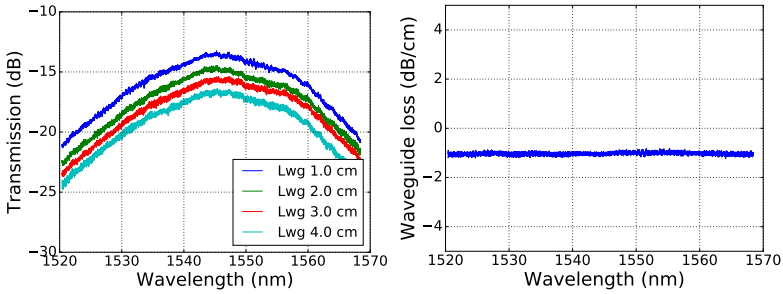


Figure 4.1: (a) An FIB cross section image of a 650 nm wide rib waveguide,(b) The effective indices as function of the rib width for the guided optical modes at a 1550 nm.

of laser cavity modes, which makes it difficult to realize single longitudinal mode operation. To overcome this issue, a narrow band filter, e.g. a ring resonator with a large FSR [12], can be used to select one of the longitude cavity modes. Using the thermo-optic effect of Si, the tuning range of such laser is limited to 10 nm. By incorporating a so-called vernier filter which is formed by cascading a pair of comb filters (micro-ring resonators) with slightly different FSRs in the laser cavity, the tuning range of the laser can be extended to over 40 nm [13, 14].

4.2 Building blocks for widely tunable lasers

In this section, we briefly introduce some building blocks developed on the imec 400 nm Si photonic platform, which was already discussed in the second chapter. This platform has a 400 nm thick Si device layer and a 2 µm thick buried oxide layer. The Si waveguide is realized by a 180 nm deep single step dry etching. The use of 400 nm thick Si layer is essential for the optical coupling between the III-V and Si waveguide layer. The III-V-on-Si integrated lasers that have been demonstrated on this platform by the Photonics Research Group are mostly stand-alone lasers. For example, DFB lasers that merely consist of a DFB grating and a pair of GCs (GCs) to interface with optical fiber. In order to increase the complexity and to improve the performance of PICs which are realized in this 400 nm Si photonic platform, a variety of essential components have to be developed, e.g., low loss waveguides, fiber GCs, MMIs, ring resonators, directional couplers etc.



(a) (b)

Figure 4.2: Measured transmission spectra for a set of waveguides with different length,(b) Calculated propagation loss of the fundamental TE mode in 650 nm wide rib waveguide.

4.2.1 Single TE mode waveguide

Fig. 4.1(a) shows an SEM image of the cross-section of a 'standard' single TE-mode waveguide, which has a 650 nm wide core width. The etch step in the cladding region is 185 nm with a 85° sidewall angle. The inset shows the intensity distribution of the fundamental TE mode. Fig. 4.1(b) shows the effective indices of the guided modes as a function of waveguide width at 1550 nm. The simulation is performed using FIMMWAVE. As can be seen, the waveguide does not support high order TE modes below 650 nm width, therefore 650 nm is used as the standard waveguide width. The propagation loss of the fundamental TE mode in this waveguide is investigated by comparing the transmission of a set of waveguides with different lengths. Fig. 4.2(a) shows the transmission spectra of a set of waveguides with length of 1 cm, 2 cm, 3 cm, and 4 cm. The propagation loss is extracted by implementing a linear fitting to the measured transmission spectra as a function of waveguide length. As shown in Fig. 4.2(b), the propagation loss is found to be 1 dB/cm over the 1520 nm to 1570 nm wavelength range.

4.2.2 Microring resonators

Microring resonators play a considerable role in Si PICs because of their versatility. In general a ring resonator is formed by a looped waveguide and one or two bus waveguides. The first case is named all-pass ring resonator, while the second case is called add–drop ring resonator on the other hand. Thanks to a low waveguide loss, an ultra-high Q-factor and low insertion loss can be achieved. The high index contrast between Si and SiO_2 (or air) cladding allows for microring resonators with ultra-small footprint and thus large FSR. These merits make ring resonators attractive in a variety of applications, including optical (de)multiplexers [15, 16],

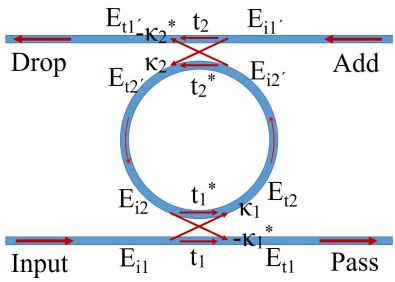


Figure 4.3: Model of an add–drop ring resonator.

optical delay lines [17], optical sensors [18, 19], high speed modulation [20], reservoir computing [21], frequency comb generation [22] and so on.

4.2.3 Properties of an add–drop ring resonator

Fig. 4.3 shows a schematic layout of an add-drop ring resonator, which consists of two directional couplers in the transfer matrix model. The transfer matrix of the coupling section at bottom is written as:

$$\begin{bmatrix} E_{t1} \\ E_{t2} \end{bmatrix} = \begin{bmatrix} t_1 & \kappa_1 \\ -\kappa_1^* & t_1^* \end{bmatrix} \begin{bmatrix} E_{i1} \\ E_{i2} \end{bmatrix}$$

Where E_{in} and E_{tn} denote the indent and transmitted field, respectively, t_n and κ_n represent the self-coupling and cross-coupling coefficient, respectively. Here we assume the coupling section is lossless so that t and κ satisfy

$$|t_n|^2 + |\kappa_n|^2 = 1 \tag{4.3}$$

After traveling through a half ring the optical field is expressed as:

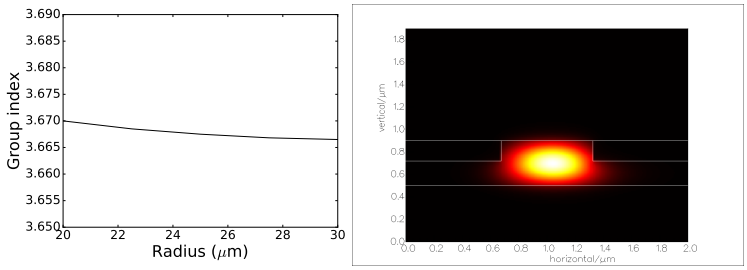
$$E_{i2'} = E_{t2} * \alpha^{1/2} e^{i\phi/2} \tag{4.4}$$

where α and ϕ represent the single-pass amplitude transmission and phase shift, respectively. Assuming that there is no back-scattering or reflection in the ring resonator, a part of the incident field is coupled to the drop port and, the rest is coupled to the pass-port. The transfer matrix of the add-drop ring is as such:

$$\begin{bmatrix} E_{t1} \\ E_{t1'} \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix} \begin{bmatrix} E_{i1} \\ E_{i1'} \end{bmatrix}$$

where s_{21} is expressed as:

$$s_{21} = -\frac{\kappa_1 \kappa_2 \alpha^{1/2} e^{i\phi/2}}{1 - t_1 t_2 \alpha e^{i\phi}} \tag{4.5}$$



(a) (b)

Figure 4.4: (a) Group index as a function of bend radius for TE_{00} mode at 1550 nm,(b) The profile of TE_{00} mode in a 650 nm width rib waveguide with $25\,\mu\mathrm{m}$ bend radius.

The drop-port intensity transmission is obtained by squaring s_{21}:

$$T_{drop} = \frac{{\kappa_1}^2{\kappa_2}^2\alpha}{1 + {t_1}^2{t_2}^2\alpha^2 - 2\alpha t_1 t_2 cos\phi} \tag{4.6}$$

The effective phase delay induced by the ring resonator can be calculated from Eq. 4.5:

$$\Phi_{drop} = arg(\frac{E_{t1}^{'}}{E_{i1}}) = arg(s_{21}) = \frac{\phi}{2} + arctan(\frac{\alpha t_1 t_2 sin\phi}{1 - \alpha t_1 t_2 cos\phi}) \tag{4.7}$$

The free spectral range (FSR) of the transmission spectrum is determined by the perimeter of the ring resonator and the group index at the wavelength of interest:

$$FSR_r = \frac{\lambda^2}{2\pi R_r n_g} \tag{4.8}$$

Where λ and n_g represent the operation wavelength in vacuum and the group index of the optical mode, R_r is the radius of the micro-ring resonator.

In this work, a microring based Vernier filter will be used in the laser cavity for achieving over 40 nm tuning range. Therefore the target combined FSR of such a Vernier filter is 40 nm. The ring resonators will be designed with 650 nm wide rib waveguide. As a start, the FSR of one micro-ring is set around 4 nm. Fig. 4.4 shows the simulated group index of the fundamental TE mode as a function of bend radius. Given a group index of 3.67 at 1550 nm, the radius of one ring is decided to be $25\,\mu\mathrm{m}$, which leads to an FSR of 4.17 nm according to Eq. 4.8

For a Vernier filter that consists of two ring resonators with slightly different FSRs, the eventual combined FSR, or maximal tuning range, is given by

$$FSR_{vn} = \frac{FSR_{ring1} \times FSR_{ring2}}{|FSR_{ring1} - FSR_{ring2}|} \tag{4.9}$$

Therefore to achieve 40 nm tuning range, the FSR of the other ring resonator (FSR_{ring2}) should be 4.44 nm or 3.65 nm, which corresponds with a radius of $22.5\,\mu\mathrm{m}$ or $27.5\,\mu\mathrm{m}$, respectively. In this work, the larger radius ($27.5\,\mu\mathrm{m}$) is used for the other ring resonator to have a high Q-factor due to the lower bend loss. On the other hand, S-shaped bent bus waveguides rather than straight waveguides are used to reduce the parasitic reflections and to avoid splitting of resonances [23, 24]. The bend radius of the coupling section is $30\,\mu\mathrm{m}$. An SEM picture is shown in Fig. 4.5. Fig. 4.6(a) and Fig. 4.6(b) show transmission spectra of the $25\,\mu\mathrm{m}$ and $27.5\,\mu\mathrm{m}$radius add-drop rings, for which the measured free spectral range (FSR) around 1550 nm is 4.03 nm and 3.66 nm, respectively. Besides the FSR of the ring resonators, the loaded Q-factor and the drop-port insertion loss are of importance, as they will determine the linewidth of the laser. As the basic layout of the ring resonator has been fixed, the transmission properties are mainly determined by the coupling ratio of the directional coupler. Therefore a set of ring resonators with different coupling gaps ranging from 200 nm to 450 nm are investigated. A higher loaded Q-factor can be achieved by using directional couplers with larger coupling gap (lower cross coupling ratio). As a trade-off the drop port loss will be higher. Fig. 4.6(c) shows a representative spectrum of a ring resonator with 300 nm coupling gap around 1550 nm, revealing a loaded Q-factor of 19400. The measured loaded Q-factor and drop port loss as a function of coupling gap are shown in Fig. 4.6(d).

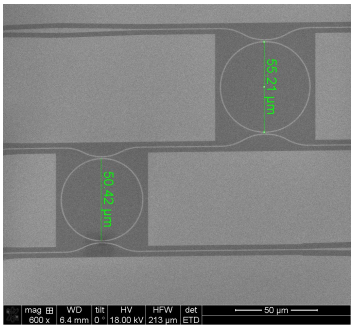


Figure 4.5: Microscope image of a Vernier filter based on cascaded ring resonators with slight different radius.

4.2.4 DBR reflector

Besides narrowband filters, broadband reflectors are also required in some PICs. Sagnac loop mirrors based on a closed loop splitter(1×2, 2×2 MMI or a directional coupler) are usually used as a broadband mirror [14, 25–28]. As an alternative, Bragg gratings that have a compact footprint are also widely adopted. The

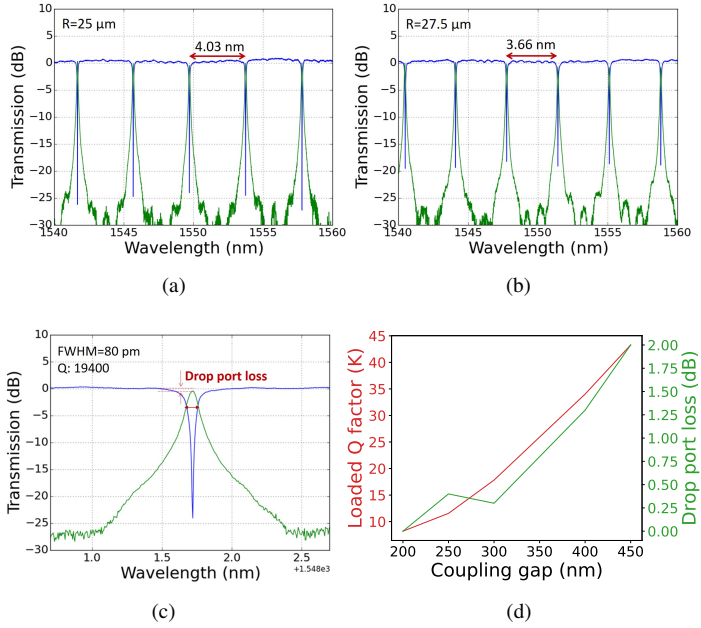


Figure 4.6: Drop port and through port transmission spectra of ring resonators with a radius of (a) 25 µm and (b) 27.5 µm, showing an FSR of 4.03 nm and 3.66 nm around 1550 nm, respectively. (c) A resonance spectrum around 1550nm, showing a loaded Q-factor of 19400, (d) The measured loaded Q-factor and drop port loss as function of the coupling gap.

central wavelength of a Bragg grating is determined by the Bragg condition:

$$\lambda_{bragg} = \frac{2n_{eff}\Lambda}{m} \tag{4.10}$$

$$R_{bragg} = \left[tanh(\kappa L_{bragg}) \right]^2 \tag{4.11}$$

Where n_{eff} is the effective index of the propagating mode along the Bragg grating, m and Λ represent the diffraction order and period of the grating, respectively. First order gratings with 50% duty cycle are preferable to have a broad stopband and low loss [29]. To eliminate additional scattering loss in the lateral direction, a wide (e.g. 2 µm) waveguide is usually used and is connected to the waveguide circuit via an adiabatic taper. The effective index of the grating (n_{eff}) can be roughly estimated by averaging the effective indices in the etched and unetched segments. Care has to be take in the design as the feature size of the grating is small, a 60% duty cycle is usually obtained for a 50% duty cycle design due to

the exposure dose used in the process, therefore the target duty cycle is set to be 60% in the simulation. Given a $2\,\mu m$ wide Bragg grating, the simulated refractive indices of these segments are 2.85 and 3.19, respectively, for a 180 nm etch depth. Therefore the period of the DBR with a target Bragg wavelength at 1560 nm is found to be 255 nm according to Eq. 4.10. The stopband of the DBR is mainly determined by the coupling strength (or index contrast of the grating). The reflectivity of the DBR is determined by the product of coupling strength and grating length (Eq. 4.11). Fig. 4.7(a) shows the simulated reflection spectra of DBRs for different length (number of periods). The simulation is performed using Lumerical FDTD. Given a large index contrast (0.34) and thus a high coupling coefficient, over 100 nm stop band which covers the entire C- and L-band is achieved. The reflectivity at the center wavelength (1560 nm) increases with grating length and saturates at $95\,\%$ with 30 periods, as shown in Fig. 4.7(b). Unfortunately, it is not straight forward to characterize the wavelength response of the DBR due to the relatively narrower operation bandwidth of our GCs. As shown in Fig. 4.7(c), only a slight wavelength shift is observed when the etch step varies, which leads to a relaxed tolerance in the PIC fabrication. The wavelength shift with respect to grating period is shown in Fig. 4.7(d).

4.3 III-V-on-Si widely tunable laser based on DVS-BCB bonding

4.3.1 Design of the tunable laser

In [13], a III-V-on-Si integrated widely tunable laser with a ring-loop cavity was demonstrated by J. C. Hulme and *et. al.* at UCSB in 2013. Over 40 nm tuning range with 35 dB SMSR was achieved by using a microring-based Vernier filter. The maximum waveguide coupled power and the linewidth were found to be 3.3 mW and 338 kHz, respectively. These ring cavity lasers have a common issue of mode competition between the counter-propagating modes. The most straight forward approach to suppress this competition is by incorporating a non-reciprocal loss element (e.g. an isolator) in the laser cavity to kill one circulating mode while leaving its counter-propagating mode circulating. There are some proposed approaches for the integration of isolators on Si PICs, e.g. by flip-chipping magneto-optic materials on PICs or by using cascaded phase modulators [30–32]. Because the complexity of the device layout, complicated fabrication steps and high insertion loss, these devices are not suitable for inserting in a laser cavity. More practical routes have been evaluated to realize unidirectional lasing, including the use of an S-bend SOA in a ring-shaped laser cavity [33], a snail shape laser [34] or a reflector coupling the CW and the CCW mode [35, 36]. The latter approach is followed in this work.

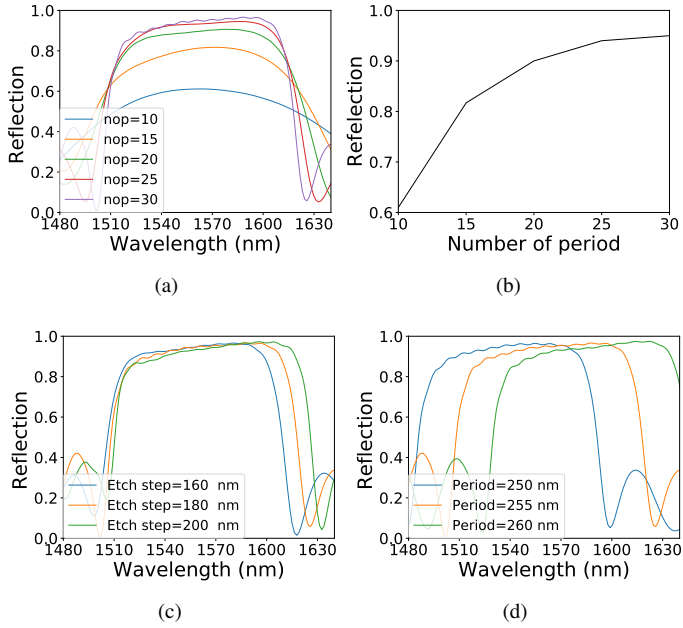


Figure 4.7: (a) Simulated reflection spectra of DBR with different number of grating periods. (b) The reflectivity as a function of the number of periods. (c) Reflection spectra of DBR with different etch steps, (d) Reflection spectra of DBR for different periods.

Fig. 4.8 shows a schematic layout of the proposed laser structure, which has a ring laser cavity that is formed using two micro-ring resonators with a III-V gain section in between. The ring resonator structures have a ring radius of $25\,\mu\mathrm{m}$ and $27.5\,\mu\mathrm{m}$. The gap between the ring resonator waveguide and bus waveguide (both 650 nm wide) is 300 nm, which corresponds to a loaded Q-factor of around 19K. The III-V gain section is $400\,\mu\mathrm{m}$ long, excluding the $180\,\mu\mathrm{m}$ long adiabatic tapers for coupling to the Si waveguide layer. The III-V mesa is $3.2\,\mu\mathrm{m}$ wide in the gain section. Out-coupling is realized using a directional coupler structure. The length of the directional coupler is $15\,\mu\mathrm{m}$ and the gap is 350 nm, leading to a coupling of $45\,\%$ to $50\,\%$ in the 1560 nm to 1600 nm wavelength range (i.e., the tuning range of the presented device). So-called reflectionless GCs are used to interface with optical fiber (GC1 and GC2) and to terminate the waveguides as well as to ensure a low external reflection to the laser cavity (-30 dB). Ti/Au micro-heaters are integrated on the ring resonators for wavelength tuning. A phase section is incorporated in the laser cavity by adding a Ti/Au micro-heater on top of the Si waveguide between the two ring resonators.

The laser linewidth is inversely proportional to cavity length and output power.

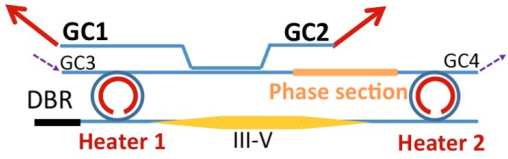


Figure 4.8: Schematic of the unidirectional, widely-tunable and narrow-linewidth III-V-on-Si laser.

Because the Si rib waveguide defined in the 400 nm platform has a low loss ($\sim$ 1 dB/cm), a long cavity can be used to increase the photon lifetime and to reduce the laser linewidth. To ensure single mode operation, the eventual longitudinal mode interval should be comparable with the full width at half maximum (FWHM) of the Vernier filter transmission spectrum.

Assume the two micro-rings have the same loaded Q-factor and are spectrally aligned, the effective cavity round trip phase shift is given by

$$\Phi_{cavity} = 2\Phi_{ring} + \Phi_{WG} + \Phi_{IIIV} \tag{4.12}$$

Fig. 4.9 shows a normalized simulated transmission of the ring-based Vernier filter and the cavity roundtrip phase as a function of wavelength. The physical cavity length is $6\,\mathrm{mm}$. Although the phase delay in the micro-rings results in a narrower longitudinal mode spacing at resonance, the FWHM of the two-ring transmission spectrum is comparable to the longitudinal mode spacing, which allows for single mode operation. If the lasing longitudinal mode is not exactly aligned with the resonance peak (which can be achieved by tuning the phase section), the strength of the coupling between the CW and CCW mode by the DBR can be enhanced due to the increased transmission to the through port of the rings, resulting in unidirectional operation. At the same time, the strong wavelength dependence of the cavity loss is helpful for narrowing the linewidth (when positioned on the long wavelength side of the resonance peak). This effect is known as detuned loading [8].

4.3.2 III-V epitaxial material for bonding-based laser integration

The III-V epitaxial layer stack used in this demonstration is shown in Table. 4.1. It consists of a 200 nm thick n-InP contact layer, two 100 nm thick InGaAsP separate confinement heterostructure layers (bandgap wavelength $1.17\,\mu\mathrm{m}$), 6 InGaAsP quantum wells (7 nm thick, emission wavelength $1.58\,\mu\mathrm{m}$) surrounded by 9 nm thick InGaAsP barriers, a $1.5\,\mu\mathrm{m}$ thick p-InP top cladding (graded doping from $5 \times 10^{18}\,\mathrm{cm}^3$ to $5 \times 10^{17}\,\mathrm{cm}^3$ at the active region) and a 200 nm heavily doped p-InGaAs contact layer. A 200 nm thick InGaAs layer and a 200 nm InP

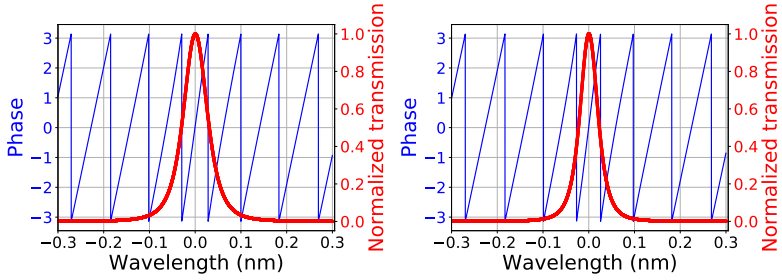


Figure 4.9: Normalized simulated transmission of two spectrally aligned ring resonators and the cavity roundtrip phase as a function of wavelength for rings with a loaded Q factor of (a) 15000 and (b) 20000.

layer are grown on the top as sacrificial layers to protect the layer stack and to ensure a clean surface in the bonding process.

4.3.3 Laser fabrication via DVS-BCB adhesive bonding

The Si waveguide circuits are planarized using SiO_2 deposition and chemical mechanical planarization (CMP) down to the Si device layer, using the SiN hard mask as the polish stop, which is afterward removed using a hot phosphoric acid wet etch. The laser fabrication was carried out in the Ghent University cleanroom, following the standard III-V-on-Si integration process flow established in the Photonics Research Group.

4.3.3.1 DVS-BCB adhesive bonding

As the fabricated PICs were delivered as an undiced 200 mm wafer with a photoresist protection layer from imec, the first step is to dice out a sample with a size around $2 \times 2\,\mathrm{cm}^2$ and with the desired structures in the center to enable the post-processing on it. Care has to be taken in this step to avoid the sample from being contaminated. The die-to-wafer bonding follows the standard process flow [37]. A 1:8 DVS-BCB (CYCLOTENE 3022-35):Mesitylene solution is first spin-coated on the sample at 3000 rpm for 40 seconds, followed by a 15 minutes soft bake at $150\,^{\circ}\mathrm{C}$ to let the mesitylene solvent evaporate. After slowly cooling down to room temperature, the Si chip is ready for bonding. On the other hand, a $7.5 \times 10\,\mathrm{mm}^2$ III-V chip is diced out from a 2-inch III-V epitaxial wafer. The III-V die is then cleaned using acetone, IPA and DI water, after which the InP and the InGaAs sacrificial layers are removed by sequentially immersing in $37\,\%$ HCl and in a 1:1:18 H_2SO_4:H_2O_2:H_2O piranha etchant for 40 seconds and 2 minutes, respectively. To

Table 4.1: III-V epitaxial layer stack for bonding-based integration

Layer	Layer type	Material	Thickness (nm)	Doping level (cm^{-3})	Refractive index
26	Sacrificial	InP	200		3.17
25	Sacrificial	InGaAs	200		3.6
24	N cladding	InP	190	1×10^{18}	3.17
23	SCH	InGaAsP	100		3.321
11×6	QW	InGaAsP(Q1.55) 0.8 % compressive strain	7		3.54
10×7	Barrier	InGaAsP(Q1.17) 0.3 % tensile strain	9		3.32
9	SCH	InGaAsP	100		3.321
8	Cladding P	InP	500	5×10^{17}	3.169
7	Cladding P	InP	1000	2×10^{18} ~ 5×10^{17}	3.17
6	Transition	InGaAsP(Q1.2)	10	$>3 \times 10^{18}$	3.35
5	Transition	InGaAsP(Q1.4)	10	$>3 \times 10^{18}$	3.44
4	Contact P	InGaAs	200	$>1 \times 10^{19}$	3.17
3	Sacrificial	InP	200		3.17
2	Stop etch	InGaAs	200		3.6
1		InP	50		3.17
0	Substrate	InP			3.17

improve the adhesion of III-V material to the Si layer, 10 nm thick SiO_2 is deposited on top of the exposed n-InP layer in a plasma-enhanced chemical vapor deposition (PECVD) tool. Then the III-V die is placed upside down on the Si photonic chip, covering the area where it is desired. Note that the III-V die has to be oriented with its $[01\bar{1}]$ crystal axis paralleling to the long side of the III-V gain section to ensure a 'V' shape cross-section of the InP mesa. Then the samples are sandwiched by two Pyrex wafers and are fixed on a transport wafer holder with three clamps. After that, the sample is loaded into a wafer bonding machine (Suss MicroTec's ELAN CB6L). The bonding procedure is performed in a series of steps. Firstly the chamber is pumped down to 1×10^{-3} bar; at the same time, the temperature is ramped at a rate of 15 °C/min. When the temperature in the chamber reaches 150 °C, a 300 kPa pressure is applied onto the loaded sample. After 10 minutes stabilization, the temperature is then raised to 280 °C. A low ramp of 1.5 °C/min is used in this step to ensure a uniform DVS-BCB bonding layer. When the temperature reaches 280 °C, nitrogen is purged in the chamber.

This condition is then kept for an hour to cure the DVS-BCB bonding layer fully. When this curing step is complete, the chamber is cooled down to $50\,^{\circ}\mathrm{C}$ at a rate of -$8\,^{\circ}\mathrm{C}$/min. By then, the sample can be unloaded from the chamber.

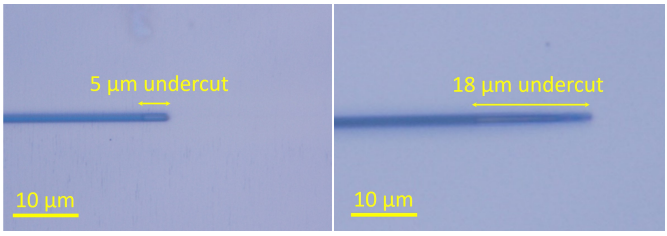
4.3.3.2 InP substrate removal

Normally pure HCl is used to remove the InP substrate, but it always leaves a thick 'ear' at the edge of the III-V die due to the anisotropic wet etch of InP in HCl, as an example shows in Fig. 4.10. This 'ear' can be avoided by using a diluted HCl etchant (e.g. 3:1 HCl:H_2O) at $40\,^{\circ}\mathrm{C}$. After the InP substrate removal, the sample is immersed in a 1:1:18 H_2SO_4:H_2O_2:H_2O piranha solution for 90 seconds and then dipped in pure HCl for 40 seconds to remove the 200 nm thick InGaAs etch stop layer and the 200 nm InP sacrificial layer, respectively.

Figure 4.10: Residual InP (named 'ear') at the sides of the bonded III-V material.

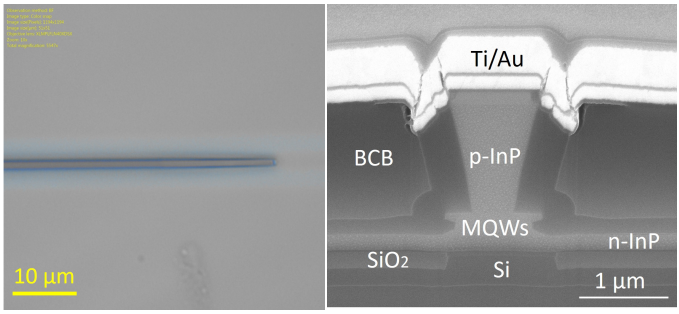
4.3.3.3 Mesa definition

After the p-InGaAs contact layer is exposed, the sample is loaded in a PECVD tool to deposit a 10 nm thick SiO_2 layer and a 300 nm thick mixed-frequency (MF) SiN layer as a hard mask for the following processes. The first SiO_2 layer is used to improve the adhesion between InP and SiN. The deposition is performed at $270\,^{\circ}\mathrm{C}$. The laser mesa is defined through optical contact lithography with MIR 701 photoresist. A good vacuum contact is a prerequisite for realizing a small feature size. After developing the exposed photoresist, an RIE dry etching using a gas mixture of CF_4:H_2:SF_6 (80 sccm:7 sccm:3 sccm) is performed to transfer the patterns from the photoresist soft mask to the SiN layer, after which the resist mask is removed by rinsing in acetone, IPA and DI water. To avoid undercut of p-InGaAs, 11 cycles of ICP dry etching is performed to etch through the InGaAs layer and 300 nm into the p-InP layer, followed by a wet etching in a room temperature 1:1 HCl:H_2O etchant. The duration of this wet etching has to be carefully controlled to avoid undercut of the p-InP in the taper section. Fig. 4.11(a) shows microscope images of a mesa taper after a two-step HCl etching (7 minutes and 2 minutes), which results in a $5\,\mu\mathrm{m}$ undercut from the taper tip inwards. After this etching, the color of the exposed surface is still not uniform, which indicates some residual



(a) (b)

Figure 4.11: Microscope image of a p-InP mesa taper with (a) a $5\,\mu m$ and (b) a $18\,\mu m$ undercut from the taper tip inwards.



(a) (b)

Figure 4.12: (a) Microscope image of a laser mesa taper tip after the active region definition, (b) FIB cross section of the III-V/Si hybrid waveguide structure, showing a V-shape p-InP mesa.

p-InP, therefore a few short dips in the HCl etchant is carried out to remove the remaining p-InP. Fig. 4.11(b) shows a microscope image of the resulting taper with a $18\,\mu m$ undercut. As the length of the InP mesa taper is designed to be more than long enough ($180\,\mu m$), this undercut can be tolerated.

4.3.3.4 Active region patterning

The active region is patterned through a self-aligned approach: a 200 nm thick mixed frequency SiN layer is first deposited, followed by RIE dry etching to transfer the shape of the already defined p-InP mesa to the SiN layer, which is then used as a hard mask for the QW patterning. In this way, the QW mesa can be perfectly aligned to the p-InP mesa and the fabrication is substantially simplified by skipping a contact lithography process. To avoid a deep lateral undercut in the active layers, four cycles of ICP etching is at first performed to etch down 200 nm

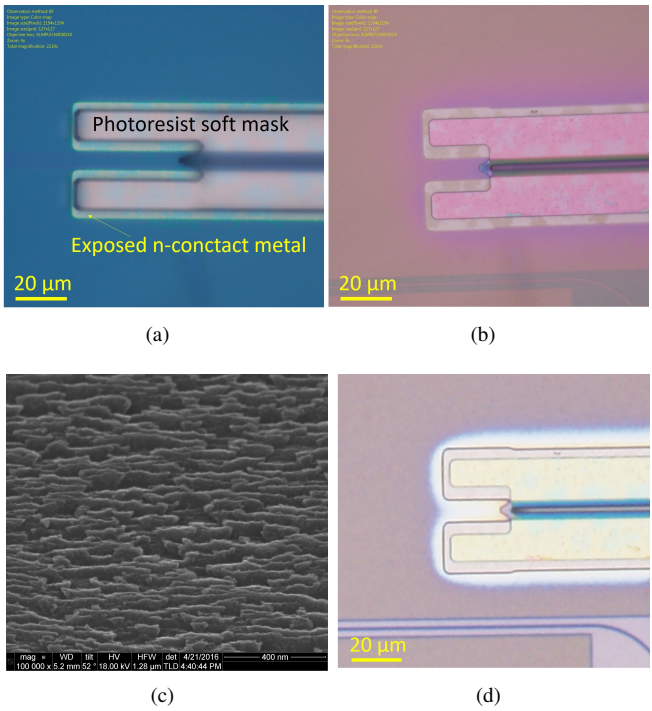


Figure 4.13: Metal re-deposition occurred in the RIE dry etching, hindering the n-InP etching in HCl. Microscope image of a device (a) with photoresist mask and (b) after the SiN hard mask patterning, (c) An SEM image of the exposed n-InP surface after a short HCl wet etching, showing a rough surface, (d) Microscope image of a device after the n-InP was completely removed.

InGaAsP. The remaining active layers are then removed using a room temperature 1:1:10 H_2SO_4:H_2O_2:H_2O piranha, which provides an etch rate of 25 nm/min for InGaAsP. When thinning down the active layers, a profilometer can be used to check the etching progress. Once the n-InP layer is exposed, a short over etching can be performed to narrow down the QW taper tip. Fig. 4.12(a) show a microscope image of a resulting taper tip after this procedure and Fig. 4.12(b) is an FIB cross-section image of a fabricated device $90\,\mu m$ inwards from the taper tip.

4.3.3.5 N-type contact metal deposition and island definition

A standard metal layer stack (Ni/Ge/Au/Ti/Au) is used for the n-metal contact. After which the sample is dipped in a 1:1:20 H_2SO_4:H_2O_2:H_2O etchant for 5 seconds to remove the native oxide. Then a 400 nm thick SiN layer is deposited

to passivate the exposed active layers and also as a hard mask to define the island. Here a mistake was made in the contact mask design, where the size of the island is too small to cover the n-type metal contact, as shown in Fig. 4.13(a). It results in a re-deposition of the exposed Au onto the n-InP layer during RIE etching, which consequently hinders the etching of n-InP in HCl. As shown in Fig. 4.13(b), the gradient color around the n-type contact metal indicates the presence of re-deposited Au. With this re-deposited Au, the etch rate of the n-InP in 1:1 HCl:HO_2 is found to be less than 20 nm/min, and a rough surface was observed after etching, as an SEM image shows in Fig. 4.13(c). In order to etch down the remaining n-InP and to ensure a good electrical isolation, a 1 minute ICP dry etching is performed, followed by immersing in a fresh room temperature 1:1 HCl:H_2O solution to clean up the surface. Fig. 4.13(d) shows a microscope image of a device after the island definition. As can be seen, most of the area shows a uniform color, which means most of the n-InP has been removed. To avoid the above etching issue caused by Au re-deposition an island with a larger dimension should be used or, we can pattern the island prior to the n-type metal deposition using the existing contact mask.

4.3.3.6 DVS-BCB planarization and p-type metal deposition

After the island definition, a $4\,\mu m$ thick DVS-BCB layer is spin-coated to planarize the devices, followed by a DVS-BCB full cure procedure using an Unitemp oven. After that the DVS-BCB layer together with the SiN layer is thinned down to the p-InGaAs layer by a two step RIE dry etching using a gas mixture of SF_6:O_2 (5 sccm:50 sccm) and CF_4:SF_6:H_2 (80 sccm:3 sccm:7 sccm) for DVS-BCB and for SiN etching, respectively. Then an image reversal lithography using Ti 35 photoresist is performed to define the p-type metal contact and a metal layer stack of 40 nm/200 nm Ti/Au is deposited through a lift-off process. Fig. 4.14 shows two devices with p-type metal contact.

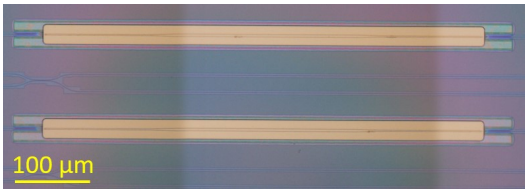


Figure 4.14: Microscope image of devices after p-type contact metal deposition.

4.3.3.7 Heater definition

To realize wavelength tuning, a set of micro-heaters have be to integrated with the laser cavity, including a pair of micro-heaters for the ring resonators, and a heater over a section of the Si waveguide in the laser cavity for phase tuning. The heaters consist of two levels. The first level is the resistor with high resistance, consisting of a 100 nm thick Ti layer and a 10 nm thick gold layer on top, which prevents Ti from oxidizing. A 40 nm thick Ti and a thick gold layer (e.g., 800 nm) are used in the second level for low resistance wiring and contact pads. To avoid optical attenuation, a thick spacer layer is desired to isolate the optical mode from the heater (Ti/Au). As a trade-off, it will reduce the tuning efficiency. Fig. 4.15 shows the simulated result of the optical loss with respect to the thickness of the DVS-BCB spacer layer. The simulation is performed using COMSOL and the optical absorption induced by the metal heater is deduced from the imaginary part of the complex effective index of the fundamental TE mode. As the fitting curve shows, the loss dramatically decreases with the increase of the DVS-BCB spacer layer from 200 nm to 400 nm and no obvious loss can be seen when the thickess of the spacer layer goes over 600 nm. So before heater deposition, the DVS-BCB planarization layer was thinned down to 600 nm by RIE dry etching. As the III-V taper structures are covered by the p-type metal layer, no mask is needed in this step. As the resistor is very thin, AZ 5214 photoresist is used in the image reversal contact lithography. After which a 30 seconds RIE O_2 plasma is performed to remove residual photoresist in the opened area. Then the resistor layer (100 nm/10 nm Ti/Au) is deposited using a Leybold Univex sputtering system, followed by a lift-off process. The contact metal (40 nm/500 nm Ti/Au) is deposited in the same way. Fig. 4.16(a) and Fig. 4.16(b) show a microscope image and an FIB cross-section of a ring resonator with Ti/Au micro-heater/metal contact layer, respectively.

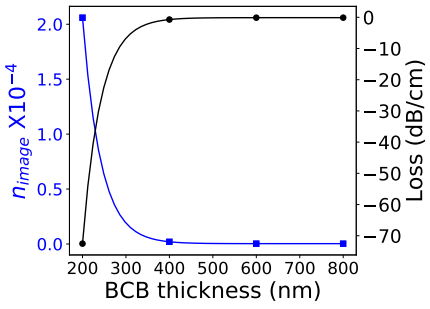
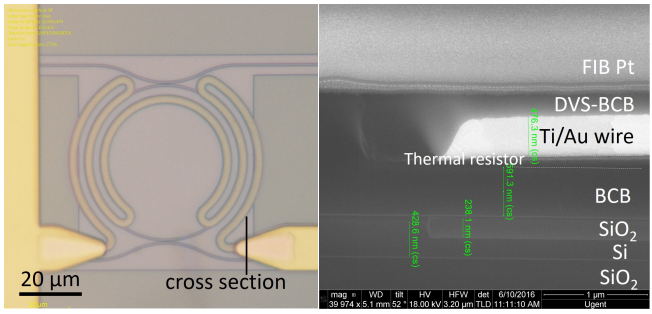


Figure 4.15: Simulated imaginary part of the refractive index n_{image} and metal absorption as a function of the thickness of the DVS-BCB spacer layer.



(a) (b)

Figure 4.16: (a) Microscope image and (b) SEM cross-section image of the ring resonator with an integrated Ti/Au micro-heater.

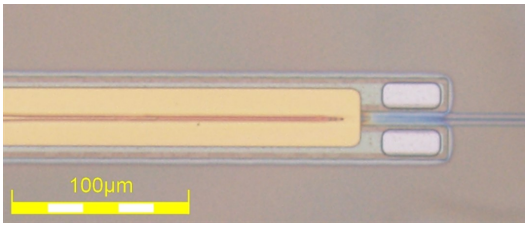


Figure 4.17: Microscope image of a device after N-via opening.

4.3.3.8 N-via opening and final metallization

After the micro-heater deposition, the devices are again planarized using DVS-BCB. The n-vias are opened by an image reversal lithography using Ti 35 photoresist, followed by RIE dry etching. The contact pads of the heaters are also exposed at the same time. Fig. 4.17 shows a device after the n-via opening. After the resist removal and a short RIE oxygen plasma cleaning, the fabrication is completed by a thick Ti/Au deposition to wire the micro-heater contacts and laser contacts to a bond pad array. Fig. 4.18 shows a microscope image of an array of fabricated devices. The III-V-on-Si gain section, micro-ring resonators, phase section, and output GCs (GC1 and GC2) are indicated. The DBR grating and the output directional coupler cannot be seen in this figure as they are covered with metal traces. As the Si waveguides are difficult to discern from the microscope image, black traces are overlaid for one of the lasers.

4.3.4 Characterization of the ring resonator with micro-heater

In this section, micro-ring resonators with integrated heaters will be discussed. A Keysight 8164B Lightwave Measurement System which consists of a tunable

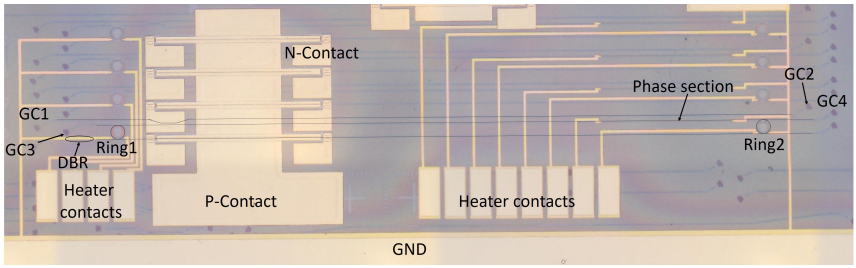


Figure 4.18: Top-view microscope image of an array of fabricated devices.

laser module and a power meter module was used to check the transmission of the devices, with 1 pm wavelength sweeping step. Fig. 4.19 shows measured spectra of a $25\,\mu m$ radius device with integrated heater. Here, the loaded Q-factor of the micro-ring is found to be $\sim$17000 with an extinction ratio around 20 dB over the entire C and L band. The drop port loss is found to be around 1dB, by comparing the maximal transmission from the drop port and the through port.

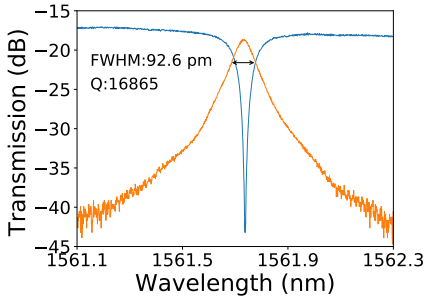
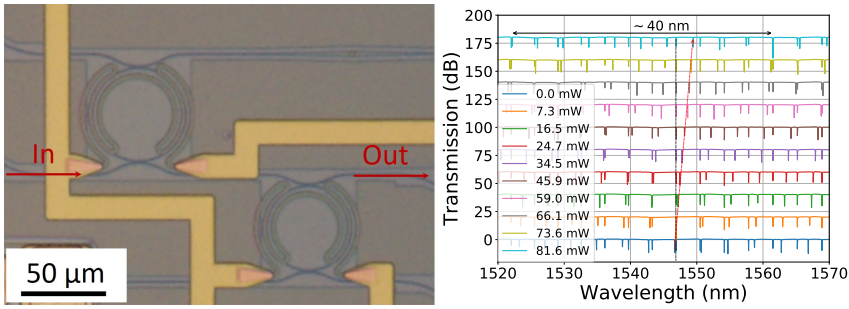


Figure 4.19: Representative drop port and through port transmission spectrum of the ring resonator structure.

4.3.5 Characterization of the Vernier filter

Fig. 4.20(a) shows a microscope image of a tunable Vernier filter (with integrated micro-heaters), which consists of two ring resonators with a slightly different radius ($25\,\mu m$ and $27.5\,\mu m$). Fig. 4.20(b) shows the transmission spectra and tuning behavior of this Vernier filter. The FSR of the $25\,\mu m$ and $27.5\,\mu m$ radius device is around 500 GHz and 450 GHz, respectively, which result in a combined FSR of 40 nm for the Vernier filter. The series resistance of the integrated heaters is found to be $5\,k\Omega$, which is expected to be $1\,k\Omega$ from our experiences. Such a high resistance is mainly caused by thinner deposited Au top layer. To check the maximum wave-



(a) (b)

Figure 4.20: (a) Microscope image of two cascaded ring resonators with a 25 µm and 27.5 µm radius, respectively. (b) Measured transmission spectra of the Vernier filter as a function of the dissipated power in one of the micro-heaters.

length tuning range, the applied current was increased till the micro-heater failed. A wavelength tuning of 2.8 nm (75 % of FSR) was achieved for the 27.5 µm radius device when the heater failed with 80 mW dissipated power. Before failure, a continuous and rapid increase in the detected voltage was observed when the applied power was over 50 mW, which indicates a degradation of the heater. Therefore, the maximal dissipated power has to be limited to 50 mW in the laser characterization to prevent heaters from being damaged. Fortunately, by combing the tuning range of these two rings, a discrete tuning over a full FSR of the Vernier filter can be realized. The suspected reason for failure is that the thermal expansion of Ti and DVS-BCB is different, which will induce a thermal stress across the interface of Ti and DVS-BCB when temperature goes up. Together with a poor adhesion of Ti to DVS-BCB, at some point Ti detaches from the DVS-BCB and forms a defect with a high local resistance. The thermal power density at the defect point will be higher. As a vicious circle, the local resistance increases because of the deformation of the heater, which eventually leads to the failure of the heater. To address this issue a dielectric material rather than DVS-BCB will be used for the spacer layer in later iterations.

4.3.6 Laser performance

4.3.6.1 Measurement setup

The measurement setup is schematically presented in Fig. 4.21. Three Keithley 2401 current sources are used to apply the electrical power to the micro-heaters. They were set to be voltage sources with a current compliance so that the current drops when the resistance of the heater increases, which prevents the heaters

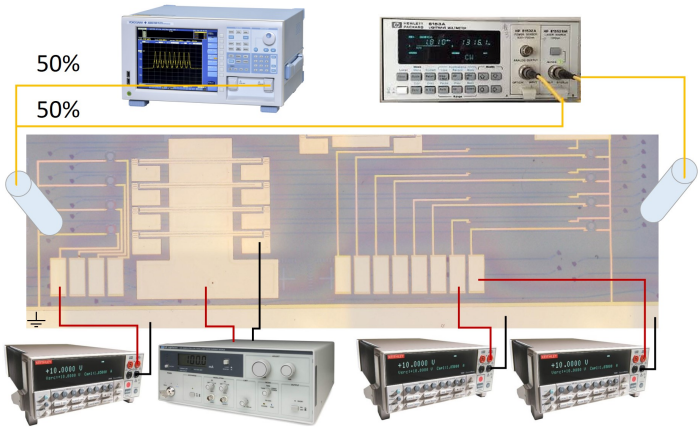


Figure 4.21: Schematic of the tunable laser measurement setup.

from being damaged. To reduce the laser phase noise and to ensure an accurate linewidth measurement, a Newport LDX-3620B battery current source is used to bias the III-V gain section. All the bias currents are applied to the on-chip device through a set of DC probes. The optical power is collected using single-mode fibers (SM-28) through fiber GCs. The left fiber probe (CCW output) is connected to a 3 dB splitter with one branch linking to an optical spectrum analyzer (SOA, YOKOGAWA AQ6375) to record the optical spectrum and the other branch connecting to a optical power meter (HP 8163A). while the right side fiber probe (CW output) is directly coupled to the other power meter (HP 8163A).

4.3.6.2 Series resistance of the gain section

The characterization of the tunable laser was carried out on a temperature-controlled stage which was stablized at $20\,^{\circ}\mathrm{C}$. Firstly the series resistance of the gain section was measured by sweeping the bias current. Fig. 4.22 shows the measured IV curve and the calculated differential resistance from that. The resistance is found to be comparable with other III-V-on-Si devices fabricated in our cleanroom.

4.3.6.3 Tuning behavior

Two lasers, one with DBR reflector and the other one without, are measured as a comparison. The differential resistances of these two devices and their threshold and the maximum output power are at the same level. The output power of the laser with DBR reflector (external feedback) is found to be more stable due the suppression of the competition between the CW and CCW lasing mode.

The micro-heaters on the ring resonators have a series resistance of $5\,\mathrm{k}\Omega$, while that on the phase section has a series resistance of $7\,\mathrm{k}\Omega$. The power dissipation in

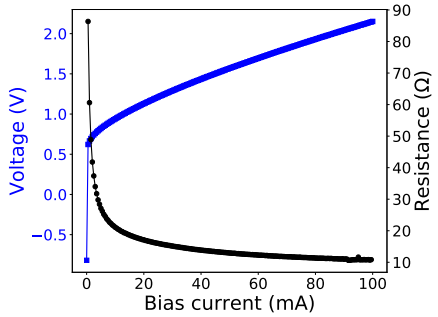
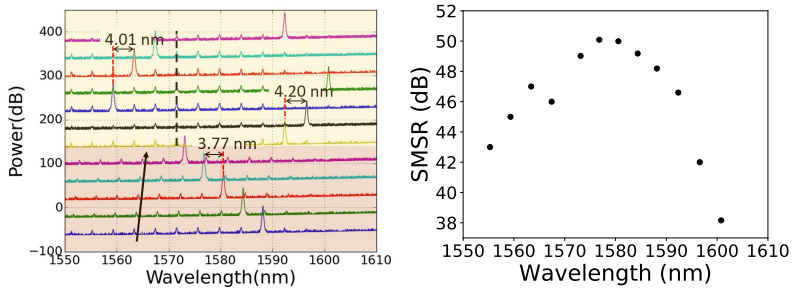


Figure 4.22: Measured V-I curve and differential resistance of a fabricated device.

the micro-heaters depends on the wavelength the laser is tuned to, but is below 50 mW per micro-heater. Because of the high resistance of the heaters, a high voltage, e.g., up to 20 V for the phase adjustment, is required in the measurement.

Limited by the tuning range allowed by the integrated micro-heaters, part of the wavelength range of interest can be discretely covered by tuning one micro-ring together with a fine adjustment of the phase section. By tuning the other micro-ring, the rest of the combined FSR of the Vernier filter can be covered, as shown in Fig. 4.23(a). The spectra in the yellow region and the pink region show a tuning step above 4 nm over the tuning range and of 3.77 nm at 1580 nm, respectively. Which correspond to the tuning of the $27.5\,\mu\mathrm{m}$ ring and the $25\,\mu\mathrm{m}$ ring. These lasing lines fill the entire 40 nm combined FSR of the Vernier filter. The measured side mode suppression ratio (SMSR) for the laser with DBR reflector is above 40 dB over the entire tuning range except for the last data point at a wavelength of 1600 nm, where it is 38 dB, as shown in Fig. 4.23(b). Fig. 4.24(a) shows a superposition of the representative laser spectra with and without DBR around 1590 nm, where the power is normalized to 0 dB and the high noise level at the longer wavelength results from the calibration of the insertion loss of the GC. As can be seen, the DBR does not have much influence on the side mode suppression but it induces a set of periodical peaks (micro-ring resonance wavelengths), which indicates that the stopband of the DBR covers the entire wavelength range of the interest. Fig. 4.24(b) and Fig. 4.24(c) show the superimposed laser spectra of the CCW modes of the laser with and without DBR reflector. The output power indicated in the graph is the output power in the silicon waveguide connected to GC GC1, so generated by the counter-clockwise propagating mode. The spectra are all recorded under the optimized condition with the highest output power. As shown in Fig. 4.24(b), the output power of the laser with external feedback varies between 1.5 and 3.3 mW over the tuning range. This smooth behavior of the output power versus wavelength is attributed to the unidirectional operation of the laser.



(a) (b)

Figure 4.23: (a)Tuning behavior of the laser with external DBR reflector, (b) Side mode suppression ratio as a function of laser emission wavelength.

On the other device without the DBR reflector, much larger power fluctuations were observed ($>$ 5dB) due to the competition between the CW and CCW mode, as seen in Fig. 4.24(c).

4.3.6.4 Unidirectional operation

The unidirectional behavior of the device is studied by simultaneously mapping the output power from GC1 and GC2. Fig. 4.25 shows the output power of the CCW and CW mode as a function of wavelength, at a laser bias current of 100 mA. The exact ratio of the CCW mode to CW mode depends on the wavelength setting but is in the range of 10 dB. This is very different from the behavior we observed from devices without an integrated DBR, where depending on the wavelength setting, either the CW or CCW mode can be dominant due to the strong mode completion. The behavior of the device as a function of the gain section bias current was also assessed. For this, the micro-heaters were driven to select a certain emission wavelength at a laser bias of 100 mA. Afterward, the micro-heater settings were fixed, and the gain section current was swept between 0 and 100 mA. In Fig. 4.26, the power in the CW and CCW mode is plotted as a function of gain section bias current at four wavelengths across the laser tuning range. As can be seen, for particular wavelengths, the device behaves unidirectional from threshold up to the 100 mA bias current. At particular wavelengths, bi-directional operation in the power versus current trace can be observed over a limited current range. This behavior is due to the fact that the longitudinal mode aligns with the resonance of the ring resonator in these current ranges. Given the high extinction ratio of the ring resonators and the high coupling ratio of the output directional coupler ($\sim$50 %), this makes the reflection from the two GCs (measured to be about -30 dB from optical frequency domain reflectometry (OFDR) in the wavelength range

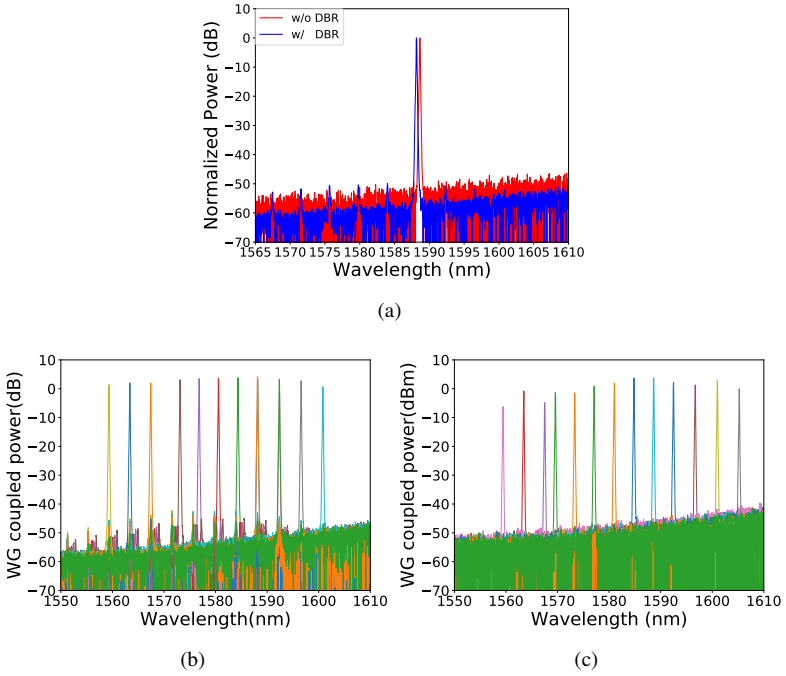


Figure 4.24: (a) Representative overlaid output spectra of the tunable laser with external DBR reflector and without external DBR reflector and, superimposed output spectra of the tunable laser (a) with external DBR reflector and (b) without external DBR reflector.

of interest) dominant, causing mutual coupling between the CW and CCW mode. The reflectivity at the 500 nm wide III-V taper tip is simulated to be below -40 dB. The strong variation in the output power is attributed to mode hops in the laser emission during bias current tuning.

4.3.6.5 Laser linewidth

The linewidth of the laser was evaluated over its tuning range. This measurement was realized using a delayed self-heterodyne system, using a 200 MHz acoustic-optic frequency shifter in one arm of the interferometer and a 5 km long fiber delay line in the other arm to kill the coherence. Moreover, a polarization controller is added together with the fiber coil to optimize the interference strength at the output port. The measurement setup is schematically depicted in Fig. 4.27. Note that the external reflection could significantly impact the linewidth of the laser, and the measured beating frequency spectrum is also sensitive to the reflection in the fiber interferometer [38]. Therefore two cascaded in-line optical isolators (ISOs) are

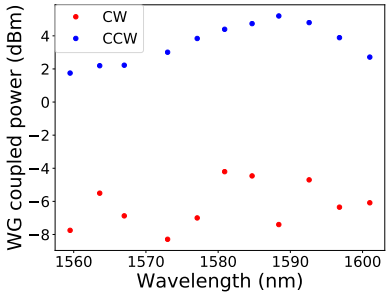


Figure 4.25: Output power of the CCW and CW mode as a function of laser wavelength at 100 mA bias current.

connected to the fiber probe to prevent back-reflection and, the fiber connectors are carefully cleaned to reduce the potential reflection at the interface. A 99/1 splitter is used with the $1\,\%$ branch connected to the delayed self-heterodyne system. The $99\,\%$ branch is split again by a 3 dB splitter and then connected to an SOA and an optical power meter, respectively. The optical beating signal is converted to an electrical signal via a commercial optical receiver and is then fed to an N9010A EXA Signal Analyzer to analyze the beat note. Usually, the optical linewidth can be extracted by implementing Lorentzian fitting to the raw data, and the half of the full width at half maximum (FWHM) of the fitting curve is took for the laser linewidth. The result as a function of laser wavelength is shown in Fig. 4.28. The laser linewidth is consistently below 1 MHz and reaches 550 kHz in the optimal operation point.

4.4 Pre-fabrication of SOA arrays for micro-transfer-printing

4.4.1 III-V epitaxial layer stack

Compared to the III-V epitaxial material used for the transfer printed DFB laser fabrication, as presented in the second chapter, some minor modifications were made to the III-V wafer used in this fabrication, including an additional 25 nm thick InGaAsP layer with a band gap of $1.17\,\mu\mathrm{m}$ on top of the AlGaAsIn active region to prevent the active layers from oxidizing, and a release layer consisting of a 500 nm thick AlInAs layer and a 50 nm thick InGaAs layer. The overall thickness of the p-type InP layer is $2\,\mu\mathrm{m}$ due to an unexpected imperfect control of the p-InP growth. This III-V epitaxial material is provided Tyndall.

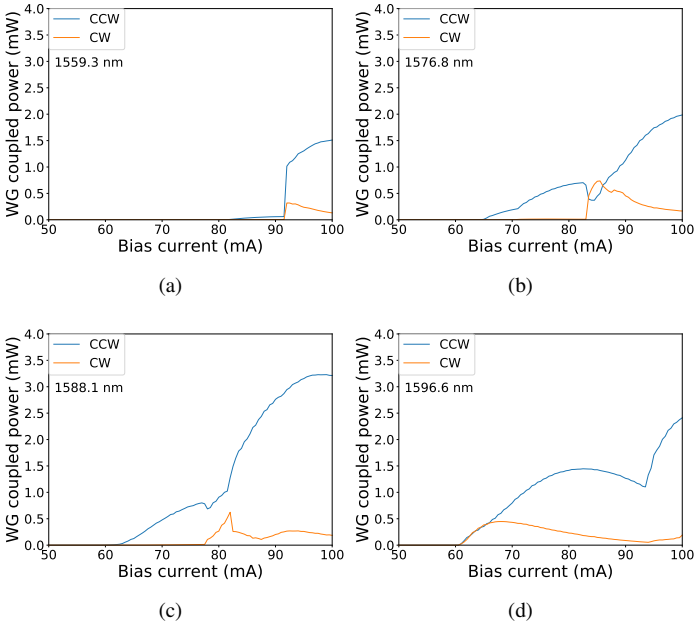


Figure 4.26: Waveguide-coupled output power in the CW and CCW direction as a function of gain section bias current for different output wavelengths of the laser.

4.4.2 An alignment-tolerant III-V/Si SOA design

The linear III-V/Si taper structures that have been widely used in evanescently coupled III-V-on-Si devices realized through die-to-wafer bonding require a stringent alignment accuracy (typically less than 300 nm) [39]. That is also the reason an intermediate route–transfer printing of III-V material coupons–rather than pre-fabricated SOAs was adopted to realize DFB lasers in the second chapter. To further exploit the μTP technology to integrate pre-fabricated III-V devices, an adiabatic coupling scheme that can tolerate $1\,\mu\mathrm{m}$ lateral misalignment is desired.

Fig. 4.29 schematically illustrates the alignment-tolerant III-V-on-Si taper structure. The hybrid waveguide section consists of a $4.5\,\mu\mathrm{m}$ wide III-V waveguide and an underlying $2.5\,\mu\mathrm{m}$ wide Si waveguide with a thin DVS-BCB bonding layer. The use of such wide Si waveguide results in a strong confinement of the mode in the Si. In this way, the disturbance to the guided optical mode induced by any misalignment of the III-V taper structure is significantly reduced, at the expense of a reduced confinement in the III-V active region. Fig. 4.30(a) shows the intensity profile of the fundamental TE mode in this hybrid waveguide. The optical confinement factor in the quantum wells increases from $3\,\%$ to $6\,\%$ with an increase

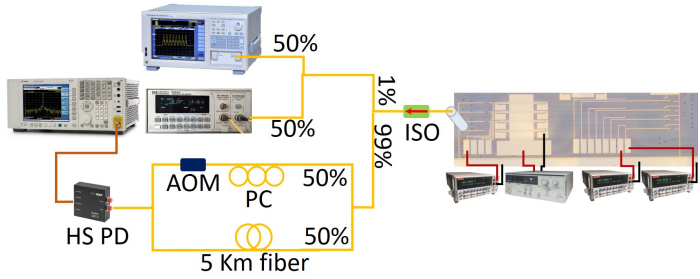


Figure 4.27: Schematic of the delayed self-heterodyne system for laser linewidth measurement.

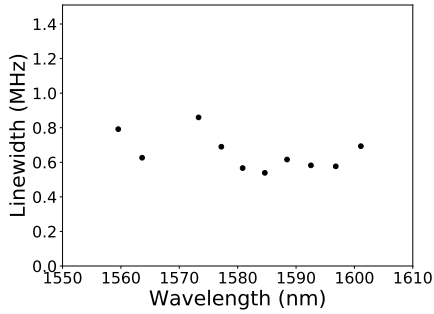
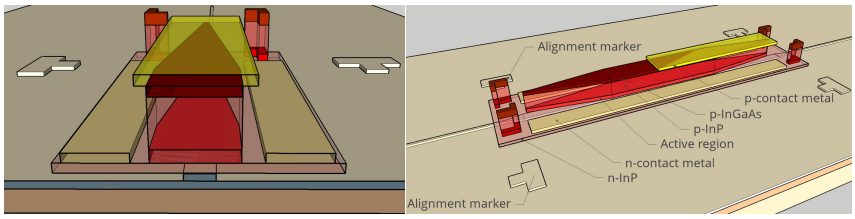


Figure 4.28: Laser linewidth as a function of emission wavelength as measured using a delayed self-heterodyne measurement scheme.

of the thickness of the DVS-BCB bonding layer from 20 nm to 60 nm, as shown in Fig. 4.30(b).

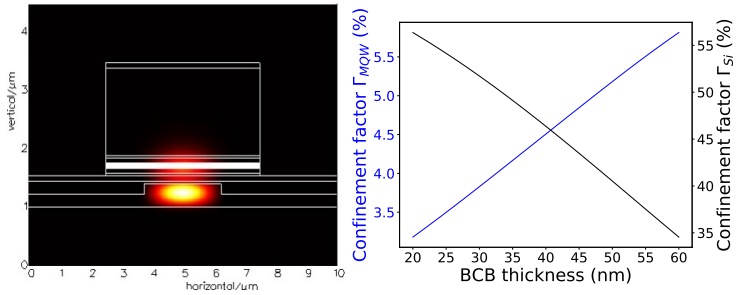
A linear III-V taper structure is designed to push the mode into the underlying Si waveguide, which is then narrowed down and connected to a 650 nm wide single TE mode waveguide. The structure also shows potential for high saturation power semiconductor optical amplifiers (SOA) due to the reduced confinement in the active region. Fig. 4.31 shows the optical mode conversion through the taper structure, where the lateral misalignment is set to be $1\,\mu\mathrm{m}$. The III-V taper tip is 400 nm, the III-V taper structure is $180\,\mu\mathrm{m}$ long, and the DVS-BCB bonding layer is 20 nm. As can be seen, the hybrid mode gradually converts to the fundamental mode in the Si waveguide and eventually resides in the 650 nm wide rib waveguide.

The influence of the lateral misalignment, the thickness of the DVS-BCB bonding layer, and the width of the III-V taper tip on the coupling efficiency are studied. Fig. 4.32(a) and Fig. 4.32(b) show the coupling efficiency as a function of the length of the III-V taper structure for different DVS-BCB thickness. When the III-V taper is perfectly aligned to the underlying Si waveguide, the transmission



(a) (b)

Figure 4.29: Schematic layout of the adiabatic taper structure with an alignment-tolerance of 1 µm.



(a) (b)

Figure 4.30: (a) Fundamental TE mode profile,(b) Confinement factor of the fundamental mode in Si and in III-V, respectively.

rapidly increases with the increase of the taper length and saturates at 98 %, while with 1 µm lateral misalignment, a 180 µm long taper is needed to reach the maximal transmission for a hybrid waveguide with less than 40 nm DVS-BCB bonding layer. Fig. 4.32(c) shows the influence of the III-V taper tip width on the coupling efficiency with a given taper length of 180 µm. As can be seen even an 800 nm wide taper allows for 95% coupling, which will significantly ease the mesa definition through the contact lithography. Based on the above discussion, a 180 µm long III-V taper will be used in the SOA design and the width of the taper tip will be less than 800 nm.

4.4.3 A general overview of the process flow

Fig. 4.33 describes the process flow of the fabrication of III-V taper structures on the native InP substrate. Firstly, the InP sacrificial layer is removed, and a SiN layer is deposited as a hard mask to pattern the InP mesa through a combination of ICP dry etching and wet etching using 1:1 HCl:H_2O (Fig. 4.33(a)-(e)). Again a

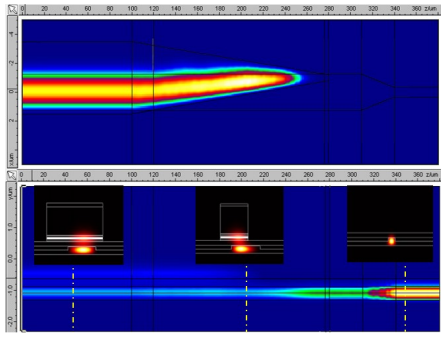


Figure 4.31: Mode propagation through the taper structure with 20 nm thick DVS-BCB bonding layer.

thin SiN layer is deposited and is then etched back as a hard mask to define the active region (Fig. 4.33(f)). The n-InP island is patterned with a photoresist soft mask (Fig. 4.33(g)). A typical n-type contact metal layer stack (30 nm/20 nm/50 nm Ni/Ge/Au) with an extra Ti/Au layer stack (40 nm/100 nm) is deposited on the n-InP layer, closed to the mesa at both sides through a lift-off process (Fig. 4.33(h)). Then a thin layer of room temperature SiN is deposited (Fig. 4.33(i)) to passivate the sidewalls of the AlGaAsIn active region immediately after a two-step native oxide removal procedure (a short dip in BHF and then in pirahna). After the SiN passivation, the devices are planarized with a DVS-BCB layer(Fig. 4.33(j)), which is then etched back (together with the SiN) to expose the InGaAs contact layer for the following p-type metal (Ti/Au) deposition (Fig. 4.33(k)).

The first $40\,\mu\mathrm{m}$ wide coupon mesa is patterned by etching through the DVS-BCB layer with a photoresist soft mask, as shown in Fig. 4.33(l). Using a photoresist mask and wet etching the AlInAs release layer is selectively etched and stops on the InP substrate, after which a few cycles of ICP etching are performed to etch 300 nm into the InP substrate (Fig. 4.33(m)). Then the coupons are encapsulated by a $2.5\,\mu\mathrm{m}$ thick photoresist (Ti 35) layer which is patterned in such a way that the device coupon is protected, the release layer is locally exposed, while also tethers are defined (Fig. 4.33(m)). The coupon is undercut by immersing in a low temperature (below $10\,^{\circ}\mathrm{C}$) aqueous $FeCl_3$ solution (Fig. 4.33(o) and (p)).

4.4.4 Pre-fabrication of SOA arrays on the InP substrate

4.4.4.1 SOA mesa definition

A $1.5 \times 1.5\,\mathrm{cm}^2$ III-V die is used in this fabrication. In order to enable the automatic alignment of the pre-fabricated SOA onto the Si PIC using the patterning recognition function, a pair of 'L' shape alignment makers are patterned at the ends of the coupons, as shown in Fig. 4.34(a). Same as we did in the DFB laser fabri-

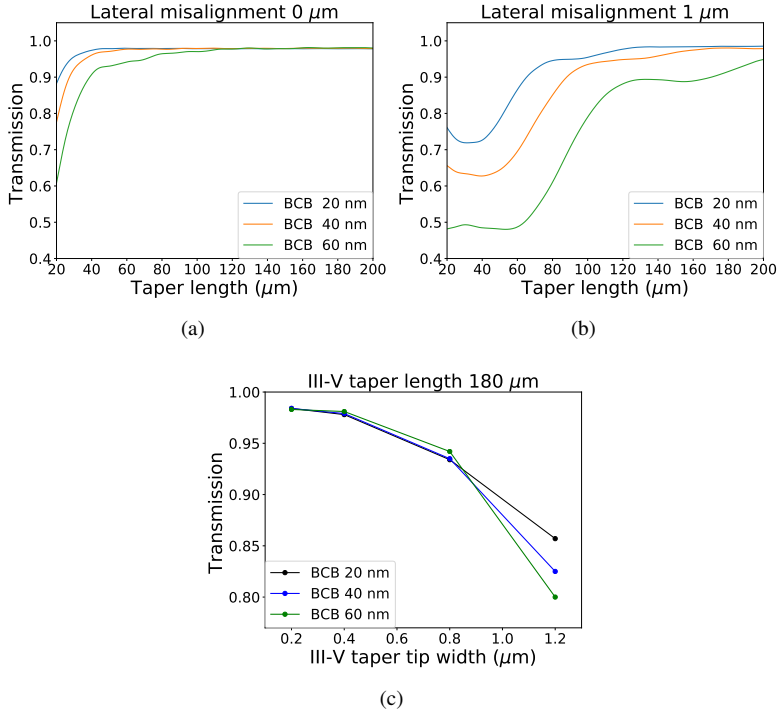


Figure 4.32: Simulated coupling efficiency as a function taper length for the taper structure with a lateral misalignment of (a) 0 µm and (b)1 µm.(c) Coupling efficiency as a function of III-V taper tip width.

cation, an ICP dry etching is first performed to etch the p-InGaAs layer and most of the p-InP layer, followed by a short wet etching in 1:1 HCl:H_2O. Benefiting from a shorter HCl wet etching the undercut of the p-InP in the taper section is controlled within 10 µm. After the p-InP mesa definition, a 200 nm thick 270 °C MF SiN is deposited and is then etched in an RIE tool. In this way the shape of the p-InP mesa is transferred to the SiN layer, which then acts as a hard mask for the following QW definition. Then four cycles of ICP dry etching are performed to etch through the 25 nm InGaAsP layer and into the AlGaAsIn active layers. The rest of the active layers is etched using 1:1:20 H_3PO_4:H_2O_2: H_2O. As a FIB cross-section image shows in Fig. 4.34(c), the width of the p-InGaAs is around 800 nm, which indicates a good vacuum contact in the optical lithography. The p-InP mesa shows a 'V' shape cross-section with 400 nm wide bottom, which together with a 600 nm wide (at the bottom) QWs taper tip ensures an efficient mode conversion between III-V layer and the underlying Si waveguide.

As the height of the SOA mesa is about 3 µm, a 7 µm thick photoresist layer

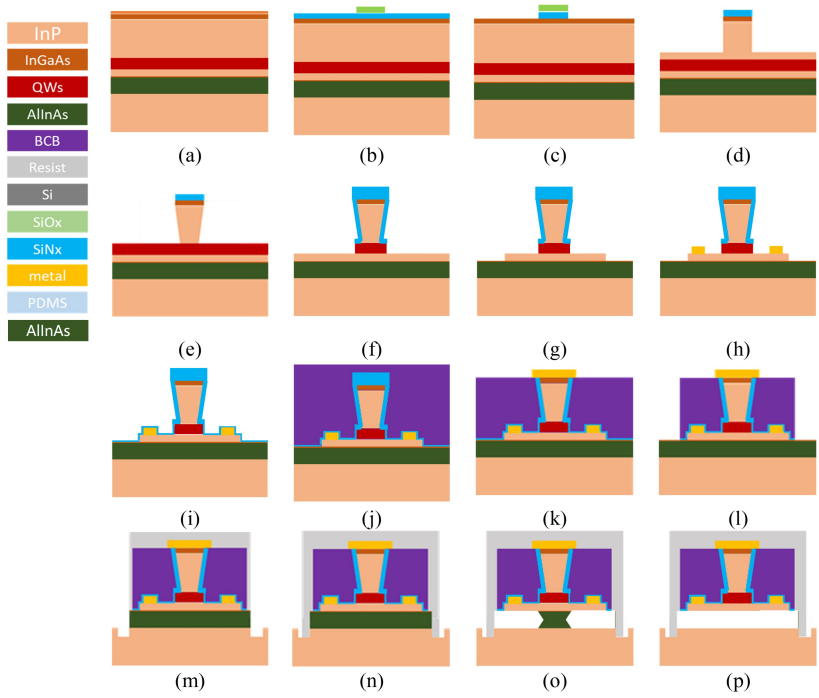
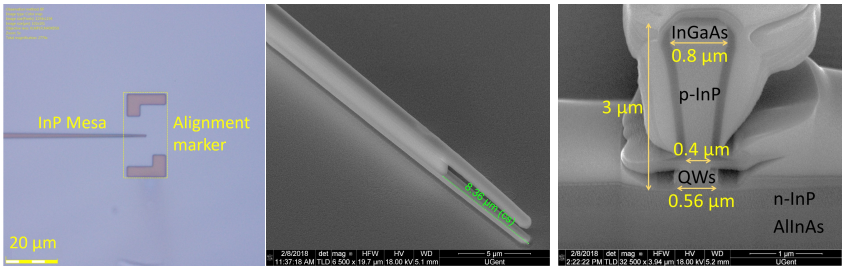


Figure 4.33: Process flow for the definition of III-V taper structure on the native InP substrate.

(AZ 9260) is used to define the shape of the n-InP island via an optical lithography procedure, after which the sample is immersed in a 1:1 HCl:H_2O solution to etch down the n-InP layer. After the n-InP patterning, a deep lateral undercut is observed, as a shown in Fig. 4.35. To avoid a further undercut and thus a high resistance or even open circuit, the wet etch is stopped with some residual n-InP left on the AlInAs release layer.

Following the standard process flow a n-type metal layer stack (30 nm/20 nm/50 nm/40 nm/100 nm Ni/Ge/Au/Ti/Au) is deposited through a lift-off process. Fig. 4.36 shows a microscope image of an array of SOAs with n-type metal contacts. Then a series of fabrication steps, including SiN passivation, DVS-BCB planarization, and p-type metal contact (40 nm/150 nm Ti/Au) deposition are performed.



(a) (b) (c)

Figure 4.34: Definition of the III-V taper structure. (a) Microscope image of the taper tip with the 'L' shape alignment markers, (b) SEM image of the III-V taper tip, showing a $8.3\,\mu m$ undercut of n-InP, (c) FIB image of the III-V waveguide cross section, revealing a 'V' shape p-InP mesa and a 560 nm wide active region.

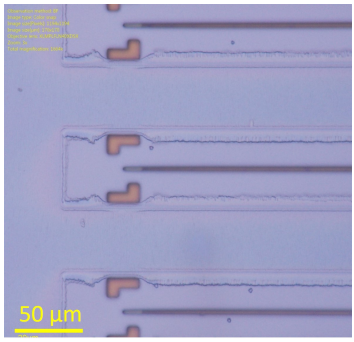


Figure 4.35: Microscope image of the device after wet etching of n-InP, showing a deep undercut.

4.4.4.2 Coupon mesa definition

The coupon mesa is $2.5\,\mu m$ wider in each direction compared to the n-InP island and with four rectangular notches at the sides to leave the n-type metal exposed. The coupon mesa is defined using a $3.5\,\mu m$ thick photoresist (Ti 35) soft mask and RIE dry etching. Fig. 4.37 shows a microscope image of an array of devices after this procedure.

4.4.4.3 Via etching

Ti 35E photoresist is used as a positive photoresist in the optical lithography to open the coupon vias, after which a short RIE oxygen plasma cleaning is performed to remove the potentially remaining photoresist in the via. Then the sample

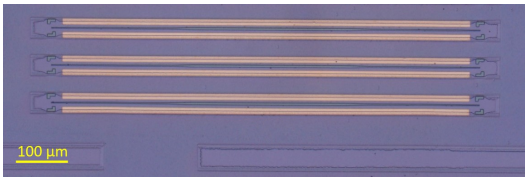


Figure 4.36: Microscope image of an array of devices with n-type metal contact.

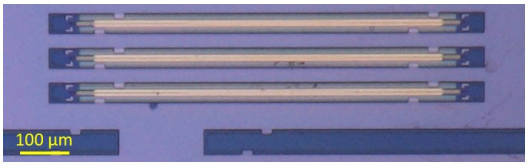


Figure 4.37: Microscope image of an array of devices with photoresist soft masks for the first coupon mesa patterning.

is baked at 120 °C for 3 minutes. As already mentioned, there was some residual n-InP left above the AlInAs release layer, so four cycles of ICP dry etching are first performed to expose the release layer. Then the sample is immersed in a room temperature 1:1:20 H_3PO_4:H_2O_2:H_2O piranha solution for 150 seconds to etch through the AlInAs layer at an etch rate of $\sim$ 250 nm/min, With the existing photoresist mask four cycles of ICP dry etching is again performed to etch around 300 nm into the InP substrate. The resulting coupons with the remaining photoresist mask are shown in Fig. 4.38.

4.4.4.4 Encapsulation and tether definition

As the p-InP layer is thicker ($2\,\mu m$) than the III-V coupon ($1.5\,\mu m$) used for the DFB laser demonstration which was presented in the third chapter, a thicker photoresist layer is needed to protect the sidewall of the coupon. Therefore the spin coating rate is reduced to 2500 rpm to have a thicker resist layer, while the remaining fabrication steps follow the standard process flow. Fig. 4.39 shows a microscope image of coupons with two different tether designs. The one without tethers is a test structure which is used to indicate the progress of the release.

4.4.4.5 Release of the pre-fabricated SOAs

The release etch is performed in a 3 °C aqueous $FeCl_3$ etchant. When the test coupons flow away, it means the release is complete. As shown in Fig. 4.40, the pattern with surrounding rectangular teeth on top of these devices used to be covered by a test coupon. As the etch rate of AlInAs in aqueous $FeCl_3$ is much

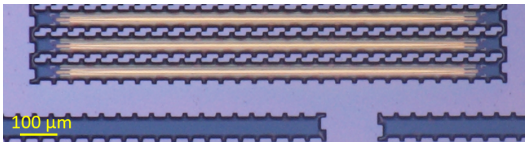


Figure 4.38: Etching through the release layer with a photoresist soft mask.

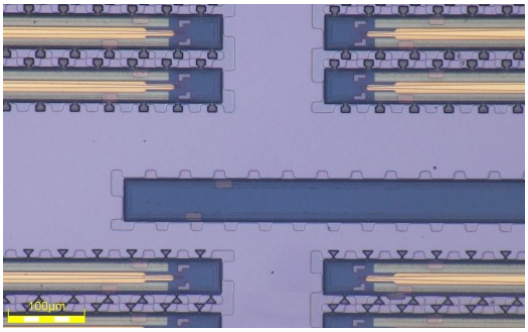


Figure 4.39: Microscope image of the coupons encapsulated with a layer of photoresist.

faster than that of InGaAs this release took only about 80 minutes. When the release is complete, the sample is carefully immersed in a water bath to get rid of the remaining $FeCl_3$ and is then very gently dried using a N_2 gun. The colorful rectangles surrounding the coupons are resulting from the aforementioned residual n-InP. After the release etch, a piece of scotch tape is used to pick up some coupons manually. Fig. 4.41(a) shows the area where the devices were picked up and, Fig. 4.41(b) shows the bottom side of the coupons attached on the tape. It reveals a clean surface on both the InP substrate and the bottom surface of the fabricated devices. Fig. 4.41(c) shows a microscope image of a coupon with one side attached on scotch tape and the other side free-hanging in the air. No obvious bending or deformation is observed on the release device.

4.5 Tunable laser realized by μTP of pre-fabricated SOAs

4.5.1 Tunable laser design

Fig. 4.42 shows the schematic layout of the laser cavity design. Opposite to the ring laser design explored in the previous section, here we focus on a linear cavity arrangement as it inherently does not suffer from the competition between two

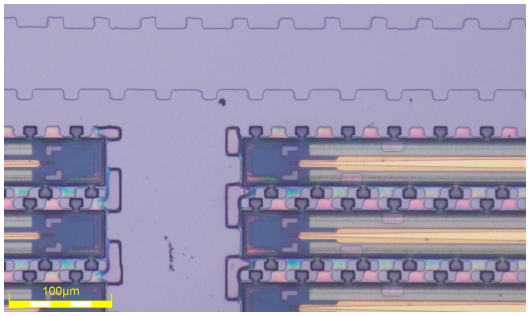
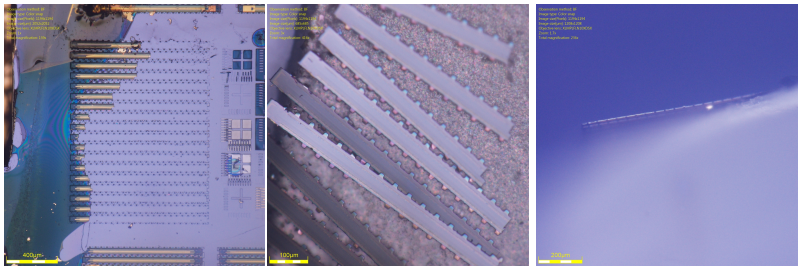


Figure 4.40: Microscope image of the released coupons.



(a) (b) (c)

Figure 4.41: The manually picking up test using a piece of scotch tape, (a) Surface of the InP substrate after picking an array of coupons, (b) Bottom surface of the coupons, (d) A free hanging coupon, showing no obvious deformation.

counter propagation modes and it is the most widely used tunable laser geometry. It is realized on imec's 400 nm platform using 193 nm deep UV lithography and a 180 nm dry etch into the 400 nm Si device layer. The laser design has a $\sim$ 3 mm long cavity and consists of a loop mirror with a pair of ring resonators incorporated inside a closed MMI loop, a balanced MZI based tunable reflector and a $2\,\mu\mathrm{m}$ wide waveguide between the mirrors to facilitate the µTP-based integration of the III-V/Si gain section. As discussed above, the use of a wide Si waveguide relaxes the alignment requirements at the expense of a reduced confinement of the optical mode in the gain region. The micro-rings have a radius of $25\,\mu\mathrm{m}$ and $27.5\,\mu\mathrm{m}$, respectively, leading to a combined Vernier FSR over 40 nm in the 1560 nm wavelength range, as already discussed in the previous tunable laser demonstration through bonding. In this design, the gap between the bus waveguide and the ring resonator waveguide (both are 650 nm wide) is 400 nm, which results in a loaded Q-factor of 34.5×10^3 and a drop port loss of 1.3 dB. All the waveguides are terminated with so-called reflectionless GCs [40] to reduce the external refection

to the laser cavity, except that the output port of the tunable reflector is connected to a Si taper structure which can be used for interfacing with optical fiber. Micro-heaters (not shown in the schematic) are integrated post μTP on the ring resonators, the phase section and the tunable reflector for laser tuning purposes.

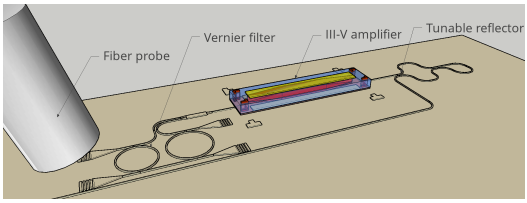


Figure 4.42: Schematic of the tunable laser with an transfer printed pre-fabricated III-V taper structure.

4.5.2 Overview of the μTP of pre-fabricated SOAs and post-process flow

The process flow for the integration of III-V-on-Si lasers by μTP of pre-fabricated SOAs is described in Fig. 4.43. The integration process starts with a spin-coating of a 40 nm thick DVS-BCB layer on the Si photonic chip, followed by a 15 minutes soft-bake at $150\,^{\circ}\mathrm{C}$. Then the SOA structures are picked up and printed onto the target Si PICs through a semi-automatic printing procedure with help of the pattern recognition function (Fig. 4.43(b)). After transfer printing, the photoresist encapsulation layer is removed via a 45 minutes RIE oxygen plasma cleaning, after which the chip is baked at $270\,^{\circ}\mathrm{C}$ to fully cure the DVS-BCB bonding layer. A $1\,\mu\mathrm{m}$ SiO_2 layer is deposited as a spacer layer for the integration of heaters over the microrings and phase sections (Fig. 4.43(d)). The devices are then planarized using DVS-BCB with the p-contact metal exposed after the DVS-BCB etching back process (Fig. 4.43(e)). Then n-contact vias are opened by RIE dry etching (Fig. 4.43(f)), and the laser integration is finished by a thick Ti/Au metal contact deposition (Fig. 4.43(g)). In order to deposit heaters on the SiO_2 spacer layer, an RIE dry etch without mask is performed to remove the DVS-BCB planarization layer. Due to a high etch selectivity of DVS-BCB to SiO_2(7:1) this etch can be well controlled with slight over etch into the SiO_2 spacer layer (Fig. 4.43(h)). Then heaters with two-level metal layer stacks are deposited through standard lift-off processes (Fig. 4.43(i)).

4.5.3 μTP of the pre-fabricated SOA

A $2 \times 2\,\mathrm{cm}^2$ silicon photonic chip which is diced from a 200 mm wafer is used in this work. As discussed before the waveuide circuits are planarized using a

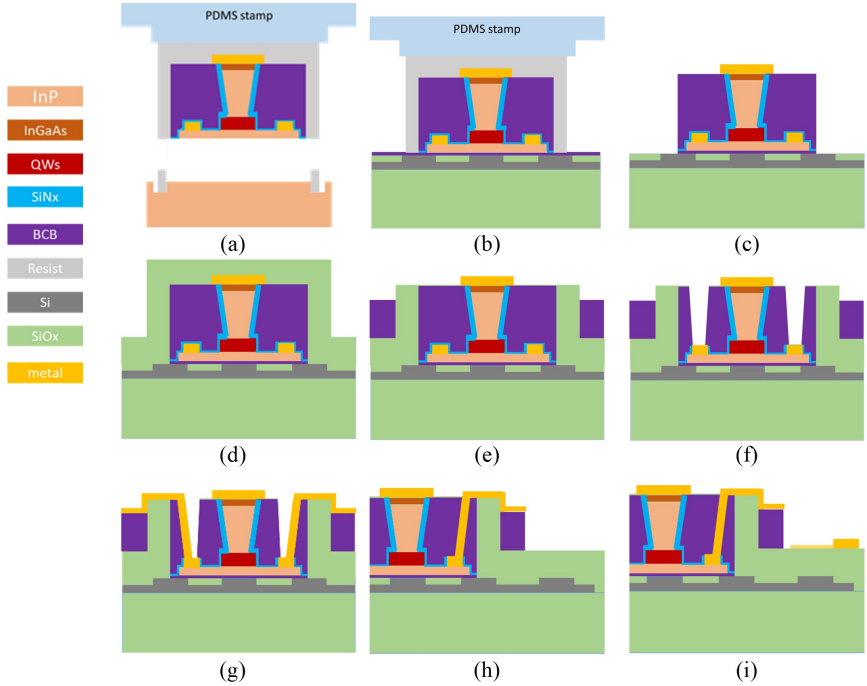
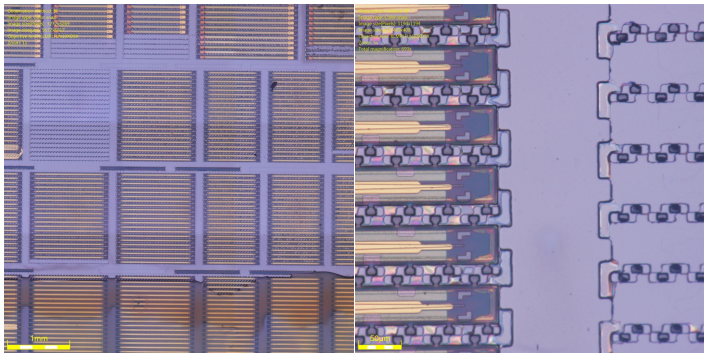


Figure 4.43: μTP of the pre-fabricated III-V SOA onto Si PIC and the post-process flow for the laser fabrication. (a) Picking up the pre-fabricated SOA from the native InP substrate, (b) Transfer printing the SOA coupon onto the co-designed Si PIC, (c) Resist removal, (d) SiO_2 spacer layer deposition, (e) DVS-BCB planarization and etching back to expose the p-type metal contact, (f) n-via opening, (g) Ti/Au metallization, (h) Etching down DVS-BCB to expose the SiO_2 spacer layer, (i) Micro-heater deposition.

SiO_2 chemical mechanical polishing process, whereas to avoid the Si device layer from being damaged, this CMP process is stopped $\sim$ 30 nm before reaching the Si device layer. According to the simulation, an ultra-thin DVS-BCB bonding layer (e.g. $<$40 nm) is required to realize an efficient mode coupling from the SOA to the Si waveguide and to have a relaxed alignment tolerance, therefore prior to the integration of SOAs, the sample is dipped into BHF to remove the excessive SiO_2 in the trench. In this demonstration, a 1:4 diluted DVS-BCB (CYCLOTENE 3022-35) solution is used as the adhesive bonding agent, which is spin-coated at 3000 rpm for 40 seconds, followed by a soft-bake at 150 °C for 10 minutes to let the solvent evaporate. Then the III-V source wafer and the silicon photonic chip are both loaded on the sample stages in the X-Celeprint μTP-100 tool. 1160 μm long SOAs (including a pair of 180 μm long taper structures and a 800 μm



(a) (b)

Figure 4.44: (a) Microscope image of the source chip after picking a group of SOAs, (b) Zoom-in image showing the design of the SOA coupon array.

straight SOA waveguide section) are used in the fabrication. A PDMS stamp with a $50 \times 1400\,\mu m^2$ post is used to pick up and print the pre-fabricated SOAs. Fig. 4.44(a) shows a microscope image of the III-V chip after an array of SOAs has been picked up. As shown in the zoom-in microscope image (Fig. 4.44(b)), the tethers broke at the weakest point, leaving their 'feet' still attached on the InP substrate.

The printing of the SOAs was carried out at room temperature. Fig. 4.45 shows a microscope image of the PICs with an array of transfer-printed SOAs. The bright rectangular region on the PIC indicates the area where the SOA is desired. The SOA at the bottom-right corner is a test printing to confirm the printing parameters, after which 17 SOAs were aligned and printed onto the target PICs, with 5 failed printings which are marked using the red rectangles. The green rectangles indicate the active regions which were skipped in the printing process, and the black rectangle highlights the device of interest. It was found in later test that $100\,\%$ yield can be achieved by heating the target Si photonic chip to $70\,°C$ in the printing process.

4.5.4 Post-processes

After the DVS-BCB bonding layer is fully cured, a $1\,\mu m$ thick SiO_2 layer is deposited over the PIC as a spacer layer. Then DVS-BCB (CYCLOTENE 3022-46) is spin-coated at 2000 rmp for 40 seconds, followed by a BCB full cure process. In the etch back, an RIE dry etch with a gas mixture of 5 sccm:50 sccm SF_6:O_2 is at first used to thin down the DVS-BCB layer. Once the etching stops on the SiO_2 layer (on the printed coupons), another recipe with a gas mixture of SF_6:CF_4:H_2

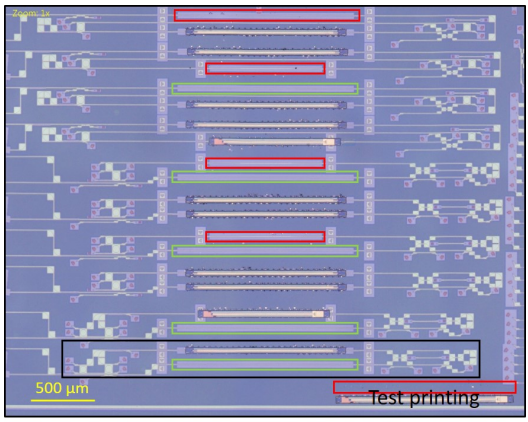


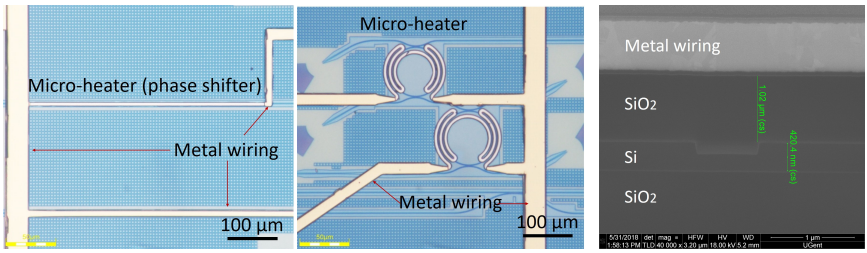
Figure 4.45: Top-view microscope image of a PIC with an array of transfer-printed coupons.

(80 sccm:3 sccm:7 sccm) is used to etch down the DVS-BCB layer and to expose the p-type metal contacts. With $3.5\,\mu m$ photoresist soft mask patterned via an image reversal contact lithography, the n-vias are opened by RIE dry etching. Then a laser contact metal layer is deposited through a standard lift-off process. Before depositing the micro-heaters, an RIE dry etch is again performed to expose the SiO_2 spacer layer. A gas mixture of 5 sccm :50 sccm SF_6:O_2 which provides selectivity of 4:1 (DVS-BCB: SiO_2) is used. To reduce the series resistance of the micro-heaters and to reduce the applied voltage, a thicker metal stack layer (120 nm/15 nm Ti/Au) is deposited for micro-heaters. Fig. 4.46(a) and Fig. 4.46(b) show a microscope image of a $200\,\mu m$ long phase section and a Vernier filter with integrated miro-heaters. Fig. 4.46(c) shows an SEM image of a FIB cross-section of a phase shifter, where a $1\,\mu m$ thick SiO_2 spacer layer between the Si waveguide and the deposited metal can be seen.

Fig. 4.47 shows the fabricated laser array. As seen all the ground (N-type contacts) of the devices is connected to a common probing pad, while most of the other metal contacts are routed to an array of contact pads at the sides of the device region for wire bonding in the future.

4.5.5 Characterization of the Vernier filter

A Santec 510 tunable laser and an HP power meter are used in the transmission measurement. A Keithley 2400 current source is used to bias the micro-heaters to investigate the tuning range of the Vernier filter. Fig. 4.48(a) shows an overlaid through port and drop port transmission spectrum. The loaded Q-factor is measured to be around 34500 (45 pm wide FWHM) due to the use of a 400 nm wide



(a) (b) (c)

Figure 4.46: PIC with integrated Ti/Au micro-heaters, (a) Phase tuning section, (b) Ring-resonators with integrated micro-heaters, (c) SEM cross-section image of the PIC after the micro-heater deposition, showing 1 µm thick SiO_2 spacer layer between micro-heater (together with metal wires) and Si device layer.

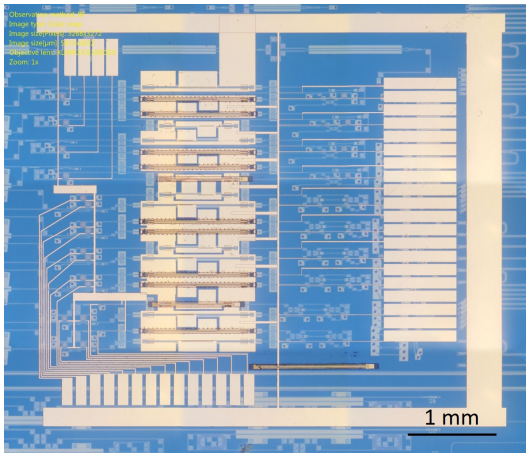
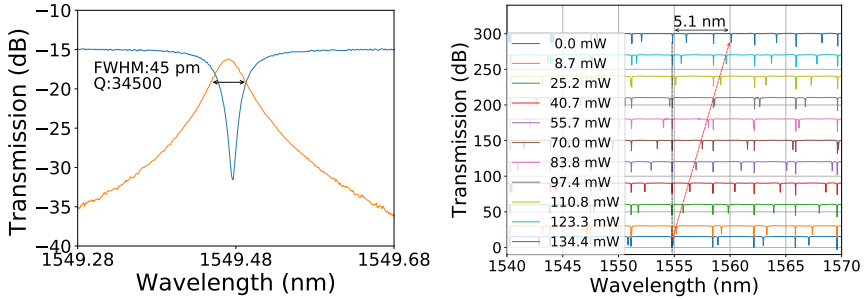


Figure 4.47: Microscope image of the fabricated III-V-on-Si laser structures.

coupling gap. The micro-heaters on the ring resonators have a series resistance of 500 Ω, while that on the phase section has a series resistance of 700 Ω.

Fig. 4.48(b) shows the recorded transmission spectra for different power dissipation in one of the micro-heaters. A wavelength tuning over a full FSR is achieved by dissipating 134.4 mW, allowing for a wavelength tuning over a full combined FSR of the Vernier filter. Apparently the quality of this micro-heater is much better than the previous one deposited on the DVS-BCB spacer layer.



(a) (b)

Figure 4.48: (a) Representative drop-port and through-port transmission spectrum of 25 µm ring resonator. (b) Measured transmission spectra of the Vernier filter as a function of the dissipated power in one of the micro-heaters, showing a tuning range over a full micro-ring FSR.

4.5.6 Laser performance

A typical tunable laser measurement setup, as shown in Fig. 4.21 is used to characterize the fabricated devices, with an extra current source and one more DC probe for adjusting the tunable reflector. The characterization was conducted at 20 °C. The output power is collected by a single-mode fiber from one output port of a ring resonator, as illustrated in Fig. 4.42. The same method was used in [13] as well. Fig. 4.49 shows a photograph of the setup where a set of DC probes were landed on the sample in the measurement.

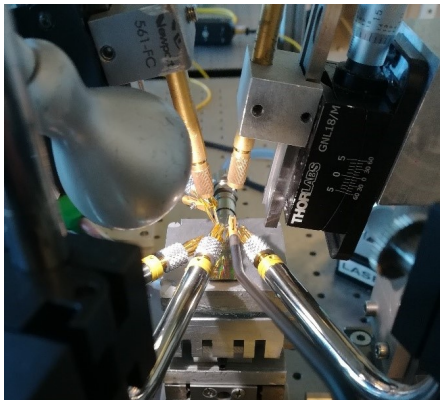


Figure 4.49: Photograph of the measurement setup with a set of DC probes landing on the PIC.

As the recorded IV curve shows in Fig. 4.50(a), the differential resistance of

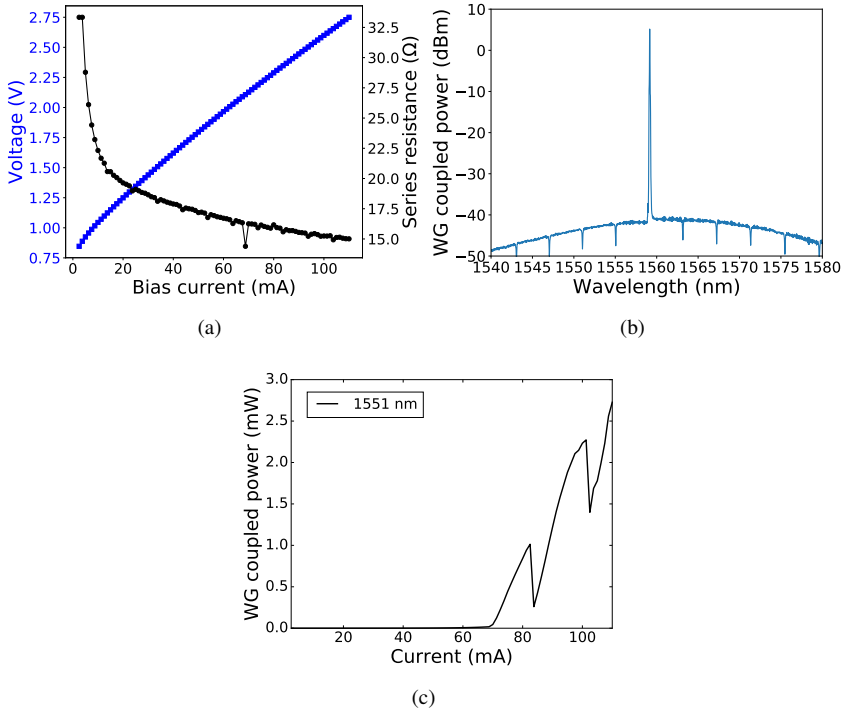
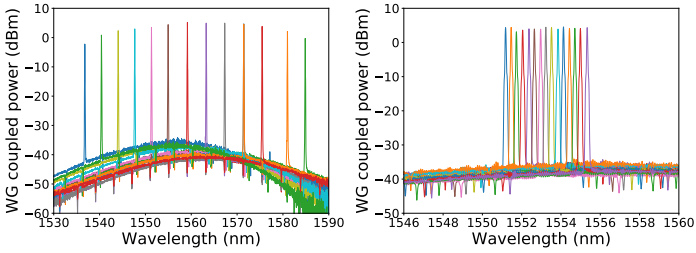


Figure 4.50: (a)V-I curve and differential resistance, (b) Recorded laser spectrum around 1560 nm, (c) P-I curve of the fabricated tunable laser.

the transfer-printed SOA is $15\,\Omega$ at a bias current of 110 mA, which is bit high for such a long device. Such a high resistance is probably because of an imperfect n-via opening and thus a poor connection between n-type contact metal to the probing contact. A $\sim 6\,\Omega$ series resistance, which is comparable with the lasers demonstrated via bonding is obtained in other fabrications using the same prefabricated SOAs. Fig. 4.50(b) shows a laser spectrum close to the gain peak (1559 nm) at a bias current of 110 mA. The side mode suppression ratio (SMSR) and waveguide coupled power is found to be 45 dB and 6 dBm, respectively. A representative P-I curve obtained at $20\,^{\circ}\mathrm{C}$ is shown in Fig. 4.50(c), revealing a threshold of 70 mA and waveguide-coupled output power over 2 mW at a bias current of 110 mA. Two abrupt changes of the output power shown on the PI curve indicate the mode hopping resulting from the phase variation when sweeping the bias current.

In the wavelength tunability test, the bias current was fixed at 110 mA. By adjusting the applied voltage and thus dissipated thermal power to one of the microheaters over the rings and fine-tuning the phase section and the tunable reflector, a discrete tuning over 48 nm is achieved. Fig. 4.51(a) shows superimposed output



(a) (b)

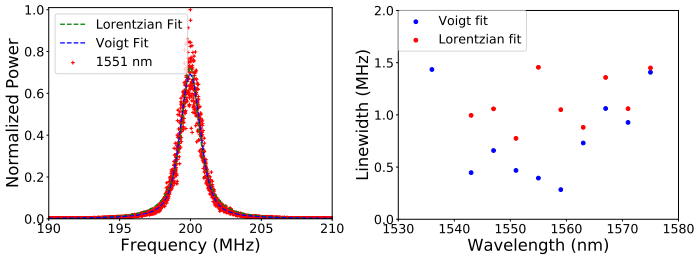
Figure 4.51: Overlaid output spectra of the tunable laser, showing a 48 nm tuning range. (b) Fine tuning over a wavelength range of 4 nm.

spectra, which reveals a waveguide coupled power variation between -1.8 dBm and 5.2 dBm over the entire tuning range. To fill the interval between the discrete lasing wavelengths, a fine-tuning with smaller tuning step is required. An effective way to realize that is by discretely tuning the lasing to a wavelength that is close to the target wavelength, followed by a simultaneous adjustment of both the micro-rings and a careful tuning of the phase shifter to maximize the output power. Fig. 4.51(b) shows a representative fine-tuning over an entire FSR (4 nm) of the $25\,\mu\mathrm{m}$ diameter ring resonator.

A linewidth measurement was also conducted using the same delayed heterodyne setup presented earlier in this chapter. As an example, Fig. 4.52(a) shows the beat note at 200 MHz with fitting curves based on the Lorentzian and Voigt functions, respectively. The results as a function of the lasing wavelength are shown in Fig. 4.52(b). A minimal intrinsic linewidth of 300 kHz (Voigt fitting) is achieved around 1560 nm, where is the peak of the gain spectrum, and it decreases with the decrease of the gain (off the gain peak).

4.6 Conclusion

In this chapter, after a brief introduction a few essential components on the imec 400 nm Si photonic platform are presented. With these building blocks, we designed and demonstrated two different types of widely tunable lasers via the well established DVS-BCB adhesive bonding technique and the μTP technique, respectively. Micro-ring based Vernier filters are incorporated in these laser cavities to achieve single mode operation and a broad tuning range over 40 nm. The wavelength tuning is achieved by thermally tuning the resonance wavelength of the micro-rings (thus the Vernier filter) and the phase section. In the first demonstration, a ring shape laser cavity with an overall length of 6 mm is used and, the incorporated micro-ring resonators have a loaded Q-factor around 17000. By intro-



(a) (b)

Figure 4.52: (a) A representative frequency spectrum of a beating note at 200 nm MHz with Lorentzian fitting and Voigt fitting, (b) Recorded linewidth as a function of the emission wavelength as measured using a delayed self-heterodyne measurement scheme.

ducing an external feedback to the laser cavity using a broad band DBR to couple the clockwise and counterclockwise mode of the ring laser cavity, unidirectional operation is obtained over the entire tuning range with about 10 dB suppression of the clockwise mode. The waveguide-coupled output power varies between 1.5 mW and 3.3 mW for a gain section bias current of 100 mA, which is more smooth compared with the laser without external feedback. The laser linewidth is consistently below 1 MHz, which enables the use of this laser as light source and/or local oscillator for an integrated QPSK coherent transceiver. More importantly this work verifies the feasibility of the use of a micro-ring based Vernier filter for a widely tunable and narrow linewidth laser on the imec 400 nm Si photonic platform. In the second demonstration, we proposed a III-V/Si coupling structure with up to $1\,\mu\mathrm{m}$ alignment tolerance for the μTP-based III-V-on-Si laser integration. The pre-fabrication of the SOAs on the native III-V epitaxial wafer and the integration of such pre-fabricated SOAs on Si PICs are presented. A linear laser cavity with an overall return length of 6 mm is used in this demonstration. The micro-ring resonators used in this laser demonstration have a higher loaded Q-factor of 34500. A $1\,\mu\mathrm{m}$ thick SiO_2 (rather than DSV-BCB) spacer layer is used between the Si waveguide and the micro-heaters to improve the adhesion of the deposited Ti/Au to the spacer layer. In this way the maximal dissipation in the heaters is significantly improved and a 48 nm wavelength tuning with a continuous tuning capability within the FSR of the ring resonators is achieved. The linewidth of the laser is below 1.5 MHz over the entire tuning range and the minimal intrinsic linewidth is found to be 300 KHz around the gain peak. As an initial demonstration this work verifies the feasibility of the µTP based integration of III-V-on-Si tunable lasers. By transfer printing the pre-fabricated III-V devices, which were pre-fabricated in dense arrays on a III-V epitaxial wafer, this demonstration show-

case the improved efficiency of the III-V material use and significantly simplified fabrication process flow for the integration of III-V-on-Si integrated devices/PICs.

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5

Towards fully integrated coherent receivers

5.1 Introduction

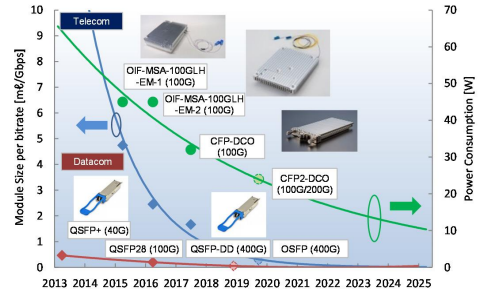
In the fourth chapter, we verified the feasibility of the integration of III-V-on-Si widely tunable lasers on the imec 400 nm photonic platform by micro-transfer-printing(μTP) of pre-fabricated III-V SOAs. In this way a simple post-processing for merely the metal wiring and probing pads definition is needed post μTP. Besides this 400 nm passive photonic platform, the 220 nm crystalline Si layer together with the 160 nm thick poly-Si layer on the iSiPP 25G/50G platform also allows for the optical coupling between the III-V and Si waveguide layer, making this platform a better choice for realising fully integrated ICRs. In this chapter we aim at realizing more complex III-V-on-Si integrated photonic circuits (PICs) : fully integrated coherent receivers (ICRs) with integrated local oscillator (LO). This chapter starts with a brief introduction of the principle and the basic configuration of the ICR. In the second section we will focus on the realization of fully integrated ICRs on passive PICs realized on a silicon on insulator (SOI) substrate with 400 nm Si device layer. The design and performance of the 90° optical hybrid, micro-ring resonators and LOs, and the fabrication of ICRs will be discussed. In the third section we will first present the design of a Si ICR on the imec iSiPP25G photonic platform. Then a demonstration of the co-integration of such an ICR with a TIA array will be presented. Given the verified performance of the existing Si ICR on the iSiPP25G platform, this section continues with an introduction of

a fully integrated ICR design on the imec iSiPP50G platform. The design of this Si ICR and the progress that has been made towards the realization of III-V-on-Si laser sources (LOs) on the iSiPP50G platform will be discussed.

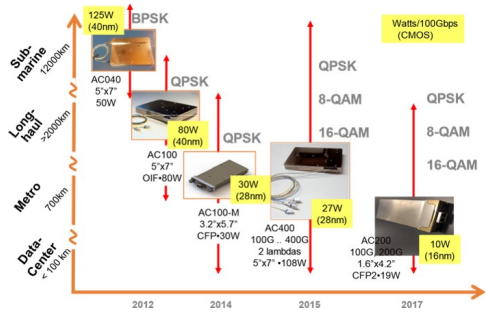
5.2 Integrated coherent receivers

Driven by the increase of the popularity of social media, data services, data storage in the cloud, etc., the explosive growth of the internet traffic in recent decades led to a renewal of intensive research on coherent technologies. By implementing multi-level modulation formats in terms of IQ modulation, coherent communication systems can provide a high bit rate to symbol rate ratio and thus a significantly enhanced spectral efficiency. By exploiting the optical polarization, the capacity of the network can be doubled again. Last but not least coherent technologies allow for the electronic compensation of linear and non-linear impairments of the transmission link [1–3]. Thanks to the rapid development of CMOS technology, high performance DSP which is able to handle 100 Gbit/s coherent detection was available around 2002, which immediately led to the update of long haul communication systems from 10 Gbit/s to 100 Gbit/s. Currently, considerable effort is being devoted to the evolution towards 400 Gbit/s, 800 Gbit/s and even higher aggregate bandwidth. [4–7].

Beside high capacity the cost, footprint and power consumption of the critical components (especially optical transceivers) are expected to be significantly reduced to allow for their deployment not only in long haul communication systems but also in metropolitan area networks and even in the access domain in the future. Fig. 5.1(a) shows a prediction of the evolution of optical coherent transceivers in the coming years. As can be seen, the power consumption and the size of the module has been significantly reduced over the past few years and this trend will continue in the coming years. A lot of effort is being devoted in this field, from both academia and industry, to keep up with this trend. As an example, Fig. 5.1(b) shows the development of the Si photonics ICR products (with DSPs in these modules) from Acacia. It is widely accepted that the only route to shrink the footprint of the optics part is photonic integration. Several photonic integration platforms are being considered for the implementation of these devices, including the use of silica-based planar lightwave circuits [8], InP-based PICs [9], and Si photonics [10]. These approaches have their respective pros and cons. The planar lightwave circuits are mainly fabricated in silica or polymer with relative low refractive index and low index contrast, which leads to a low waveguide propagation loss and efficient coupling with optical fiber. Nevertheless, complicated hybrid integration of the light sources and other active devices is required. InP-based integrated devices/circuits have been dominating the market of integrated photonic devices/PICs in the past years since most commonly used functionalities



(a)



(b)

Figure 5.1: (a) A prediction of technology development in coherent transceivers in the coming years [12], (b) Evolution of Acacia's Si photonic ICR modules in terms of power consumption and component density per 100 Gbit/s [13].

can be integrated on a single chip, however with relatively high cost due to the expensive III-V epitaxial materials and the requirement of a dedicated fabrication line. Compared with these two platforms Si photonics exhibits many advantages, *e.g.* high index contrast, CMOS compatibility and high volume production by using 200 mm or 300 mm wafers, which lead to a significant reduction of the cost, footprint and power consumption of the resulting PICs, with shortcoming of the lack of light sources. A commonly implemented approach for the laser integration in today's industry is through horizontal coupling (*e.g.*, lensed-coupling and butt-coupling) [11], nevertheless time-consuming active alignment is required in this integration procedure. In 2016 intel released the first Si photonic transceiver with heterogeneously integrated laser source via die-to-wafer boning (Fig. 5.2), which started a new era of fully integrated Si photonics transceivers.

Figure 5.2: The first commercial optical transceiver with heterogeneously integrated laser.

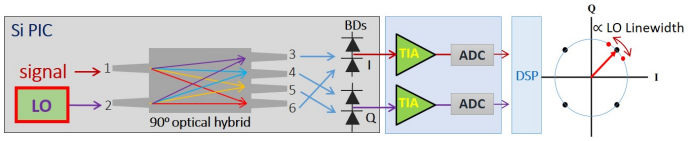


Figure 5.3: Schematic of a single polarization ICR.

5.2.1 Balanced coherent detection

In a coherent system the data signal is imprinted on the optical carrier via optical phase modulation (BPSK, QPSK, DQPSK, etc.), or together with amplitude modulation (X-QAM). To extract the phase information carried by the optical signal an absolute phase reference is normally required at the receiver side. This absolute phase reference is provided by a narrow linewidth laser, the local oscillator (LO). Usually a wide tuning range is also required for the implementation of WDM/DWDM solutions. Fig. 5.3 depicts a typical schematic diagram of a balanced coherent detection configuration (single polarization coherent receiver), where the incoming signal is first mixed with the LO via a device named optical hybrid, which introduces a certain phase delay to the mixed optical signals to enable the phase extraction via a balanced detection. A 90° optical hybrid, as its name indicates, introduces a 90° phase difference among these four channels. It is usually implemented using a cascaded 2×2 MMIs structure or simply a 4×4 MMI coupler [14, 14–18]. Alternatively, a 120° hybrid realized by a 3×3 MMI coupler can be adopted for the same purpose [10]. A balanced detector (BD) is realized by cascading two photodetectors (PDs) in the head-to-toe configuration, as depicted in Fig. 5.4. The BD eliminates the need for direct detection components.

The principle of balanced coherent detection is now briefly introduced. Let the electric field of the LO and received signal be

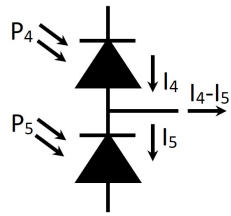


Figure 5.4: Schematic of balanced detection.

$$\begin{aligned} E_L(t) &= A_L(t)exp(i(2\pi f_L t + \Phi_L(t))), \\ E_S(t) &= A_S(t)exp(i(2\pi f_S t + \Phi_S(t))). \end{aligned} \tag{5.1}$$

Where A_L, f_L and Φ_L represent the complex amplitude, optical frequency and absolute phase of the LO signal, while A_S,f_S and Φ_S are used to describe the input optical signal. The mixed optical signals at the output of the 90° hybrid are expressed as:

$$\begin{aligned} E_3(t) &= E_S(t) + E_L(t), \\ E_4(t) &= E_S(t) + iE_L(t), \\ E_5(t) &= E_S(t) - iE_L(t), \\ E_6(t) &= E_S(t) - E_L(t). \end{aligned} \tag{5.2}$$

The corresponding optical power of the mixed optical fields are:

$$\begin{aligned} P_3(t) &= P_0 + 2|E_S(t)| \cdot |E_L(t)| \cdot cos(2\pi\Delta f t + \Phi(t)), \\ P_4(t) &= P_0 + 2|E_S(t)| \cdot |E_L(t)| \cdot sin(2\pi\Delta f t + \Phi(t)), \\ P_5(t) &= P_0 - 2|E_S(t)| \cdot |E_L(t)| \cdot sin(2\pi\Delta f t + \Phi(t)), \\ P_6(t) &= P_0 - 2|E_S(t)| \cdot |E_L(t)| \cdot cos(2\pi\Delta f t + \Phi(t)). \end{aligned} \tag{5.3}$$

where $P_0 = |E_S(t)|^2 + |E_L(t)|^2$ and $\Delta f = f_S - f_L$. The DC terms are discarded by implementing a subtraction via the balanced detection. The resulting photocurrents, which represent the in-phase (I) and quadrature (Q) components are obtained as:

$$\begin{aligned} I_Q(t) &= I_3(t) - I_6(t) = 4R|E_S(t)| \cdot |E_L(t)| \cdot cos(2\pi\Delta f t + \Phi(t)), \\ I_I(t) &= I_4(t) - I_5(t) = 4R|E_S(t)| \cdot |E_L(t)| \cdot sin(2\pi\Delta f t + \Phi(t)). \end{aligned} \tag{5.4}$$

In the above derivation, we assumed that all the PDs have identical responsivities, denoted by R. When the optical frequency of the LO perfectly matches that of the input optical signal ($\Delta f = 0$) the coherent detection is categorized as homodyne detection, otherwise it is called heterodyne detection. As shown in Eq. 5.4

the amplitudes of the resulting photocurrents are a product of the amplitudes of the input signal and LO, indicating an enhanced detection sensitivity. By plotting the received complex signals (I_I(t), I_Q(t)), a constellation diagram is obtained. Assuming that the LO does not have phase noise or intensity noise (however it is not possible), these points will be well defined and located at the ideal locations, as shown in Fig. 5.3. As all the terms in Eq. 5.4 contain noise, which together with distortion and other impairments leads to a symbol cloud. When these clouds get close to each other, the decoding will lead to more symbol errors.

Above we briefly explained the principle of the balanced coherent detection. As our main focus is the development of the III-V-on-Si integration processes, the detailed theory will not be covered.

5.3 Realization of integrated coherent receivers on 400 nm PICs

To accelerate the fabrication cycle, PICs patterned on a blank SOI chip by e-beam lithography (Raith-VOYAGER) and RIE dry etching in the Ghent university cleanroom were used. A blank SOI wafer consisting of a 400 nm thick crystalline Si device layer and a 2 µm thick buried oxide layer was used to fabricate the Si waveguide circuits. These processes were carried out by Dr. Sulakshna Kumari. The e-beam system provides up to 50 kV acceleration voltage and a maximum writing field of $500 \times 500\,\mu\mathrm{m}^2$. A 200 nm thick positive resist (AR-P 6200) was used as a soft mask in the e-beam lithography. The PICs are realized by a 180 nm deep dry etching using an RIE tool with a gas mixture of (CF_4/SF_6/H_2). Note that stitching errors always occur between consecutive writing fields in the e-beam lithography process because of an imperfect alignment. These stitching errors will result in defects or even discontinuities in the patterned waveguides and hence an increased waveguide loss [19]. Besides the implementation of an optimized writing mode to reduce such misalignment, a Si taper structure with a wide waveguide across the boundaries of the writing fields can be used to reduce the impact of stitching errors due to a lower overlap of the guided mode with the sidewall of the waveguide.

5.3.1 Design of the integrated coherent receiver

A GDSII design of an integrated coherent receiver (ICR) is shown in Fig 5.5. This ICR consists of two tunable lasers (one as a backup) and a 4×4 MMI-based 90° hybrid onto which output ports are terminated with grating couplers where the III-V PDs will be transfer-printed. A directional coupler with an expected cross-coupling ratio of $5\,\%$ is inserted between the LO and the 90° hybrid to monitor the laser performance. As ring resonators are very sensitive to waveguide loss, they are carefully placed to avoid the stitching error.

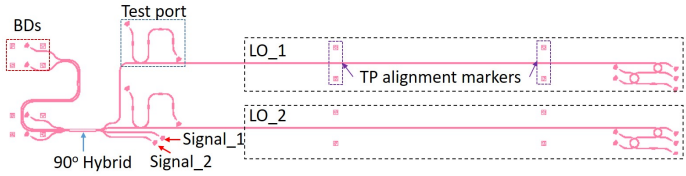


Figure 5.5: A GDSII layout of an ICR design.

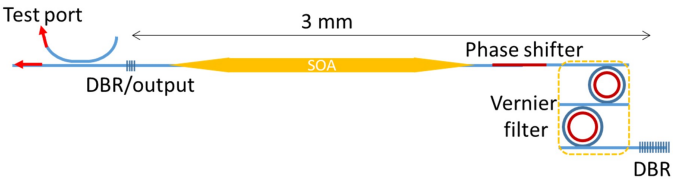
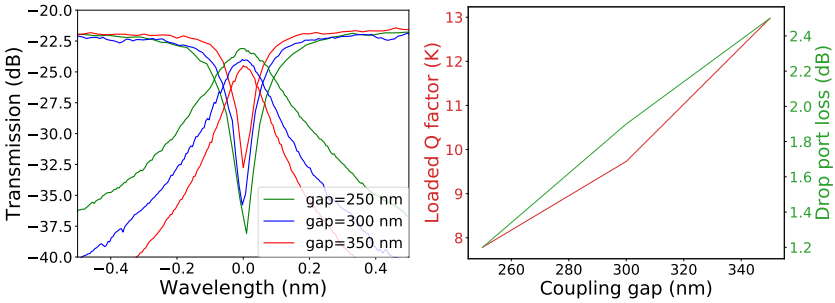


Figure 5.6: Schematic of the LO.

5.3.2 Design of local oscillator lasers

Fig. 5.6 shows the schematic of the LO design. The LO has a 3 mm long linear cavity formed by two DBR mirrors. Following the success of the use of ring-resonators for wide wavelength tuning, a micro-ring based Vernier filter is again used here to realize a 40 nm wavelength tuning. The active region is a $2.5\,\mu\mathrm{m}$ wide and $1360\,\mu\mathrm{m}$ long straight waveguide which is tapered to 650 nm wide single mode waveguides at both sides. To enable the pattern recognition and automatic printing, a set of alignment markers are defined at the sides of the active region. The directional coupler has a coupling gap and straight section of 250 nm and $2.5\,\mu\mathrm{m}$, respectively. All the waveguides are terminated with reflectionless grating couplers to interface with optical fibers or to reduce the back-reflection to the laser cavity. The wavelength tuning and phase adjustment will be realized by using a set of integrated Ti/Au micro-heaters.

The DBR mirrors are patterned on a $3\,\mu\mathrm{m}$ wide waveguide with 12 and 30 periods, respectively. The period and the duty cycle are 258 nm and $60\,\%$, respectively, for both of them. The shorter DBR, whose simulated reflectivity is about $70\,\%$, is used as the output and is connected to the active section (a $2.5\,\mu\mathrm{m}$ wide waveguide) via a linear taper structure. Ring resonators with coupling gaps of 250 nm, 300 nm and 350 nm were investigated. Fig. 5.7 shows the measured spectra of a set of $25\,\mu\mathrm{m}$ diameter devices. With an increase of the coupling gap from 250 nm to 350 nm, the loaded Q factor increases from 7800 to 13000 and the drop-port loss increases from 1.2 dB to 2.5 dB. Compared with the ring resonators realized on the imec 400 nm photonic platform, the loaded Q factor of the e-beam patterned devices are halved but the drop port loss is almost doubled due to the higher



(a) (b)

Figure 5.7: (a) Measured transmission spectra of the ring resonators with different coupling gaps. (b) Loaded Q-factors and drop port losses of the ring resonators as a function of the coupling gap.

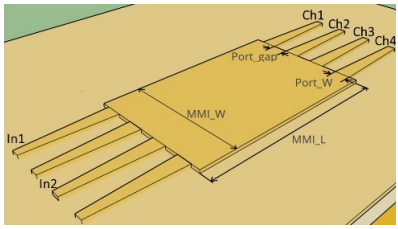


Figure 5.8: Schematic of the 90° hybrid.

waveguide loss.

In such a linear laser cavity the optical field passes by the Vernier filter twice. Assuming that the ring resonators have a Q-factor of 9700 (300 nm coupling gap) and their resonances are perfectly aligned, the FWHM of the combined resonance spectrum is calculated to be 86 pm (loaded Q-factor of 18000), which is comparable to the longitudinal cavity mode spacing at resonance (72.6 pm) and allows for single-mode operation.

5.3.3 90° hybrid

A 4×4 MMI coupler is designed for the 90° optical hybrid. Compared with the Si photonic ICR reported in [18], the use of a 4×4 MMI coupler leads to a smaller footprint and does not require additional thermal tuners to control the relative phases at the output of the 90° hybrid. Therefore less bond pads and control circuits are required, which further reduces the chip-size and cost. The layout of the MMI based 90° hybrid is shown in Fig. 5.8. The nominal device parameters are MMI_W=9 µm, MMI_L=175 µm, Port_W=1.6 µm, Port_{gap}=0.66 µm.

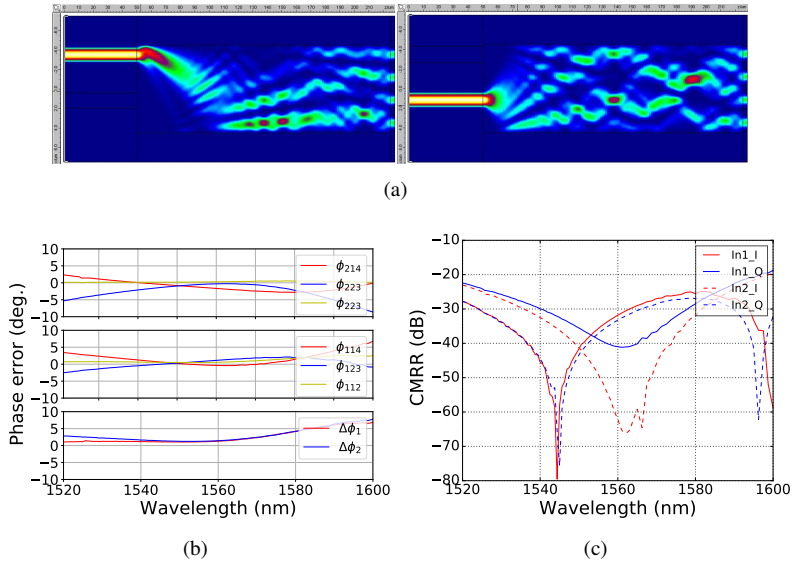


Figure 5.9: (a)Simulated optical mode propagation in the 4×4 MMI with the fundamental quasi TE mode launched into different input ports. (b) Simulated phase error and (c) CMRR as function of wavelength.

The design and optimization of the 90° hybrid were performed using FIMMWAVE. In the simulation, the fundamental TE mode is launched into one of the input ports, and the transmission together with the phase delays are recorded for further analysis. Fig. 5.9(a) depicts a representative mode evolution in the multimode section of 90° hybrid. Fig. 5.9(b) shows the wavelength dependence of the phase difference between the output ports. Here $\phi_{ijk} = \phi_{ij} - \phi_{ik}$. ϕ_{ij} is the phase delay from input in$_i$ to output ch$_j$. $\Delta\phi_1 = (\phi_{11} - \phi_{21}) - (\phi_{14} - \phi_{24}) - \pi$ and $\Delta\phi_2 = (\phi_{12} - \phi_{22}) - (\phi_{13} - \phi_{23}) - \pi$. Assuming an allowable phase difference deviation of 5°, operation over the C-band is achieved. The simulated common mode rejection ratio (CMRR= $20{\cdot}log_{10}((T_{ij} - T_{ik})/(T_{ij} + T_{ik}))$, with T_{ij} the power transmission from input in$_i$ to output ch$_j$, is better than -20 dB over the C-band, as revealed in Fig. 5.9.

5.3.4 Laser fabrication

A 1:8 DVS-BCB (CYCLOTENE 3022-35):Mesitylene solution is used as the adhesive bonding agent. It was spin-coated on the PICs at a speed of 3000 rpm for 40 seconds, followed by a soft bake at 150 °C for 10 minutes. A PDMS stamp with a $50 \times 1400\ \mu m^2$ post was used to transfer print the pre-fabricated SOAs. In the μTP process, the target sample stage was heated up to 70 °C to achieve 100 % printing

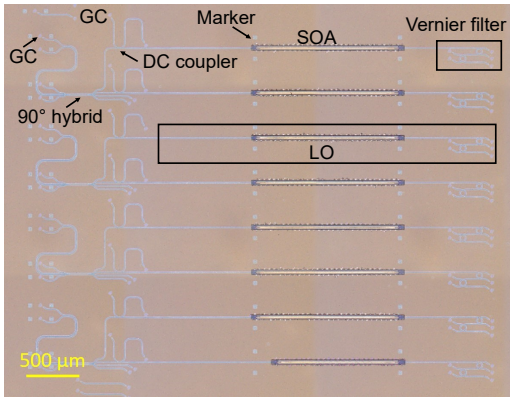


Figure 5.10: Top view microscope image of an array of ICRs with transfer printed pre-fabricated SOAs.

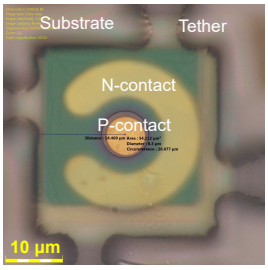


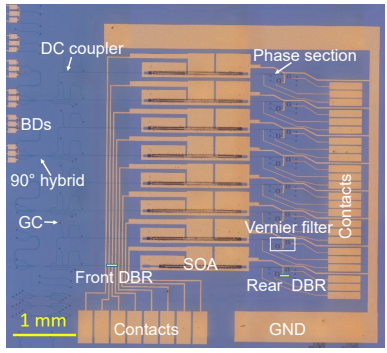
Figure 5.11: Microscope image of one C band PD on the source wafer.

yield. The Si PICs with an array of transfer printed SOAs are shown in Fig. 5.10. The fabrication post µTP follows the process flow described in the fourth chapter.

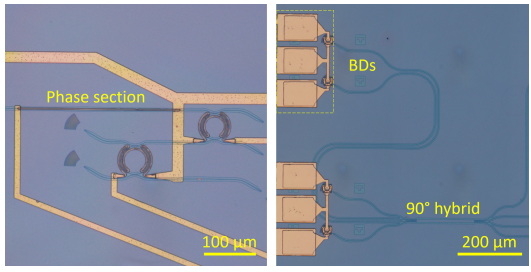
5.3.5 Transfer printing of pre-fabricated C band PDs

The III-V epitaxial material used for the C band PD is similar to that used for the O band TPD, but with a $1\,\mu m$ thick InGaAs absorption layer. Stand-alone PDs are designed in a dense array with different aperture size of $8\,\mu m$, $10\,\mu m$ and $12\,\mu m$ in diameter. The PD mesa is around $35 \times 35\ \mu m^2$. The pre-fabrication of III-V PDs on the InP substrate was carried out by Dr.Grigorij Muliuk. The pre-fabricated PDs were released by immersing in a 3° aqueous $FeCl_3$ for 80 minutes. Fig. 5.11 shows a zoom-in image of a PD after the release etching.

When the laser fabrication post-process flow was accomplished, the sample was again spin-coated with a 1:4 DVS-BCB (CYCLOTENE 3022-35):Mesitylene solution. Stand-alone III-V PDs with $8\,\mu m$ diameter aperture were used in this demonstration. A PDMS stamp with a $50 \times 50\ \mu m^2$ post was used to pick-up and



(a)



(b) (c)

Figure 5.12: (a) Microscope image of an array of fabricated ICRs. (b) Zoom-in images of (b) ring resonators with micro-heaters and phase section and (c) integrated BDs with 90° hybrid.

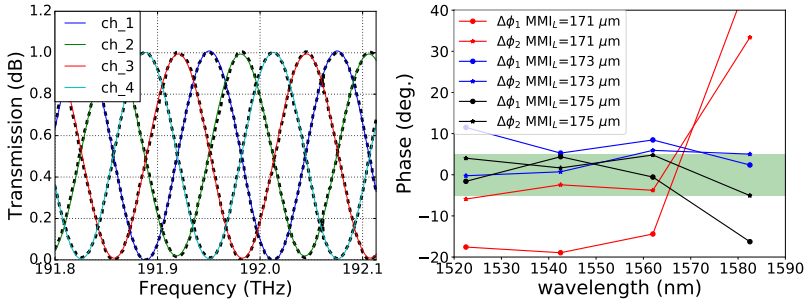
print these PDs. The printing of the PDs was carried out with the help of the pattern recognition and auto-alignment function at room temperature. The balanced PD configuration is realized by connecting the n-contact of one PD to the p-contact of the neighboring PD. The fabricated ICRs are shown in Fig. 5.12.

5.3.6 Characterization

5.3.6.1 90° hybrid

An unbalanced MZI structure consisting of a 90° hybrid and a 2×2 MMI splitter are designed to study the inherent phase delay induced by the 90° hybrid. The two output ports of the 2×2 MMI are respectively connected to the input ports in_1 and in_3 of the 90° hybrid. The physical path difference between the MZI interfering arms is $620\,\mu\text{m}$, which results in a 125 GHz FSR.

A Santec 510 tunable laser together with a HP power meter were used to characterize the transmission of the MZI structures. To avoid phase variation induced



(a) (b)

Figure 5.13: (a) Normalized transmission spectra of a 90° of hybrid in frequency domain. (b) Phase errors extracted from the measured spectra for a 90° hybrid width different length of the multimode section.

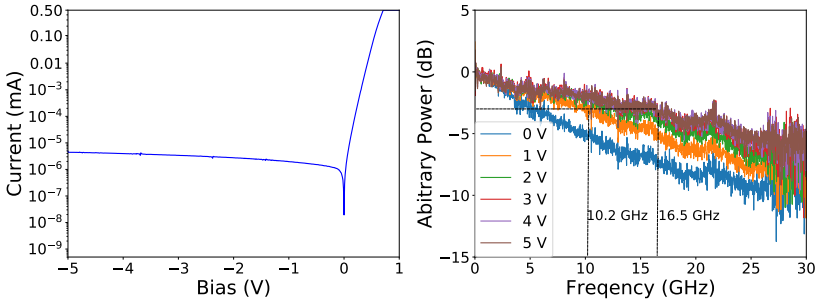
by ambient temperature fluctuation the temperature of the sample stage was stabilized at $20\,^\circ\mathrm{C}$ in the measurement. Fig. 5.13(a) shows superposed transmission spectra of a test structure with a 90° hybrid with a $175\,\mu\mathrm{m}$ long multimode section. A sine fitting is implemented to extract their relative phases. As shown in Fig. 5.13(a) the black dash lines are the normalized spectra and the solid lines represent the fitting curves. The extracted phase differences are shown in Fig. 5.13(b). As can be seen, less than 5° phase deviation over the entire C band is obtained for the device with a $175\,\mu\mathrm{m}$ long multimode section.

5.3.6.2 Static measurement of the transfer printed III-V-on-Si PDs

Fig. 5.14(a) shows the V-I curve of an integrated PD. The measurement was carried out without optical input, by sweeping the bias voltage. The dark current is within a range from 1.5 nA to 5 nA with a bias voltage increasing from -0.5 V to 5 V. The series resistance of the PD is around $300\,\Omega$, which is attributed to the small dimension of the PD.

Unfortunately a high and inconsistent waveguide loss was observed in the measurement so that it is difficult to obtain a reliable responsivity. From our experience the responsivity of a grating assisted PD is expected to be around 0.5 A/W. The failure of the waveguides is suspected to be resulting from some severe stitching errors. This issue will be overcome by using a PIC on the imec 400 platform.

To investigate the bandwidth of the fabricated PDs, small signal characterization using a Vector Network Analyzer (VNA) was carried out. Fig. 5.14(b) shows a set of small signal responses of a fabricated PD at different bias voltages. As can be seen the 3 dB bandwidth without biasing is less than 5 GHz. It increases to and saturates at 16 GHz when the bias voltage is above 3 V. The bandwidth of the



(a) (b)

Figure 5.14: (a) Measured V-I curve and (b) $|S_{21}|^2$ curves of an transfer printed PD with $8\,\mu m$ diameter mesa, showing a saturated small signal bandwith of 16.5 GHz.

PD is suspected to be limited by a large RC time constant resulting from the high series resistance.

5.3.6.3 Characterization of the transfer printed III-V-on-Si tunable lasers

Again because of the high waveguide loss, it is difficult to evaluate the performance of the fabricated lasers, however these devices were found to be lasing and the lasing wavelength can be tuned over a 40 nm range. Fig. 5.15 shows the performance of a fabricated LO. The differential resistance of this laser is $12\,\Omega$ at a bias current of 185 mA, which is comparable with that of tunable lasers demonstrated on the imec 400 nm platform, while a higher threshold current (128 mA) is observed from the P-I curve. Fig. 5.15(c) depicts a representative wavelength tuning over a tuning range of 40 nm and a fine-tuning around 1550 nm.

To conclude, we co-integrated an array of III-V PDs and widely tunable lasers on a common target Si PIC via μTP. Unfortunately we were not able to demonstrated an ICR due to the failure of the waveguide circuits. Nevertheless, this work verifies the feasibility of the close co-integration of multiple III-V functionalities on a Si PIC. As μTP of III-V PDs and tunable lasers have been successfully demonstrated and the co-integration of these devices proved to be feasible, it is promising to realize such ICRs using deep UV patterned Si photonic circuits.

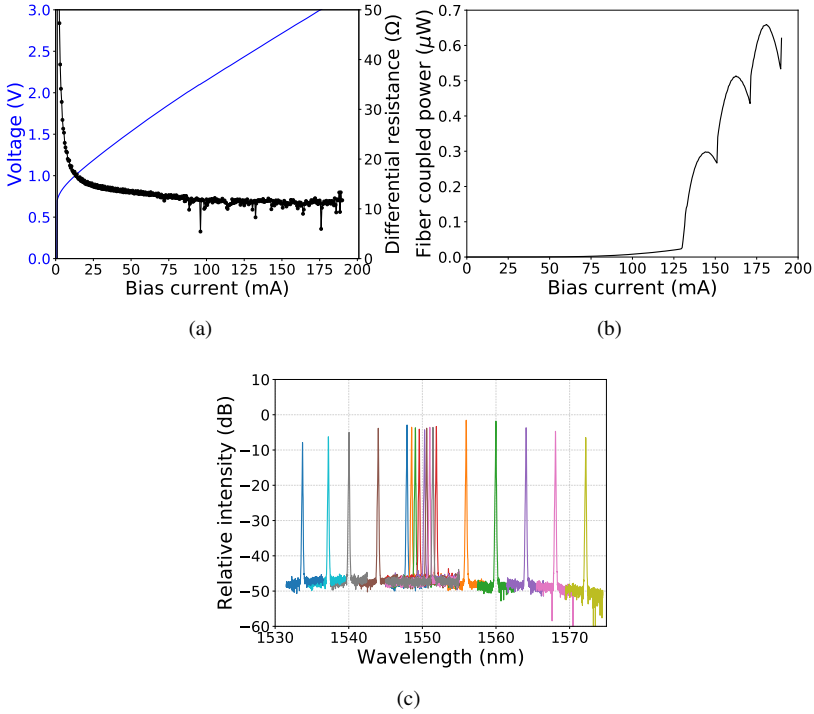


Figure 5.15: (a) Measured V-I curve, (b) P-I curve and (c) superimposed spectra of a fabricated LO.

5.4 Realization of ICRs on the imec iSiPP25G/50G platform

As discussed in the fourth chapter, the imec iSiPP 25G platform provides not only high performance passive devices but also Si and Si/Ge active devices with at least 25 Gbit/s bandwidth, which enable the realization of ICRs with ultra-compact footprint and low power consumption. Again as no hermetic packaging is needed, the cost of the resulting packaged devices can be further reduced. Today, an iSiPP50G platform with active components allowing for at least 50 Gbit/s operation is available.

In this section a sub-block of a Si ICR is at first presented. As shown in Fig. 5.16, it consists of an ultra-compact coherent receiver ($0.3 \times 0.7\,\mathrm{mm}^2$) co-integrated with a low power consumption linear TIA array. A $90°$ hybrid with dimensions of $13.7\,\mu\mathrm{m}$ by $155\,\mu\mathrm{m}$ is used to mix the incoming signal with an external narrow linewidth laser (LO). Here high-speed Ge PDs instead of III-V-on-Si integrated PDs are implemented at the outputs of the $90°$ hybrid. As a proof-of-

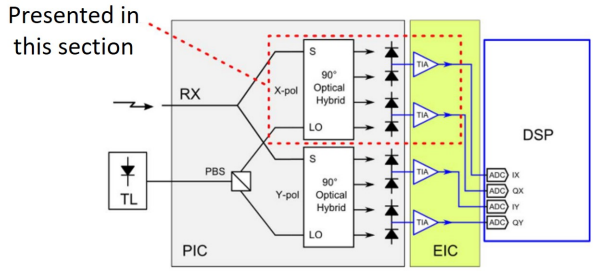


Figure 5.16: Envisaged Si photonic ICR consisting of an electronic (EIC) and photonic (PIC) integrated circuit.

principle, a single polarization ICR is demonstrated in this work. The 2-channel linear single-ended input TIA array is designed in $0.13\,\mu\mathrm{m}$ SiGe BiCMOS technology. Besides for linearity, the electronic circuit is optimized for low power consumption. As will be discussed later, a single TIA operating at 28 Gbaud consumes only 155 mW, a substantial improvement over previous demonstrations of ICRs [20, 21]. In this work, 28 Gbaud quadrature phase shift keying (QPSK) and 16-quadrature amplitude modulation (16-QAM) reception are demonstrated using the Si ICR integrated with the 2-channel TIA array. In both cases the receiver can operate below the forward error coding (FEC) limit (3.8×10^{-3}) at $7\,\%$ overhead). For QPSK less than 12 dB/0.1 nm optical signal to noise ratio (OSNR) is required to realize this, 2.5 dB above the theoretical limit.

5.4.1 Si photonic integrated circuit design

The layout of the PIC is shown in Fig. 5.17. The circuit occupies an area of 0.3 mm by 0.7 mm. It consists of single-polarization fiber grating couplers for coupling the advanced modulation format signal and LO to the chip. The insertion loss of the fiber grating coupler at 1550 nm is -6.5 dB. The -1dB bandwidth is 20 nm. Higher efficiency single polarization grating couplers [22] as well as two-dimensional grating couplers [23] for polarization diversity are also available on this platform. The layout of the 90° hybrid is shown in Fig. 5.18(a), where the back-end dielectric stack is removed for clarity. It is a 2×4 MMI, consisting of deeply etched entrance and exit waveguides defined in a 220 nm thick waveguide layer, while the multimode section is shallowly etched (70 nm) in order to reduce phase errors and power imbalance at the output [15]. The nominal device parameters are $\mathrm{MMI}_L = 115.5\,\mu\mathrm{m}$, $\mathrm{MMI}_W = 7.7\,\mu\mathrm{m}$, $\mathrm{Port}_W = 1.5\,\mu\mathrm{m}$, $\mathrm{Port}_{gap} = 0.5\,\mu\mathrm{m}$, $\mathrm{TR}_W = 3\,\mu\mathrm{m}$. The simulated wavelength dependence of the phase difference between the different output ports is shown in Fig. 5.18(b). The simulated CMRR is better than -25 dB over the C-band, as revealed in Fig. 5.18(c). Unfortunately, we

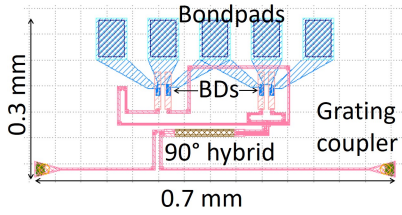


Figure 5.17: Layout of the single polarization coherent receiver with a footprint of 0.3 mm by 0.7 mm.

could not characterize the phase difference deviation of the hybrid as no MZI test structure was added in this design. However, a maximal OSNR penalty of $\sim$ 2 dB over the entire C+L band achieved by the demonstrated coherent receiver somehow verifies small phase difference deviations ($\Delta\phi_1$,$\Delta\phi_2$) for this 90° hybrid.

High-speed Ge PDs are implemented at the output of the 90° hybrid. The characteristics of an individual PD integrated on the same chip as the ICR are shown in Fig. 5.19. The individual PDs have a bandwidth above 50 GHz at -1 V bias thanks to the low junction capacitance, less than 15 nA dark current at -1 V bias and an on-chip responsivity of 0.5 A/W. Good uniformity over 200 mm wafers is obtained [24], important for chip yield and hence cost reduction. On-chip subtraction of the photocurrent was implemented to reduce the number of bondpads required (and thereby again the chip-size). While this approach doubles the capacitance of the optical receiver and thereby reduces the bandwidth [25], the high bandwidth of the individual PDs still allows for 28 Gbaud operation as will be demonstrated below. Also, the on-chip current subtraction prevents a substantial DC photocurrent from the PDs to be injected in the TIA, simplifying the design.

5.4.2 SiGe BiCMOS Linear TIA Array Design

The TIA array is designed by Bart Moeneclaey from the INTEC-Design group of Ghent University and is fabricated in a $0.13\,\mu\mathrm{m}$ SiGe BiCMOS technology. It consists of 2 identical copies of the same TIA in a mirrored configuration sharing a common ground, supply voltage (2.5 V for the analog parts and 1.2 V for the digital parts) and tunable bias voltage for the balanced PDs (set at $\sim$ 2.2 V in the experiments) [26, 27]. Furthermore, the serial peripheral interface controller is shared, and a single bias block provides a $100\,\mu\mathrm{A}$ reference current to each TIA. The total chip area is $3000 \times 900\mu\mathrm{m}^2$ of which each TIA occupies $1100 \times 900\mu\mathrm{m}^2$. A microscope photograph of the TIA array with annotated functional blocks and sizing is provided in Fig. 5.20. The electrical signal path consists of an input stage, the main amplifier, and an output stage. The input stage converts the current coming from the balanced PDs to a voltage signal through the feedback resistor RF, which

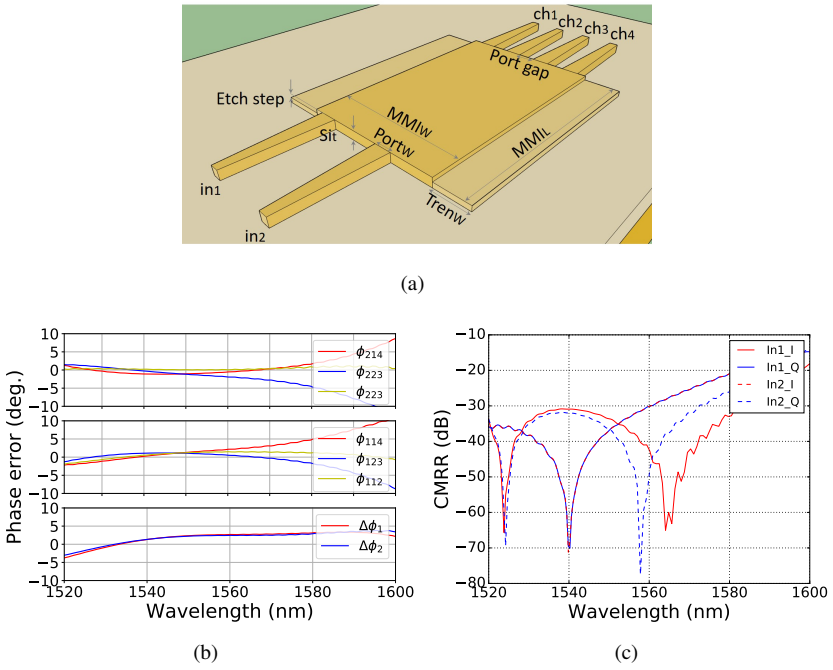
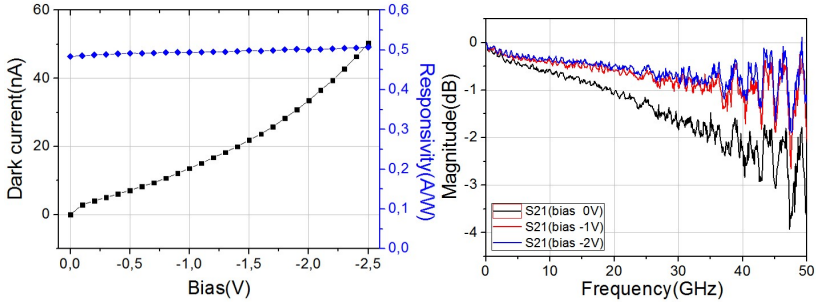


Figure 5.18: (a) Layout of the 90° hybrid realized on the imec iSiPP25G platform. Simulated (b) phase error and (c) CMRR of the device as a function of wavelength.

is implemented as an array of 8 parallel nMOS transistors operated in their linear region. As such, the gain of this stage can be controlled digitally by turning on (decreasing RF) or off (increasing RF) transistors from this array. A trans-impedance of 133 Ω is used in the experiment to strike a balance between the gain and bandwidth of the TIA. More information about the TIA design can be found in [26–28]

5.4.3 Electronic/photonic co-integration

While recently the monolithic integration of an ICR and TIA has been proposed and demonstrated [20], a hybrid integration over a monolithic approach is preferred in this work as it allows independent optimization of the used technology for the photonics and electronics, reducing the cost and allowing for commercial Si foundry services to be used. A close-up of the wire-bonded electronic and photonic die on the PCB is shown in Fig. 5.21. The developed Si photonic ICR and TIA array was integrated on a 4-layer PCB. The PCB wasn't minimized in size to enable easy testing and assembly. Both dies were placed in a cavity in the cen-



(a) (b)

Figure 5.19: Ge PD characterization (single element PD implemented close to the integrated receiver): (a) IV characteristic and responsivity as a function of reverse bias, (b) Normalized S21-parameter of the PD used in the coherent receiver as a function of reverse bias.

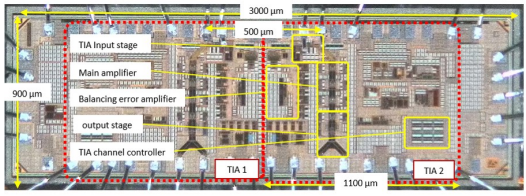


Figure 5.20: Top-view of the two-channel TIA with an indication of the position of the different functional blocks.

ter of the PCB to minimize the required wire bond length between the TIA and the traces on the PCB. Care was taken during the assembly to place the 2-channel TIA-die ($3 \times 0.9\ \mathrm{mm}^2$) and the Si PIC as close as possible together to also minimize the lengths of the interconnection wire bonds. The 2×2 differential outputs of the two-channel TIA were routed symmetrically to 4 high-speed connectors at the edge of the board. Due to limitations of the measurement setup in the lab, all measurements were however done single-ended by terminating the corresponding output of the differential signal with a DC-block and a $50\,\Omega$ termination.

5.4.4 System experiments

The measurement was conducted at room temperature without using temperature controller. For the 28 Gbaud QPSK measurement 12 dBm fiber-coupled LO power (∼5 dBm on-chip) was used. The on-chip signal power was -2.5 dBm. The transimpedance of the TIA was tuned to achieve optimal bit error rate (BER) performance for the given data rate (28 Gbaud) by trading off a lower gain (133 Ω) for higher bandwidth. The reverse bias of 2 V for the balanced PDs (1 V per diode)

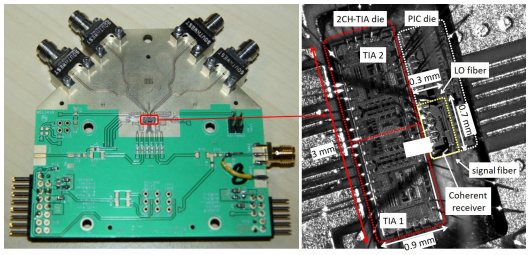


Figure 5.21: View of the PCB used for testing purposes with the Si photonic ICR and TIA array and a close-up of the wire bonded electronic and photonic die on the PCB.

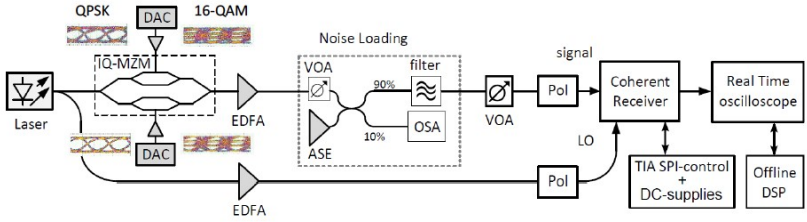


Figure 5.22: Schematic of the characterization setup of the receiver for QPSK and 16-QAM modulation.

was set through the TIA. The BER as a function of OSNR for 28 Gbaud QPSK is shown in Fig. 5.23(a), together with two representative constellation diagrams. The transmission is below the FEC-limit (i.e. 3.8×10^{-3} at $7\,\%$ overhead) for an OSNR of 12 dB/0.1 nm. The OSNR penalty with respect to the theoretical minimum is less than 2.5 dB. For 28 Gbaud 16-QAM our measurements are being limited by the performance of the DACs on the transmitter side. The minimal obtainable BER for this constellation using a commercial coherent receiver (picometrix), used as a benchmark for the system, saturated around 2×10^{-5}. Nevertheless, below FEC threshold operation was realized, as shown in Fig. 5.23(b) and Fig. 5.23(c) together with a representative constellation diagram. In Fig. 5.23(b) the LO power (in fiber) is swept for a constant signal power (4.5 dBm in fiber), while the signal power is swept for a constant LO-power (14.7 dBm in fiber) in Fig. 5.23(c). A regime of below FEC operation is obtained. In both curves the error rate increases again after a certain input power, indicating possible degeneration of the TIA due to high input current or saturation of the PDs because of the high optical input power

In the experiment at 28 Gbaud, the 2 channel TIA array consumes about 120 mA from the 2.5 V supply (both for QPSK and 16-QAM operation), yielding a low overall power consumption of 155 mW per TIA, a factor of three lower than

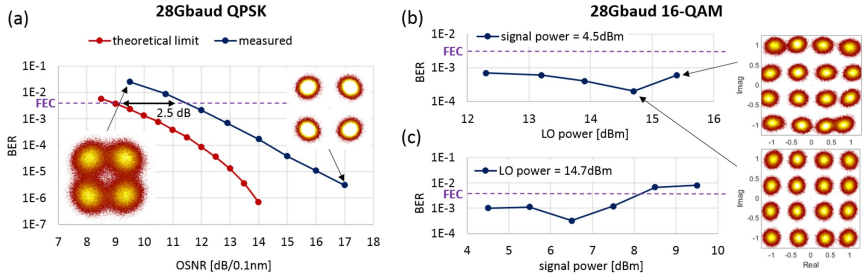


Figure 5.23: (a) BER versus OSNR curve for 28 Gbaud QPSK, (b) 28 Gbaud 16-QAM BER versus LO power together with representative constellation diagrams illustrating the BER degradation at higher LO power, (c) 28 Gbaud 16-QAM BER versus signal power. Below FEC operation is obtained.

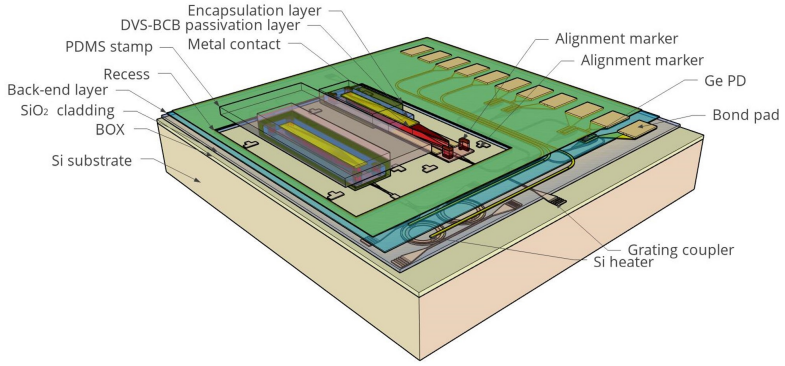
in [21] and a factor of 1.6 compared with [20]. Moreover, in a later measurement, a 40 Gbaud 16 QAM operation with a bit error rate less than 3.8×10^{-3} is achieved. More information about this demonstration is presented in [29].

5.4.5 Fully integrated Si photonic ICR on the imec iSiPP50G platform

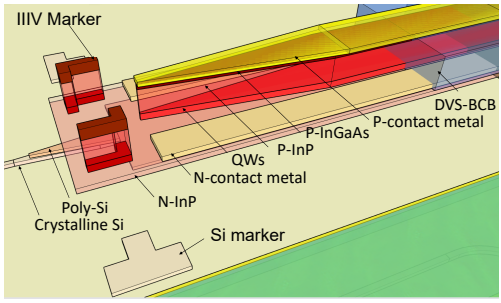
Most of the reported Si ICRs are similar to the aforementioned ICR, requiring external LOs interfaced with the PICs through edge couplers or fiber grating couplers [18, 30, 31]. Laser sources can be integrated via flip-chip or pick-and-place of micro-packaged laser, but these strategies are facing difficulty in scaling up the manufacturing and reducing the cost of the resulting modules due to the complicated assembly of the light source. Therefore a cost-effective solution for the on chip integrated lasers is desired [32]. An example of an ICR that can be realized via μTP is schematically shown in Fig. 5.24(a), where two LOs are co-integrated on the imec iSiPP50G platform with micro-heaters and germanium (Ge) PDs by μTP of pre-fabricated III-V amplifier structures in a recess that was defined .

5.4.5.1 Alignment tolerant III-V/Si taper structure

The 160 nm thick poly-Si layer together with the 220 nm thick crystalline Si layer on the imec iSiPP50G platform allows for the optical mode coupling between the III-V layer and the Si waveguide layer. Fig. 5.24(b) shows the proposed III-V/Si coupling scheme on the iSiPP50G platform. The mode coupling is realized in two steps. In the first step, a linear III-V taper structure is designed to couple the optical mode from the III-V/Si hybrid waveguide to the underlying poly-Si/Si layer, which is then connected to a 450 nm wide crystalline Si wire waveguide via



(a)



(b)

Figure 5.24: (a) Schematic of the ICR with integrated LOs via μTP on the imec iSiPP50G platform.(b) Schematic of the III-V/Si taper structure.

a poly-Si/Si taper.

This III-V/Si hybrid waveguide consists of a $5\,\mu\mathrm{m}$ wide III-V waveguide and a $3\,\mu\mathrm{m}$ wide Si waveguide with a thin DVS-BCB bonding layer in between. We first investigated the coupling from such a hybrid waveguide to the underlying poly-Si/Si waveguide. Fig. 5.25 shows the propagation of the $1.55\,\mu\mathrm{m}$ TE fundamental mode through the III-V/Si taper structure, where the lateral misalignment, the III-V taper length, the III-V taper tip and the DVS-BCB bonding layer are set to be $1\,\mu\mathrm{m}$, $200\,\mu\mathrm{m}$, 400 nm and 20 nm, respectively. As the inset images show, the optical power is mostly confined in the Poly-Si/Si layer with a small part spreading into the III-V layers in the straight hybrid waveguide. With the decrease of the III-V waveguide width, the optical mode gradually converts to the fundamental TE mode in the Poly-Si/Si waveguide. The influence of the lateral misalignment and the thickness of the DVS-BCB bonding layer on the coupling efficiency are studied. Fig. 5.26(a)shows the coupling efficiency as a function of the length of the III-V taper structure for different lateral misalignment ranging from $0\,\mu$m to $1\,\mu$m.

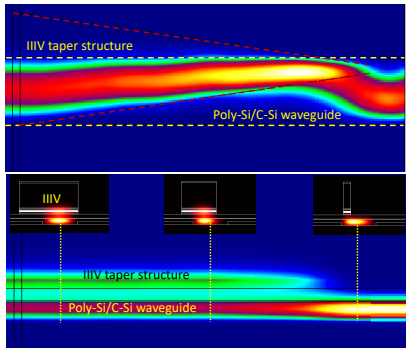
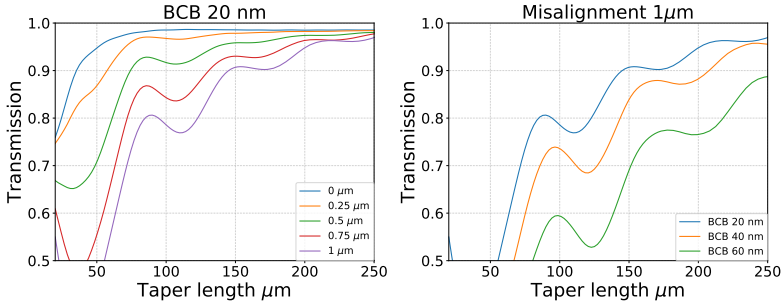


Figure 5.25: Mode propagation through the taper structure with a 1 µm lateral misalignment and a 20 nm thick DVS-BCB bonding layer.



(a) (b)

Figure 5.26: (a)Simulated coupling efficiency as a function of the taper length for the III-V/Si taper structure with (a) a 20 nm thick DVS-BCB bonding layer and different lateral misalignment and (b) a lateral misalignment of 1 µm and different thicknesses of the DVS-BCB bonding layer.

The thickness of the DVS-BCB bonding layer is set to be 20 nm. When the III-V taper is perfectly aligned to the underlying Si waveguide, the transmission rapidly increases with the increase of the taper length and saturates at 98 %. With 1 μm lateral misalignment, 95% mode coupling is achieved using a 250 μm long III-V taper structure. As shown in Fig. 5.26(b), the coupling efficiency also reaches 95% with a 40 nm thick DVS-BCB bonding layer. Based on the above discussion, a 250 μm long III-V linear taper can be used in the SOA design.

The mode coupling from the poly-Si/Si waveguide (with a DVS-BCB bonding layer and a n-InP layer on top) to the standard 450 nm wide Si waveguide is studied using Lumerical Mode solution. As illustrated in Fig. 5.27, the poly-Si/Si taper structure can be cut to three sections (Taper-1, Taper-2 and Taper-3). Because

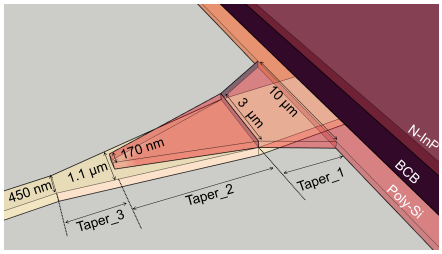


Figure 5.27: Schematic of the poly-Si/c-Si waveguide taper structure.

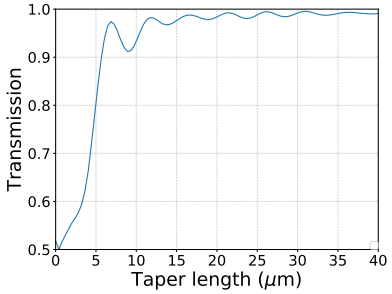


Figure 5.28: Coupling efficiency of the poly-Si/Si-Si waveguide taper structure.

of the use of 193 nm DUV lithography, a minimum feature size of 170 nm can be realized on the poly-Si layer and the poly-Si taper can be perfectly aligned to the underlying crystalline Si waveguide. In the simulation, the thickness of the n-InP layer and the DVS-BCB bonding layer are set to be 250 nm (assuming that 10 nm n-InP was removed in the release etch) and 20 nm, respectively. Other parameters can be found in the schematic layout. Because of the use of a $3\,\mu\mathrm{m}$ wide crystalline Si waveguide and the relatively low refractive index (3.169) of InP the optical mode is mostly confined in the Si layer, therefore the existance of the n-InP layer does not induce obvious loss. Fig. 5.28 shows the simulated transmission of the taper structure as a function of the length of Taper-2. The length of the Taper-1 and Taper-3 are not critical for the mode conversion. Here they were set to be $40\,\mu\mathrm{m}$ and $15\,\mu\mathrm{m}$, respectively.

5.4.5.2 Microring resonators realized on the imec iSiPP50G platform

The ring resonators are realized by a 70 nm deep dry etch in the 220 nm crystalline Si device layer. Similar to the micro-ring realized on the 400 nm photonic platform, S-bend DC couplers are used to access the ring cavity. $25\,\mu\mathrm{m}$ radius devices, which are expected to have around 4 nm FSR, are investigated at first. Fig. 5.29

shows the measured results of devices with different coupling gaps and different waveguide widths (500 nm and 600 nm). Apparently, the use of a wider waveguide leads to a higher loaded Q factor and a lower drop-port loss [33]. Given a 300 nm wide coupling gap, the loaded Q factor of the device defined with 600 nm waveguide is found to be 8.7K. It increases drastically to 250K for a device with a 800 nm wide coupling gap, but at the same time the drop-port loss increases from 0.4 dB to 5.9 dB.

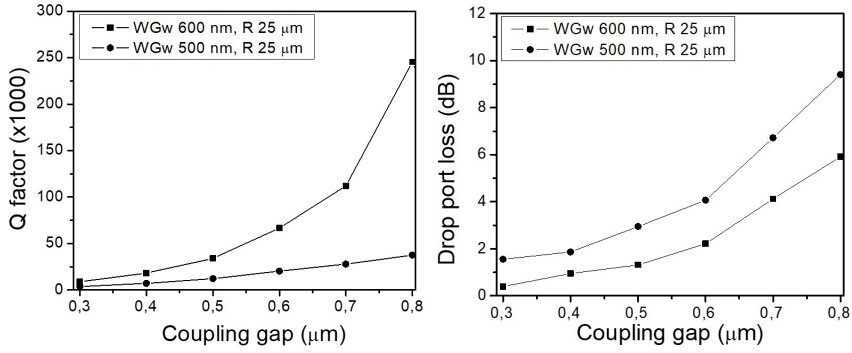


Figure 5.29: (a) Loaded Q factor and (b) drop port loss as a function of coupling gap for ring resonators with $25\,\mu\mathrm{m}$ radius.

The FSR of the $25\,\mu\mathrm{m}$ radius devices is measured to be 4.05 nm at 1550 nm, indicating a group index of 3.7765. To realize a ring-based Vernier filter with over 40 nm combined FSR, ring resonators with $27\,\mu\mathrm{m}$ radius were designed and measured. The FSR of these devices is found to be 3.77 nm at 1550 nm. Fig. 5.30 shows superimposed transmission spectra of these two ring resonators and the combined Vernier effect. As can be seen a maximum transmission is achieved when two resonance peaks perfectly overlap and the suppression over the nearest side-peaks is around 20 dB, which together with a relatively short laser cavity length allows for single-mode operation with a high side mode suppression ratio (SMSR).

5.4.5.3 Si photonic integrated coherent receiver design

Fig. 5.31 shows a GDSII layout of a polarization diverse ICR design, where a 2D grating coupler is used to realize the optical coupling from the optical fiber and the polarization demultiplexing at the same time [23]. The layout of the BDs array is redesigned to accommodate the channel spacing ($500\,\mu\mathrm{m}$) of the latest TIA array design. Two tunable lasers (one as a backup), followed by booster SOAs are used as LOs. Micro-ring resonators with a radius of $25\,\mu\mathrm{m}$ and $27\,\mu\mathrm{m}$, as discussed

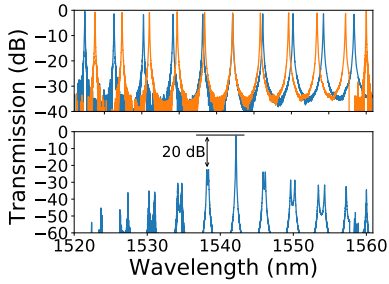


Figure 5.30: Normalized transmission spectrum of the ring resonator based vernier filter, showing a 20 dB transmission difference between the overlapped and side mode.

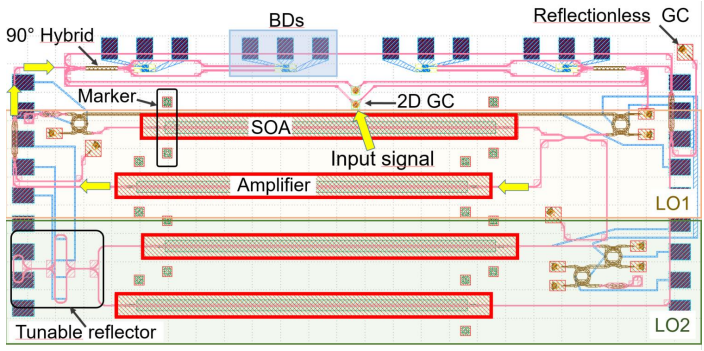


Figure 5.31: GDSII layout of a polarization division multiplexed ICR with integrated LOs.

above, are incorporated in the laser cavities to implement the Vernier effect. One of the lasers has a ring shape cavity and an external reflector (MMI-based loop mirror) for unidirectional operation, the other laser has a linear cavity formed by a tunable filter and a MMI-based loop mirror. The design of the lasers is similar to that presented in the fourth chapter. 400 nm and 500 nm coupling gaps are adopted for the ring resonators, leading to expected Q factors of 18K and 30K, respectively. The length of the laser cavities is around 2 mm. The red rectangles on Fig. 5.31 indicate the active regions where the back-end layers will be removed for the integration of III-V devices. Their dimensions are 1.33 mm $\times$ 80 μm. To reduce the external feedback to the laser cavity all the waveguides are terminated with refectionless grating couplers. The output port of the LOs is connected to 2×2 MMIs, whose output ports are then coupled to the 90° hybrids.

5.4.5.4 Transfer printing of SOAs on iSiPP50G chips

The iSiPP50G platform has around $5\,\mu m$ of back-end layer stack. As aforementioned the back-end layers in the SOA region have to be removed to enable the integration of III-V devices. In order to simplify the post-processing a 'light pass' layer was implemented over the active regions. It results in a $2\,\mu m$ thick SiO_2 layer rather than multiple layers of different materials (SiN, SiO_2, etc.) over the Si device layer. Therefore a simplified etch process can be used to expose the poly-Si layer before the μTP of SOAs.

To investigate the feasibility of the μTP of III-V SOAs in pre-defined recesses, dummy iSiPP50G chips with an array of 80×1050 μm^2 recesses were used. The $2\,\mu m$ thick SiO_2 cladding layer was removed by a combination of RIE dry etching and BHF wet etching with a $3.5\,\mu m$ thick photoresist soft mask. In order to have a uniform DVS-BCB layer in the recesses, a spray coating process rather than spin-coating was adopted in the fabrication [34]. The spray coating of DVS-BCB was performed on an EVG150 coating system at EVG.

Fig. 5.32(a) shows the source wafer with pre-fabricated C-band SOA arrays. The coupon size is 40×1000 μm^2. Three Si photonic chips that are expected to have 50 nm, 75 nm and 100 nm thick spray-coated DVS-BCB layers were used in the transfer printing test. A stamp with a 1.2 mm long post was used in the μTP process and the transfer printing was performed at room temperature. 11 out of 12 prints were successful. Fig. 5.32(b) shows a representative sample with an array of transfer-printed SOAs in the recesses. After the transfer printing process, the encapsulation photoresist is removed by RIE oxygen plasma. Then the DVS-BCB layer is cured in an oven at $270\,^{\circ}C$. A set of n-vias are defined to expose the n-contact metal by RIE dry etching. The process is finished by a definition of metal contact pads via a lift-off process. Fig. 5.33 shows a microscope image of the fabricated devices. The pre-defined recess, SOA and alignment markers are indicated in Fig. 5.32(c). As shown in a FIB image close to the III-V taper tip(Fig. 5.32(d)), a lateral misalignment of 230 nm is obtained. The BCB bonding layer is very thin and hardly visible in the SEM image.

The laser characterization was carried out on a temperature-controlled stage (with a Peltier element). Fig. 5.34 depicts a schematic layout of the measurement setup used for the optical gain measurement. A Keithley 2401 current source was used to bias the device through three DC probes with two probes landing on the n-contact pads. In the characterization, the optical power was collected by a standard single mode fiber through a GC and was split by a -20 dB tap with the -20 dB branch feeding an HP power meter and the other one connected to an optical spectrum analyzer. The optical power coupled to the waveguide and the on chip gain of the SOA was obtained by calibrating out the loss introduced by the GC and the fiber-optics.

The SOAs exhibit a differential resistance of $15\,\Omega$ at 90 mA. In the optical gain

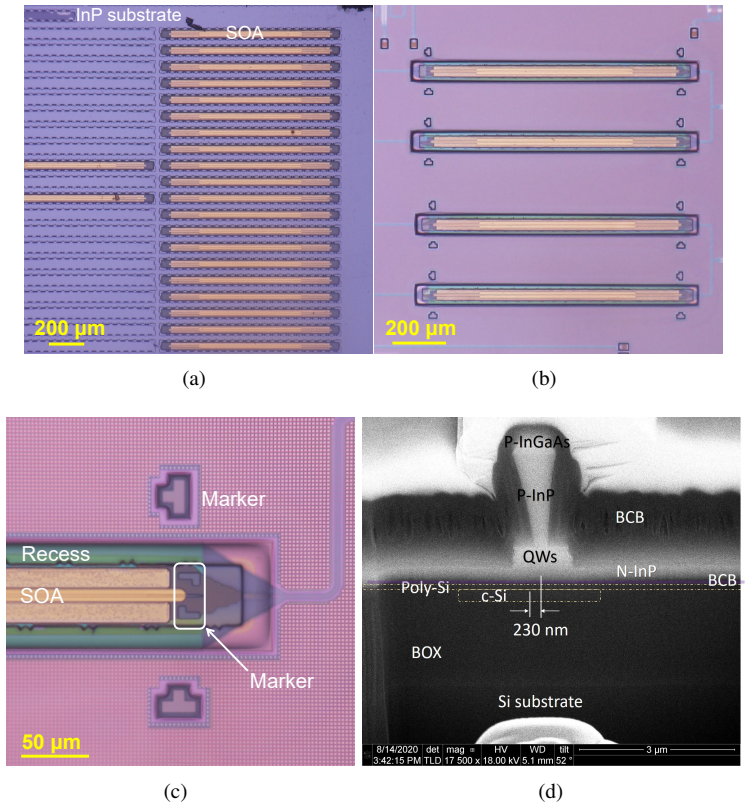


Figure 5.32: (a) Microscope image of the source wafer with pre-fabricated SOA array. (b) PICs with an array of transfer-printed SOAs.(c) Zoom-in image of a transfer-printed SOA in the recess.(d) An SEM image of the III-V taper structure close to the taper tip shows a misalignment of 230 nm.

measurement, the wavelength of the laser is fixed at 1560 nm which is around the gain peak. Due to the parasitic reflections from the grating couplers, spurs become obvious around the gain peak at bias currents over 100 mA and the devices start lasing at higher currents. Therefore the bias current of the amplifiers is swept from 15 mA to 95 mA in the gain measurement. The on-chip gain is obtained by comparing the waveguide-coupled output and the input powers and different on-chip input powers were investigated. As shown in Fig. 5.35(b), the on-chip gain increases with the bias current and saturates to 10 dB at 90 mA. It shows only a slight reduction of the on-chip gain with the increase of input power, which is due to a low optical confinement factor in the quantum well layers because of the ultra thin BCB bonding layer. Fig. 5.35 shows a set of measured gain spectra at

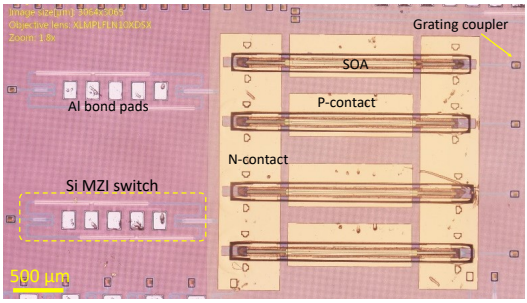


Figure 5.33: Microscope image of a photonic chip with an array of transfer-printed SOAs.

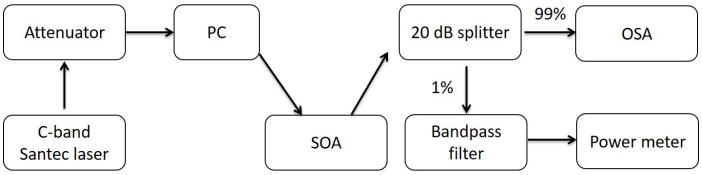


Figure 5.34: Schematic layout of the characterization setup used to characterize the transfer-printed SOAs. PC: polarization controller, OSA: optical spectrum analyzer.

different bias currents. In the measurement, the wavelength of the tunable laser is swept from 1530 nm to 1580 nm while the on-chip input power is kept at -20 dBm. The 3-dB gain bandwidth of the SOA is found to be 33 nm at 100 mA.

5.5 Conclusion

In this chapter, we reported the progress made towards the realization of fully integrated Si photonic ICRs. Two approaches based on different photonic platforms (the 400 nm passive platform and the iSiPP25G/50G platform) were investigated. In the first case, Si PICs defined by e-beam lithography and RIE dry etching were adopted for the ICR demonstration. The ICR consists of two LOs (with one as a reserve), a 90° hybrid and a pair of grating assisted III-V-on-Si BDs. The fabricated 90° hybrid show less than $\pm 5^\circ$ phase error over the entire C-band. Both the LOs and PDs were integrated via μTP. The grating-assisted PDs have a bandwidth of 16 GHz at -3 V. The fabricated lasers exhibited 40 nm wavelength tuning but with a high threshold current (130 mA) due to a high waveguide loss. Due to an uncertain waveguide loss, we were not able to estimate the waveguide coupled power. Although this demonstration did not yield functional ICRs, it at least verified the feasibility of the realization of complex photonic circuits by co-integration

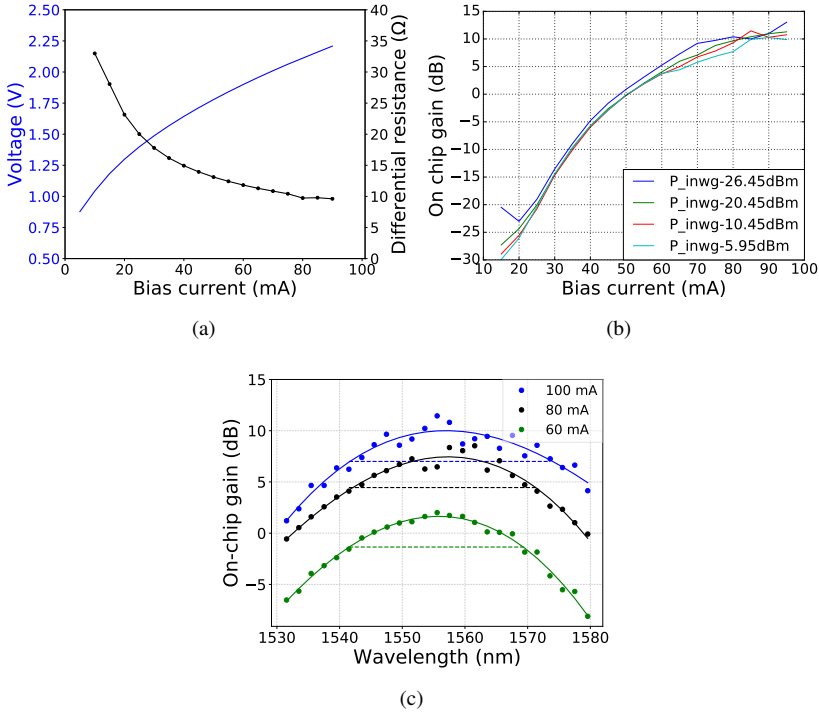


Figure 5.35: (a) V-I curve and differential resistance. (b) Variation of on-chip gain with different waveguide coupled input power at 1560 nm (around gain peak). (c) On-chip gain spectra for different bias currents.

of different pre-fabricated III-V devices via μTP.

In the second case, we aimed at realizing Si photonic ICRs on the imec iSiPP25G and iSiPP 50G photonic platform by taking advantage of the high-speed Ge PDs. In the first stage, an ultra-compact ICR ($0.3 \times 0.7\,\mathrm{mm}^2$) integrated with a 0.13-μm SiGe BiCMOS TIA array was demonstrated. Operation below FEC threshold for QPSK and 16-QAM at 28 Gbaud was obtained. Following this success we focused on the realization of fully integrated ICRs with integrated III-V-on-Si LO on the imec iSiPP50G photonic platform. An alignment tolerant taper structure was investigated, showing over 95% mode coupling with a $1\,\mu\mathrm{m}$ lateral misalignment. In the first test, III-V SOAs were successfully transfer printed in the pre-defined recesses with 100% printing yield. SOAs with 10 dB waveguide-to-waveguide gain were demonstrated paving the way for the realization of fully integrated ICRs and other high-speed photonic integrated circuits.

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6 Conclusion and Perspectives

6.1 Conclusions

Photonic integration is playing an increasingly important role in today's communications industry in coping with the ever-growing capacity demands. The intimate integration of a large number of optical components on a chip not only shrinks the footprint of photonic systems, e.g. optical transceivers, but also, and more importantly, leads to a lower power consumption and reduced cost. Silicon photonics based on the silicon-on-insulator (SOI) platform shows unique advantages over other platforms (planar lightwave circuits, InP-based photonic integrated circuits, etc.), such as high refractive index contrast and CMOS compatibility. Furthermore the existence of Si/Ge based active components (Si modulators, Ge photodiodes and Ge EAMs) enables the realization of complex and powerful PICs.

Despite the rapid developments over the last two decades, the absence of a low-cost integrated light source remains an obstacle for the proliferation of this technology. To address this issue, tremendous effort has been devoted in the past decades to integrate III-V light sources on a Si PIC. In the first chapter we discussed the existing III-V-on-Si integration approaches and presented a novel technology, micro-transfer-printing, which we adopted for the realization of III-V-on-Si integrated circuits due to its capability of manipulating micro-scale films/devices in a massive parallel manner and the fact that it allows for high-accuracy alignment. To explore the potential that μTP has, various III-V-on-Si integrated devices and circuits were demonstrated in this thesis, including III-V-on-Si integrated DFBs, a

four channel FTTH transceiver array based on an array of transfer-printed O-band PDs, widely tunable narrow linewidth lasers and coherent receivers. To enable the μTP based integration, dedicated III-V epitaxial materials were designed and used for different cases. To obtain a reliable bonding of III-V to the SOI substrate a thin layer of DVS-BCB was used as the adhesive bonding agent in the μTP process.

Electrically-pumped C-band III-V-on-Si DFB lasers based on the μTP of III-V material coupons are demonstrated in Chapter 2. A III-V epitaxial layer stack was designed to enable the transfer-printing-based laser integration. Design, fabrication and release of the dense coupon arrays were described in detail. A pyramidal shape bottom surface was found on the released coupons due to a long release etch (around 8 hours). The printing of these released coupons on dummy SOI substrates with a thin layer of DVS-BCB adhesive was carried out and showed close to 100% printing yield and a less than 20 nm thick resulting DVS-BCB bonding layer, which is sufficiently thin for an efficient mode coupling from the III-V layer to the Si waveguide. The post-processing of the printed coupons was developed and optimized in two fabrication cycles. With a well defined III-V taper structure in the second run, the resulting device showed single mode operation with over 40 dB SMSR and 2.2 mW single side waveguide coupled power at 70 mA. Because of the use of micro-scale III-V material coupons this approach shows a significant improvement of the efficient use of expensive III-V material. Nevertheless complicated fabrication processes are required for the definition of III-V devices on the target substrate, making this approach somewhat less than perfect.

To further exploit the potential that the μTP technique has, we proposed a more advanced strategy for the realization of III-V-on-Si PICs via transfer printing. Here, instead of material coupons, III-V devices pre-fabricated on the source III-V epitaxial wafer were used so that a simple post-processing which just consists of a passivation and collective wiring of the devices is needed to finalise the fabrication. In this way, the cost of the resulting III-V-on-Si PICs can be significantly reduced. Following this concept, we demonstrated two different transceivers for point-to-point FTTH networks on the central office side in chapter 3. The PICs used for this demonstration were realized on the imec iSiPP25G platform, consisting of an array of C-band ring modulators and a one by four splitter. O-band PDs with deposited metal contacts were firstly defined on a III-V wafer in dense arrays and then transfer-printed onto grating couplers on an iSiPP50G Si PIC for the realization of an upstream O-band receiver. Fabrication and release of the PD arrays on the InP source wafer was presented in detail. The transfer printing of the O-band PDs was carried out in an automatic mode where these PDs were automatically aligned onto grating couplers through a pattern recognition process.The p-metal contact and grating coupler itself were used as alignment markers in the transfer printing. Although the use of small Si photonic chips induced issues, especially in the spin coating of DVS-BCB and photoresist, 100% printing yield was

achieved. These integrated PDs exhibited a polarization-independent responsivity of $0.39-0.49$ A/W in the O-band. The fabricated transceiver array was successfully demonstrated at a bit rate of 12.5 Gbit/s. In parallel, we demonstrated the co-integration of DFB lasers and O-band PDs on a passive Si PIC for the realization of single channel FTTH transceivers, where the DFB lasers were first integrated through the aforementioned DFB integration approach, followed by the transfer printing of pre-fabricated O-band PDs on the grating couplers. Because of the use of a big photonic chip, uniform DVS-BCB layers and resist layers were obtained via spin-coating that significantly facilitated the fabrication. Despite a lower sensitivity ($\sim$ 0.3 A/W) of the integrated TPD for the O-band signal and a degraded SMSR of the C-band DFB laser, the transceiver was demonstrated at 12.5 Gbit/s. Because of the use of a DFB laser as downstream transmitter, no external light source is needed and the transceiver is more robust. More importantly, such a intimate co-integration of non-compatible components enabled by transfer printing allows for the realization of complex PICs with reduced footprint and significantly reduced cost.

These demonstrations showcase the realization of III-V-on-Si PICs via the transfer printing of pre-fabricated III-V devices. Following these successes, we demonstrated III-V-on-Si narrow linewidth and widely tunabe lasers in Chapter 4, through the same approach. To shorten the release etch and to obtain a flat and smooth bottom surface, a modified III-V epitaxial layer stack with a 500 nm thick AlInAs release layer was used in this work. A few essential components on the imec 400 nm photonic platform, including MMI couplers, ring resonators and DBR reflectors, were investigated. With these components, we first designed and fabricated a group of widely tunable lasers via DVS-BCB adhesive bonding to verify the feasibility of the use of a Vernier filter for single mode operation and a wide wavelength tuning. A set of micro-heaters were integrated for the wavelength tuning. All the fabricated lasers exhibited single mode operation and around 40 nm tuning range. The waveguide coupled output power and the linewidth is above 0 dBm and below 1 MHz respectively over the entire tuning range. Moreover by adding an external reflector the laser showed unidirectional operation. After validating the widely tunable laser design using a micro-ring based Vernier filter, we demonstrated a widely tunable laser by transfer printing pre-fabricated SOAs. Due to a poor adhesion of the micro-heater to the DVS-BCB spacer layer and thus limited thermal dissipation, continuous tuning over the entire tuning range was not achieved. A III-V/Si hybrid waveguide with an alignment tolerant taper structure was designed to accommodate the alignment accuracy ($\pm 1.5\ \mu\mathrm{m}$, 3σ) that μTP can obtain. A linear laser cavity was adopted in this demonstration to avoid the mode competition between the two counter propagating modes. The fabrication and the release of the SOA arrays on the source wafer as well as the post transfer printing processes were presented in detail in this chapter. The fabricated laser has a se-

ries resistance and a room temperature threshold of $15\,\Omega$ and 70 mA, respectively, which are comparable to the tunable lasers fabricated via die-to-wafer bonding. Along with this, a continuous tuning over 48 nm in the 1560 nm wavelength range was achieved due to the use of a $1\,\mu\mathrm{m}$ thick SiO_2 spacer layer. The maximum waveguide-coupled output power was measured to be 5.2 dBm at the center of the gain spectrum and the linewidth is minimal (300 kHz extracted by Voigt fitting) at the same wavelength. Although there is still room to improve the performance of these widely tunable lasers, in terms of output power, linewidth, tuning range, etc., this demonstration verifies the feasibility of the integration of III-V-on-Si lasers through transfer printing of pre-fabricated SOAs. This fabrication process flow can also be used for the realization of other III-V-on-Si integrated devices (e.g. amplifiers, modulators and lasers in other wavelength ranges).

In Chapter 5, we discussed two approaches for the realization of coherent receivers with integrated LO. They are based on a silicon on insulator (SOI) substrate with 400 nm Si device layer and the imec iSiPP25/50G platform, respectively. In the first case, both widely tunable lasers and C-band PDs were integrated by transfer printing pre-fabricated III-V devices. The overall fabrication went very smoothly, but a high and inconsistent waveguide loss, attributed to the imperfect e-beam lithography process, was found in the characterization. The fabricated PDs and lasers were found to be working independently, but difficulties were faced in the characterization of these devices and also the coherent receiver due to the waveguide loss issue. This problem can be overcome by adopting PICs patterned using deep UV lithography or improved e-beam lithography.

The other approach we proposed is based on the co-integration of a III-V-on-Si LO with Ge PDs on the imec 25G/50G platform. First we demonstrated a coherent receiver (integrated with a TIA array) at 28 Gbaud/s 16QAM operation, where an external narrow linewidth laser was used as LO. In the second step, we designed a coherent receiver with modified layout and integrated LO using the same building blocks (90° hybrid and Ge PDs). The integration of the LO on the iSiPP50G platform is discussed. To enable the integration of III-V-on-Si lasers, the back-end layer stack has to be removed to expose the Si device layer. Tests on dummy iSiPP50G chips were first carried out and we already managed to transfer print pre-fabricated SOAs in pre-defined recesses. With these established process flows and known causes of the issues faced in the fabrication and characterization, it is surely possible to realize complex PICs such as these ICRs through μTP.

6.2 Perspectives

In this thesis we explored the capabilities that μTP has in the field of III-V-on-Si PICs through a series of demonstrations of III-V-on-Si integrated devices/circuits. Essential aspects including the design of the III-V layer stacks, pre-fabrication and

release of III-V devices on the source wafer, transfer printing of III-V material coupons/devices, post transfer printing processes, etc. were covered in this work. These demonstrations showcase the enormous potential that μTP has for the integration of III-V devices on a Si PIC with high flexibility. Nevertheless, substantial effort has to be devoted in the future to improve the performance of these devices/-circuits to achieve commercial success. On the other hand, the potential that μTP has still waits to be further exploited.

6.2.1 Transfer printed DFB lasers

Although the use of III-V material coupons results in a significant reduction of the waste of expensive III-V materials, the required complicated post-transfer-printing processes make this integration strategy less attractive, especially for large volume production. To simplify the fabrication and to reduce the cost of resulting DFB lasers, pre-fabricated III-V devices should be used. Therefore a DFB laser that is able to tolerate ± 1.5 μm misalignment has to be designed (because of the transfer-printing alignment tolerance). This is a challenging task as such a large misalignment can easily excite high order modes in the laser cavity, resulting a multimode operation and/or low output power. A possible route is by increasing the thickness of the Si waveguide or by using a very shallow etched DFB grating. In this way the mode is more confined in the Si waveguide so that it is less sensitive to the lateral misalignment. Such devices were recently demonstrated by B. Haq, *et al.* [1].

6.2.2 FTTH transceiver

12.5Gbit/s NRZ operation was successfully demonstrated on the imec iSiPP 25G platform, nevertheless a high average power was required for error free operation for the O-band upstream receiver, due to the lack of integrated transimpedance amplifier. Therefore it is necessary to co-integrate a TIA array with this transceiver. Grating couplers with less insertion loss should be used and the p-InGaAs layer on the integrated PDs should be removed to reduce the overall insertion loss for C-band signals. The performance of the O-band PDs in terms of responsivity, bandwidth and dark current, while sufficient for 10 Gbit/s operation, can be further improved. The responsivity for the O-band signal can be improved by using a thicker absorbing layer, while care has to be taken as the bandwidth could be reduced due to an increased transit time of photogenerated carriers. Given the III-V layer stack, the bandwidth can be improved by optimizing the dimensions of the PD mesa to reduce the RC time constant. The n and p type contact metal depositions should also be investigated to achieve a low series resistance. The cause for the high dark current is not clear, but probably not related to the quality and/or the structure of the III-V layer stack. In the case of the fully integrated transceiver, again the DFB laser can be integrated through the transfer printing of

pre-fabricated III-V taper structures, preferable with a compact footprint for a high bandwidth.

6.2.3 Micro-transfer-printed III-V-on-Si widely tunable and narrow linewidth lasers

Widely tunable narrow linewidth lasers are essential building blocks in integrated transceivers, especially in integrated coherent transceivers. To enable the transfer-printing-based integration of III-V-on-Si lasers, a III-V/Si taper structure with a lateral misalignment tolerance of ± 1 µm was proposed. The intrinsic linewidth of the fabricated laser was found to be less than 1.5 MHz over the entire tuning range (with 300 kHz close to the gain peak). Apparently there is still considerable room for improvement, as much narrower linewidth has been demonstrated using the same type of tunable lasers that are fabricated via die-to-wafer bonding. Effort should be first put in the optimization of the III-V taper structure, e.g. assess and decrease the coupling losses from the III-V to the silicon waveguide, to further reduce the laser linewidth.

6.2.4 Co-integration of multiple components for the realization of complex PICs

In this work we developed and perfected an entire fabrication process flow for the co-integration of multiple III-V components on Si photonic wafers. With this established process flow one can realize complex III-V-on-Si PICs with considerable flexibility. Also, the transfer printing of pre-defined III-V SOAs in recesses on the imec iSIPP50G platform has been demonstrated. This lays the foundation for the realization of complex PICs combining III-V functionality with iSIPP50G circuits. Moreover, devices implemented in other material systems that can be released from the substrate on which they are fabricated can be added to the PICs via μTP. This creates opportunities for efficiently integrating other optical functions such as optical isolators, electro-optic modulators and even electronic driver circuits (when realized on an SOI substrate) on the Si photonic platform. It can also enable more complex PICs in non-telecom wavelength ranges such as the visible (VIS), near-infrared (NIR) and the mid-infrared (MIR).

6.2.5 Micro-transfer printing

As already discussed in Chapter 1, the transfer printing technique is very well suited to massively parallel integration of devices from a source wafer. This feature has not yet been exploited in the demonstrations presented in this thesis and should be studied and exploited in the follow-up work. Besides this, effort should also be

put to improve the alignment accuracy, as this will significantly relax the pressure in the design of Si PICs and source devices of interest.

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