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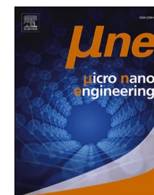

Research paper

Screening of 193i and EUV lithography process options for STT-MRAM orthogonal array MTJ pillars

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A B S T R A C T

Spin-transfer torque magnetic random-access memory (STT-MRAM) is considered as the most promising candidate to replace the complementary metal-oxide-semiconductor (CMOS) based memories that are dominating the market in the last few decades. What makes STT-MRAM superior to other memories is the high read and write speeds, non-volatility, good cycling endurance and near-zero leakage. Moreover, with the perpendicular device topology and the single transistor cell configuration, it becomes a very promising candidate for further device scaling which is essential to increase the memory densities. This paper focuses on the experiments performed using different lithography approaches in order to explore the smallest printable pitches for orthogonal array magnetic tunnel junction (MTJ) pillars, which are the main components of the STT-MRAM. Considering the high impact of the MTJ patterning process on the robustness of the memory device, several post-litho performance parameters such as wafer critical dimension uniformity (WCDU), local critical dimension uniformity (LCDU) and pillar circularity have also been measured and compared.

1. Introduction

The increased demand on more data storage requires new memory technologies with low manufacturing cost and good device performance characteristics such as high read/write speeds, endurance and non-volatility. The memory market has been dominated by CMOS memories such as flash random-access memory (RAM), static random-access memory (SRAM) and embedded dynamic random-access memory (e-DRAM), in the last few decades. On the other hand, the scaling challenges of these CMOS devices together with the increased demand for higher memory density and performance, have increased the necessity for investigation of new patterning technologies while maintaining cost margins.

STT-MRAM is a solid-state magnetic memory and it is considered to be one of the most promising candidates, primarily because of its high reading and writing speeds. Fig. 1 shows where STT-MRAM stands amongst the various memory classes.

STT-MRAM is not only a non-volatile memory device with very good cycling endurance and near-zero leakage, but also its read speed is comparable to SRAM [1]. Moreover, the single-transistor memory cell configuration of the STT-MRAM is a huge advantage to enable higher memory densities. The manufacturing cost for STT-MRAM is also low compared to other memory technologies. In a standard STT-MRAM manufacturing flow, only three additional masks are required on top of the CMOS circuitry; which are the bottom electrode, MTJ cell and the top electrode. These masks are typically used for perpendicular device manufacturing [2].

MTJ is the main component of STT-MRAM. MTJ is a sub-100 nm magnetic element consisting of two ferromagnetic layers separated by a thin insulating layer, which is typically MgO. The information is stored in the magnetic state of one of the magnetic layers which is called the free layer. The second magnetic layer, reference layer, provides a reference frame required for reading and writing. STT-MRAM functionality is driven by two phenomena: 1) the tunneling magnetoresistance (TMR) effect for reading and 2) the spin-transfer torque (STT) effect for writing [3]. The MTJ stack and the device configuration is shown in Fig. 2.

The resistance of the MTJ, which is known as TMR, depends on the relative orientation of the magnetic layers. The resistance in the anti-parallel state (known as HRS, high resistance state) can be several times larger than the one in the parallel state (known as LRS, low resistance state). The TMR enables the magnetic state of the free layer to be sensed and the stored information can be read [3]. As TMR is a function of the resistance difference between the two different magnetic states, the variations on the resistance of the MTJ cell will degrade the read performance of the device. The dominant source of the resistance variation is the LCDU of the patterned MTJ layer. Therefore, ensuring a good LCDU is crucial in STT-MRAM manufacturing [2].

The STT effect, on the other hand, creates a torque on the magnetization of the free layer by enabling the electrons flowing through the MTJ to transfer spin angular momentum between the magnetic layers. This torque enables the magnetic state of the free layer to be changed if it is sufficiently strong and the information can be written [3].

Increased memory density is one of the biggest demands of the market.

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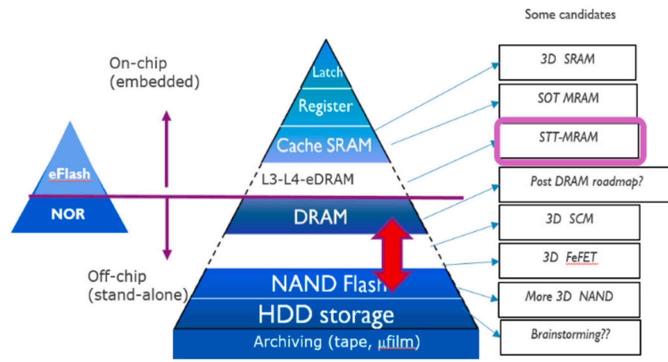

Fig. 1. Classification of memory devices [2].

For a certain device topology, this can be achieved by scaling down the feature and/or pitch size. On the other hand, the process variations relative to the nominal process parameters deteriorate as feature sizes scale down. This has a huge impact for the device robustness; thus, yield.

Patterning MTJ pillars is one of the most critical steps in the STT-MRAM manufacturing flow. Besides the LCDU impact on the TMR performance mentioned before, WCDU and the circularities of the MTJ pillars are the other performance criteria for robust STT-MRAM manufacturing. In this paper, we focus on different lithography approaches to explore the smallest printable pitches for orthogonal array MTJ pillars with reasonable LCDU, WCDU and pillar circularity performance.

This paper is organized as follows. In Section 1, the STT-MRAM device has been introduced and the motivation of the study has been given. Section 2 reviews the experimental plan while section 3 focuses on the details of the metrology used during the process screening. The experimental results obtained are shown in section 4. Section 5 compares the screened approaches in terms of the manufacturing cost and alignment/overlay challenges. Finally, section 6 gives the conclusions.

2. Experimental plan

Four different lithography approaches have been tested by screening different photoresists and illumination sources for each approach. Two of these approaches are based on single exposure ArF immersion litho with two different mask and photoresist tonalities. The third approach is a double exposure ArF immersion litho where two perpendicular line/space (L/S) structures are exposed with single resist coating to achieve pillars. The last approach is a single exposure EUV lithography.

In total, 5 different photoresist materials have been screened together with 7 different illumination sources in total. In order to emulate the hardmask (HM) stack used in MTJ patterning, the Si wafers exposed with immersion lithography have been coated with 65 nm/28 nm – spin-on-carbon/spin-on-glass (SOC/SOG) stack; while, the EUV exposures were performed on 65 nm/10 nm – SOC/SOG stack. SOC/SOG materials and thicknesses coated during this study are identical to the ones used at standard MTJ patterning at imec in order to preserve the reflectivity of the full stack exposures. The stacks used for exposures are shown in Fig. 3 below.

Table 1 below shows the experimental details of this study. LF stands for light-field and DF for dark-field. NTD PR, on the other hand, is negative tone development photoresist, while PTD PR is positive tone development photoresist. IL1, IL6 and IL7 are flexray sources dedicated to the imec STT-MRAM process or the test masks used. IL2 is a C-Quad 20° source with 1.35 NA and 0.97/0.82 σ_{out}/σ_{in} values with x/y polarization. The same NA, polarization and σsettings apply to IL3 Quasar 20° source. IL4 and IL5 are the combination of 40× and 40Y Dipole sources used for double exposure. They are both x/y polarized sources with 0.98/0.80 σ_{out}/σ_{in} for IL4 and 0.98/0.84 σ_{out}/σ_{in} for IL5. IL5 has 1.35 NA compared to 1.2 of IL4.

3. Metrology

The CD measurements have been performed using CG6300 CDSEM from Hitachi®. Standard on-tool bi-directional ellipse measurements for pillars have been done, using imec best-known methods (BKMs) on 45 dies for uniformly exposed wafers and on each die for the focus exposure matrix (FEM) wafers. To obtain the wafer mean CD and WCDU, 45 different CD values of each die (which is obtained by averaging the CD values of all pillars in a certain image) are used. The mean value of these CD values are reported as wafer mean CD and the 3σ of these CD values are reported as WCDU.

The pillar circularity performance was also measured. In order to do so, X/Y ratios of the horizontal and vertical CD measurements of all the pillars are calculated and averaged. The DOF (depth-of-focus) values reported in the paper are obtained from the process window analysis of the FEM wafers for the given EL (exposure latitude) values.

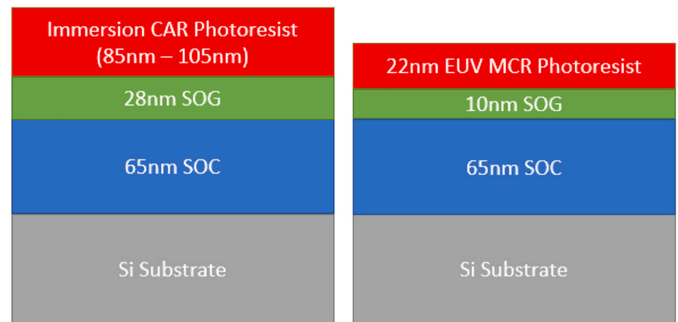

Fig. 3. HM stacks used for experiments.

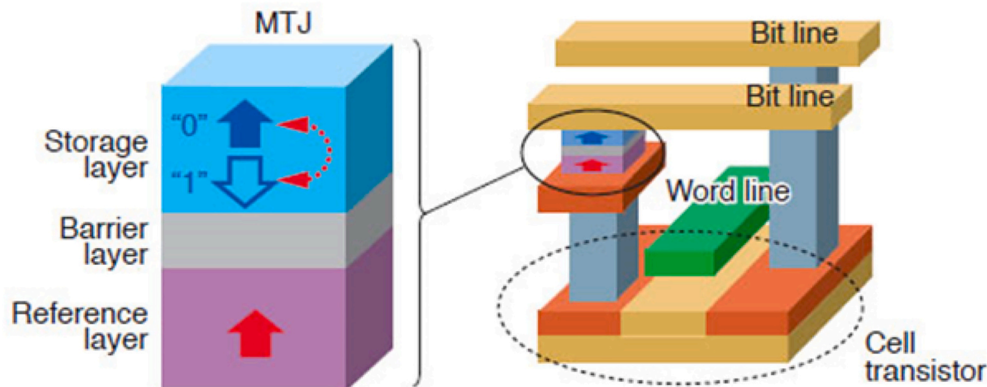

Fig. 2. STT-MRAM memory device and the MTJ stack [4].

Table 1
Experimental details of the four different approaches.

Approach	Immersion 1	Immersion 2	Immersion 3	EUV
Tool	NXT:1950i NXT:2000i	NXT:1950i NXT:2000i	NXT:1950i NXT:2000i	NXE:3400
Exposure	Single	Single	Double	Single
Polarity	DF Mask NTD PR	LF Mask PTD PR	LF Mask PTD PR	DF Mask NTD PR
HM Stack	SOC/SOG 65 nm/ 28 nm	SOC/SOG 65 nm/ 28 nm	SOC/SOG 65 nm/ 28 nm	SOC/SOG 65 nm/ 10 nm
Photoresists	PR1 PR2	PR3 PR4	PR3 PR4	PR5
Illumination Sources	IL1 IL2 IL3	IL1 IL2 IL3	IL4 IL5	IL6 IL7

Finally, LCDU was calculated by measuring 4 or 5 different locations (depending on the design availability of the test masks) with the same CD and pitch combinations. 40 to 100 pillars per location (depending on the pitch size and the field of view of the imec standard metrology recipes) were measured. This makes the number of pillars measured per die at least 160 and maximum 400. To obtain the LCDU, the 3σ values of these 160 to 400 pillars were calculated for each die and the average 3σ values of 45 different dies are used to define the LCDU of a particular wafer. In total, 7200 to 18,000 pillar measurements are used to define the LCDU. Fig. 4 shows the top-down view SEM image for a certain pillar array, Fig. 5 illustrates the LCDU measurement methodology used and Fig. 6 shows the sampling data for 45 dies and 5 image locations per die.

4. Iv. Results

In order to explore the smallest pitch with good process performance, four different litho approaches were tested by screening different photoresists and illumination sources.

4.1. Immersion 1 approach

In this approach, single exposures of a DF mask (contact hole mask) are performed with 6 different sets of process parameters. The process splits are based on the selection of 2 different NTD (to enable pillar printing for a CH mask) photoresists and 3 different illumination sources. Test structures within 82 nm to 94 nm pitch size combined with several design CD values have been used for screening.

The experiments performed using PR1 could not achieve any pillars for the pitch sizes below 90 nm and the smallest pitch with a reasonable process window was 96 nm. Since that particular photoresist, regardless of the illumination source used, has performed worse compared to the PR2, uniform exposures of PR1 has not been performed. The same applies to the process combination of PR2 and IL2, where no process window could be obtained for 94 nm pitch pillars. PR2 exposures combined with IL1 and IL3, on the other hand, have given promising results compared to the other approaches. A reasonable litho process (good process window with no collapsing pillars) could be obtained for 92 nm pitch using the PR2-IL1 process and for 86 nm pitch using the PR2-IL3 process.

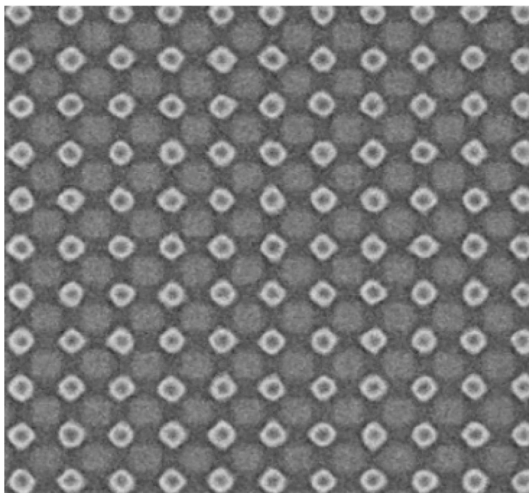

Fig. 4. The top-down view SEM image of pillars.

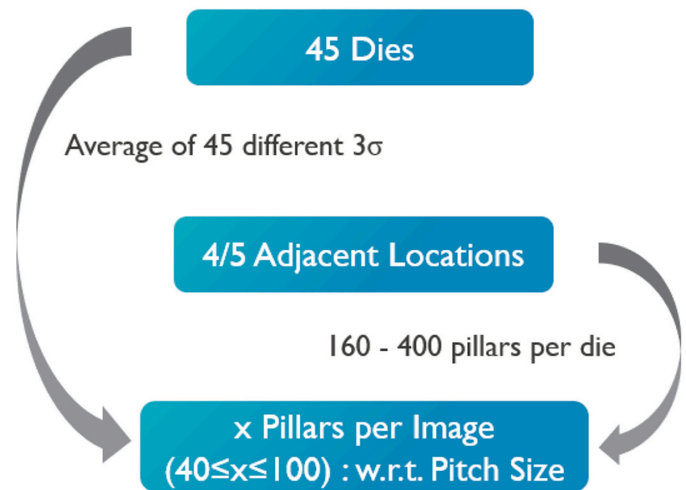

Fig. 5. LCDU measurement methodology used.

Fig. 7 shows the CD based process window (with 10% allowable variation) for PR2-IL1 for 46 nm pillars at 92 nm pitch while Fig. 8 shows the process window for PR2-IL3 for 43 nm pillars at 86 nm pitch. Both processes have a DOF (depth of focus) around 140 nm for a similar EL.

Table 2 shows the results obtained from the uniform wafer exposures. Two wafers for each experiment have been exposed and the results are averaged.

As a result, the collapse-free smallest pitch that could be printed with Immersion 1 approach is 86 nm. The required dose to print 43 nm pillar CD was slightly below 50 mJ, which is a reasonable dose value for the process throughput. The wafer CDU, LCDU and the pillar circularity ratios reported in Table 2 are also very promising for a robust MTJ patterning process at 86 nm.

4.2. Immersion 2 approach

In this approach, single exposures of a LF mask (pillar mask) are performed with 6 different sets of process parameters. The process splits are based on the selection of 2 different PTD photoresists and 3 different illumination sources. Test structures within 80 nm to 86 nm pitch size combined with several design CD values have been used for screening. The reason for focusing on 86 nm (which was the smallest pitch obtained with Immersion 1 approach) and smaller pitch values is the use of a LF mask instead of DF mask. LF masks are expected to have better image contrast; hence, better resolution [5].

The exposures performed using IL1 and IL2 sources could not print any pillars for pitch sizes below 86 nm. The smallest pitch with a reasonable process window was 90 nm. The IL3, on the other hand, gave good results for both photoresists PR3 and PR4. A reasonable litho process could be obtained for 82 nm pitch using the PR3-IL3 process and for 80 nm pitch using the PR4-IL3 process. Fig. 9 shows the CD based process window for PR3-IL3 for 41 nm pillars at 82 nm pitch while

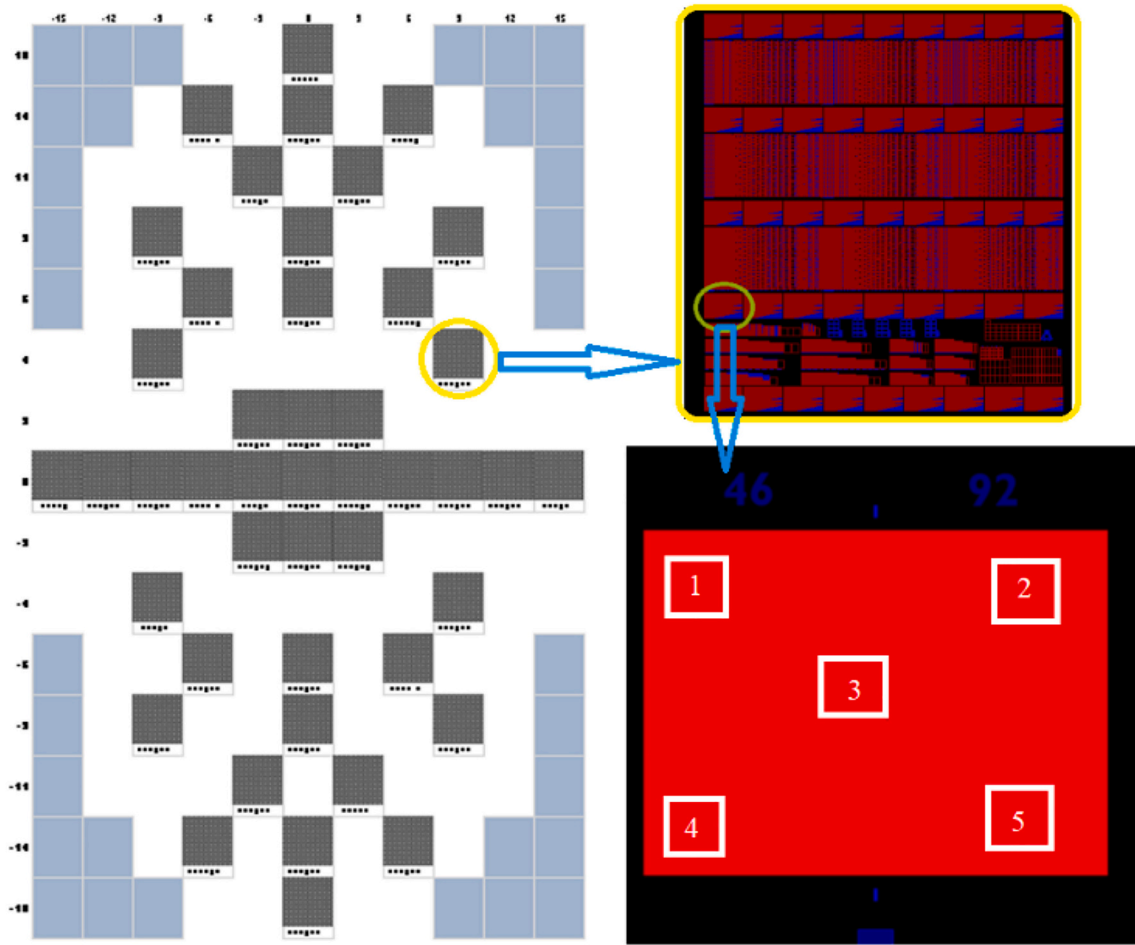

Fig. 6. Sampling for LCDU measurements.

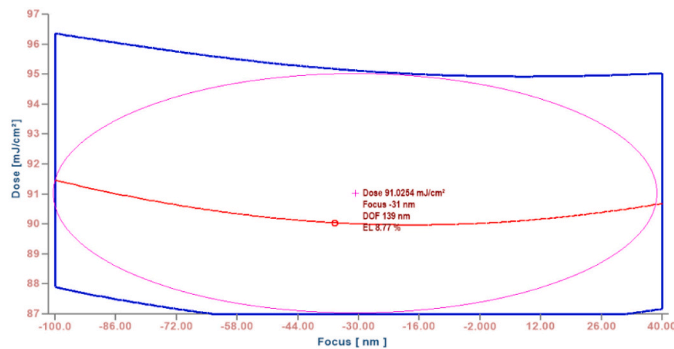

Fig. 7. Process window for PR2-IL1 at 92 nm pitch.

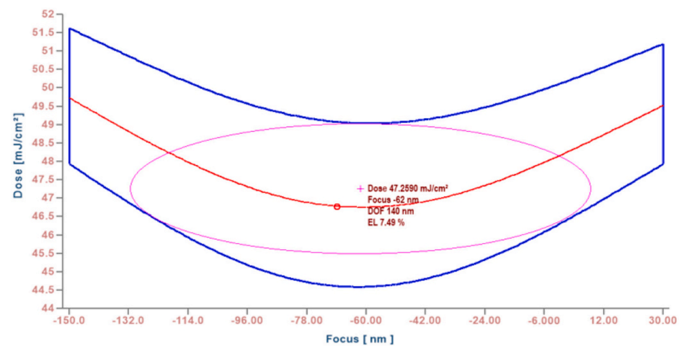

Fig. 8. Process window for PR2-IL3 at 86 nm pitch.

Fig. 10 shows the process window for PR4-IL3 for 40 nm pillars at 80 nm pitch. Both litho processes have a good process window which is 192 nm DOF at 12% EL for PR3-IL3 and 160 nm DOF at 10% EL for PR4-IL3.

Table 3 shows the results obtained from the uniform wafer exposures. Similar to the Immersion 1 approach tests, two wafers for each experiment were exposed and the results averaged. As a result, the collapse-free smallest pitch that could be printed with Immersion 2 approach is 80 nm. The required dose to print 40 nm pillar CD was 18.5 mJ (slightly more dose is needed to fine-tune the CD value reported), which was a good energy value for process throughput. The wafer CDU, LCDU and the pillar circularity ratios reported in Table 3 are also very promising for a robust MTJ patterning process at 80 nm.

Table 2
Litho performance for Immersion 1 approach with PR2-IL1 and PR2-IL3 process options.

Process	Pitch	Mean CD	Dose	WCDU	LCDU	X/Y
PR2-IL1	92 nm	46.37 nm	90.5 mJ	1.58 nm	5.37 nm	1.02
PR2-IL3	86 nm	43.11 nm	49.7 mJ	1.36 nm	4.21 nm	1.02

4.3. Immersion 3 approach

In this approach, double exposure of two perpendicular L/S masks were performed with 4 different sets of process parameters. The process

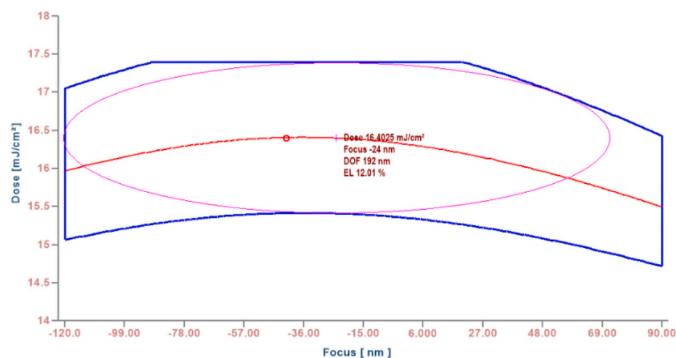

Fig. 9. Process window for PR3-IL3 at 82 nm pitch.

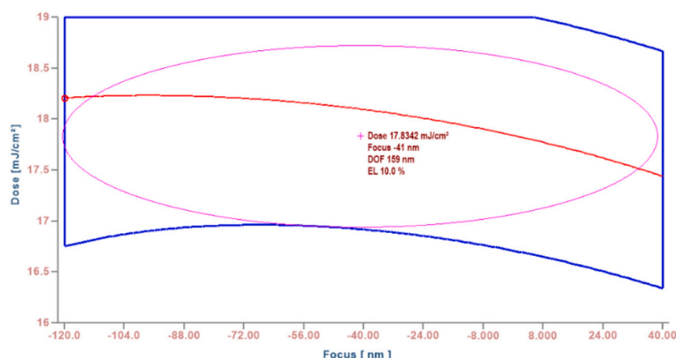

Fig. 10. Process window for PR4-IL3 at 80 nm pitch.

Table 3
Litho performance for Immersion 2 approach with PR3-IL3 and PR4-IL3 process options.

Process	Pitch	Mean CD	Dose	WCDU	LCDU	X/Y
PR3-IL3	82 nm	41.05 nm	16.3 mJ	0.76 nm	3.81 nm	1.00
PR4-IL3	80 nm	41.70 nm	18.5 mJ	1.59 nm	3.85 nm	1.00

splits are based on the selection of 2 different PTD photoresists and 2 different illumination sources. To enable pillar patterning, two perpendicular line structures were exposed with a single PTD resist coating process. Fig. 11 shows the design of two L/S masks used to print pillars.

The experiments performed using IL4 could not print any pillars for the pitch sizes below 84 nm. The IL5 (a higher NA source), on the other hand, gave good results for both photoresists PR3 and PR4. A reasonable litho process could be obtained for 78 nm pitch using the PR3-IL5 and PR4-IL5 processes.

Fig. 12 shows the CD based process window for PR3-IL5 for 39 nm pillars at 78 nm pitch while Fig. 13 shows the process window for PR4-IL5 for the same CD and pitch. Both litho processes resulted in good process windows around 330 nm DOF at 10% EL for PR3-IL5 and 290 nm DOF at 10% EL for PR4-IL5. Table 4 shows the results obtained from the uniform wafer exposures. Again, two wafers for each experiment were exposed and the results averaged.

As a result, the collapse-free smallest pitch that could be printed with Immersion 3 approach is 78 nm. Considering the PR4-IL5 process as the best option, the required dose to print 39 nm pillar CD was around 12 mJ, which makes it cost efficient. The wafer CDU, LCDU and the pillar circularity ratios reported in Table 4 were promising for a robust MTJ patterning process at 78 nm.

4.4. EUV approach

In this approach, single exposures of a DF mask are performed with

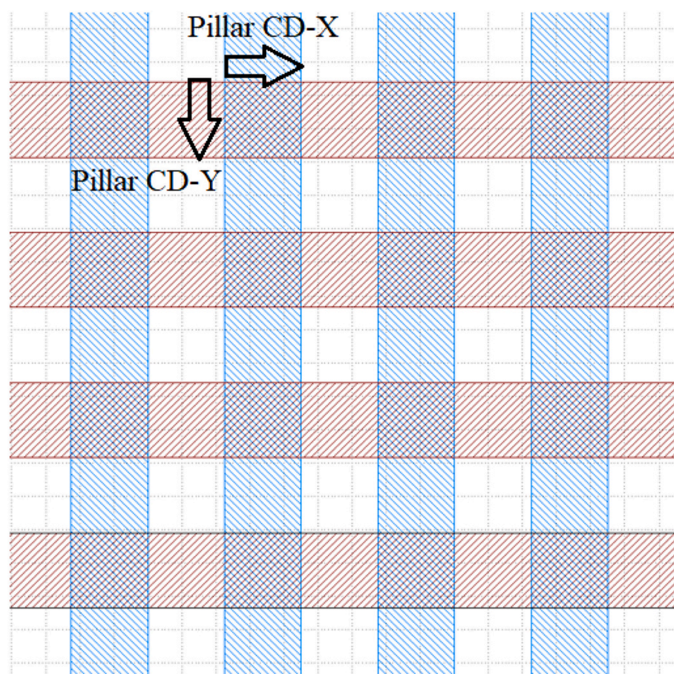

Fig. 11. Perpendicular L/S masks used for pillar printing with double exposure approach.

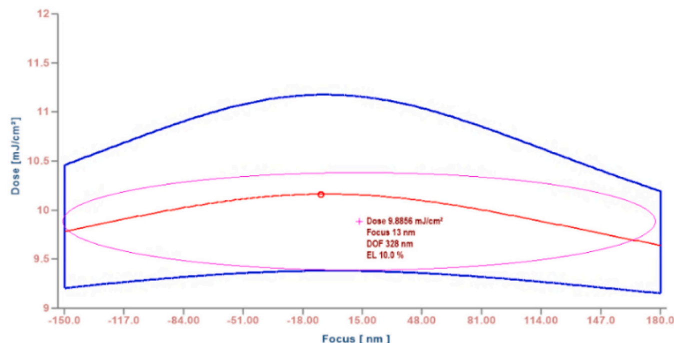

Fig. 12. Process window for PR3-IL5 at 78 nm pitch.

EUV. Standard MCR EUV resist of imec (PR5) were exposed using two different illumination sources, IL6 and IL7. For both illumination sources, the smallest pitch that could be properly printed was 42 nm.

Fig. 14 shows the process window for P5-IL6 for 21 nm pillars at 42 nm pitch while Fig. 15 shows the process window for PR5-IL7 for the same CD and pitch. Both litho processes have a good process window around 115 nm DOF at 10% EL for PR5-IL6 and 154 nm DOF at 10% EL for PR5-IL7.

Table 5 shows the results obtained from the uniform wafer exposures. Similar to previous tests, two wafers for each experiment were exposed and the results averaged.

Even though both illuminations could properly print 42 nm pitch pillars with a reasonable post-litho performance, PR5-IL7 process does not only have a wider process window, but also a better WCDU and LCDU performance with a similar dose requirement and pillar circularity. It should be noted that the required dose to have the 21 nm target CD is a bit high. This could have been lowered by using a higher design CD (positive design bias); however, for 42 nm pitch, the maximum available design CD on the test mask is 24 nm which is already the structure used for the experiments performed.

In order to increase the accuracy of the reported performance values, not only reasonable number of sample points have been used, but also the measurements have been performed on the state-of-art CG6300

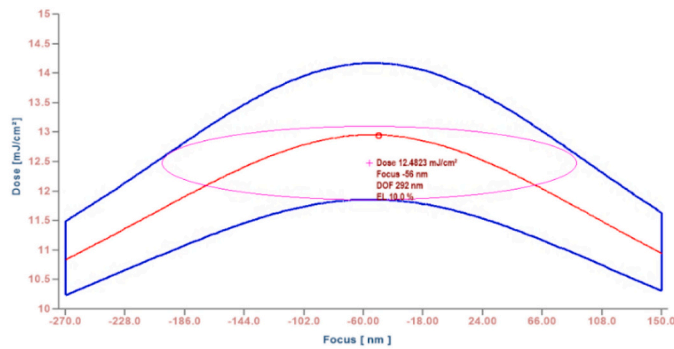

Fig. 13. Process window for PR4-IL5 at 78 nm pitch.

Table 4
Litho performance for Immersion 3 approach with PR3-IL5 and PR4-IL5 process options.

Process	Pitch	Mean CD	Dose	WCDU	LCDU	X/Y
PR3-IL5	78 nm	39.01 nm	9.55 mJ	1.01 nm	2.95 nm	0.96
PR4-IL5	78 nm	38.84 nm	12.1 mJ	0.84 nm	2.75 nm	0.96

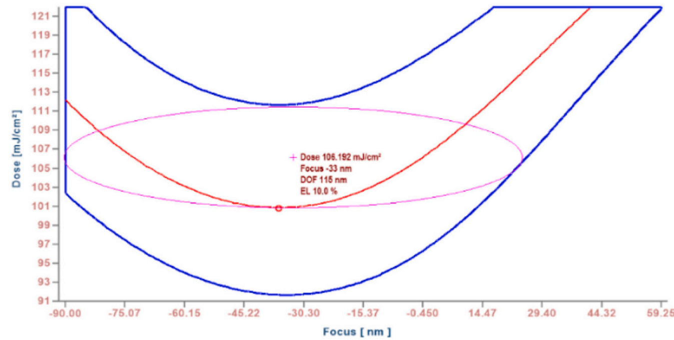

Fig. 14. Process window for PR5-IL6 at 42 nm pitch.

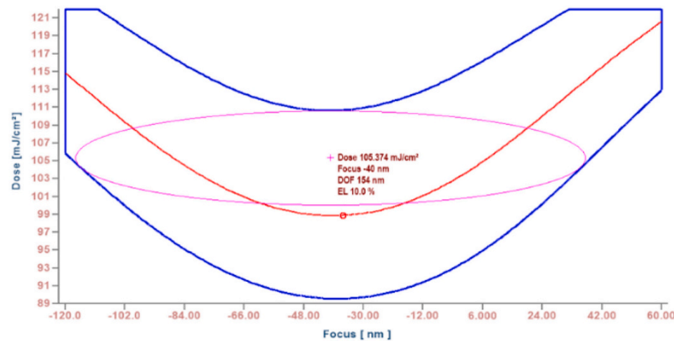

Fig. 15. Process window for PR5-IL7 at 42 nm pitch.

Table 5
Litho performance for EUV approach with PR5-IL6 and PR5-IL7 process options.

Process	Pitch	Mean CD	Dose	WCDU	LCDU	X/Y
PR5-IL6	42 nm	20.55 nm	102 mJ	1.00 nm	2.83 nm	1.05
PR5-IL7	42 nm	21.01 nm	102 mJ	0.57 nm	2.46 nm	1.05

Hitachi CDSEM to enable the bi-directional scan to minimize the contribution of the metrology on the CD error budget.

The masks used for the different experiments are test reticles which include thousands of test structures which makes it difficult to obtain the mask CDU directly from the reticle plate. In order to estimate the impact of the mask CD error on wafer, the pillar CDs measured at the very same locations of 45 different dies have been averaged in order to generate the mean CD value of a certain pillar. This has been done for 40–100 different pillars (depending on the pitch) and the standard deviation of these mean values have been calculated to estimate the impact of the mask CD error. Table 6 below shows the impact of the mask CD error on wafer CDU for the smallest pitch of each approach. The results propose that the contribution of the mask CD error on the wafer CDU is not the main component of the observed differences between different process options tested.

Table 6
Impact of the mask CD error on wafer CDU.

Approach	Pitch	Impact of the Mask CD Error on Wafer CDU (3σ)
Immersion 1	86 nm	0.39 nm
Immersion 2	80 nm	0.38 nm
Immersion 3	78 nm	0.41 nm
EUV	42 nm	0.27 nm

5. Comparison and discussion

The experiments show that the smallest achievable pitch for orthogonal array pillar printing varies between 42 nm and 86 nm depending on the process approach. The choice of the approach amongst the four different possibilities screened is not only a question of the required pitch (meaning higher memory density) but also the overall manufacturing cost. It should be noted that all four approaches are based on single patterning process. Typically, all these four approches use the very same MTJ multilayer together with the same hardmask stack making them have the same cost for deposition, clean and etch process. The main differences between the approaches are coming from the lithography itself. The major parameters are the cost for the lithography tool, the costs for the reticle and also the exposure times, hence the throughput. Even though they allow an obvious pitch scaling, EUV scanners are more expensive solutions compared to 193i lithography tools. Moreover, EUV reticles are also more expensive than the reticles used for immersion lithography. It should also be noted that the double exposure approach requires two times of masks compared to single exposure together with two times of exposure time, making it a relatively expensive solution.

The cost of ownership (COO) model in Fig. 16 below [6] shows that the main cost difference between the 22 nm (half pitch) EUV single exposure process and 45 nm CD 193i single exposure process is caused by the reticle and the litho process (tool price, exposure time etc.) itself.

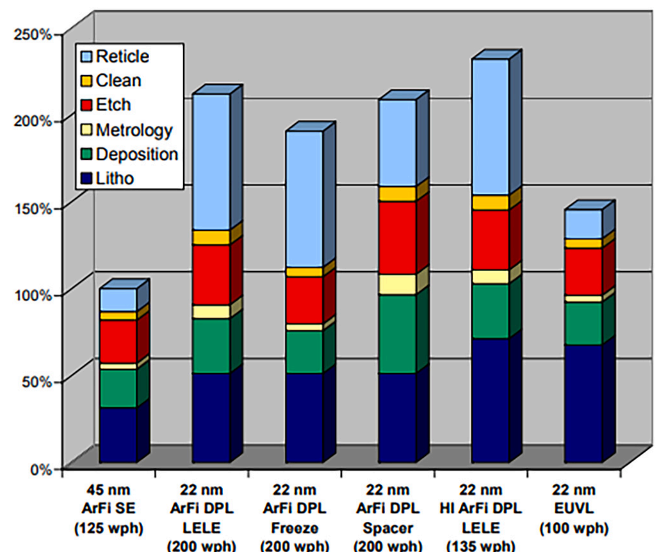

Fig. 16. Layer costs obtained with 20,000 wafers/mask [6].

In [7], it is shown that the double exposure 193i approach induces 67% more lithography process cost compared to single exposure, making it almost as expensive as single exposure EUV process. Hence, for memory densities which require around 80 nm pitch orthogonal array pillars, Immersion 2 approach will be a better solution than the Immersion 3 approach.

Another discussion about the four different approach screened is the alignment/overlay challanges. As mentioned before, all of these approaches typically use the same MTJ stack as well as the hardmask scheme, resulting in similar challanges and performance for wafer alignment. It should be noted that, in the double exposure approach, even though the two masks are exposed sequentially using a single alignment, the movement accuracy of the stage will bring an extra contribution to the overlay error, typically between 1.5 nm to 2.0 nm, for the state-of-art 193i tools.

6. Conclusion

In this paper we focused on screening different lithography process approaches to enable the scaling down of orthogonal array pillar pitch sizes for MTJ patterning of the STT-MRAM. The choice of the approach is a question of the overall manufacturing cost. Single exposure EUV process for instance, obviously enable smaller pitches compared to the immersion lithography process. In this study, rather than comparing different approaches, we have focused on the pitch scaling of orthogonal array pillars within each approach to identify the lithography process limits.

While exploring the smallest pitch sizes that could be printed with different approaches, to guarantee the manufacturing of a robust memory cell, the post-litho performances such as WCDU, LCDU and pillar circularity have been measured and compared. Process exploration was performed by using 5 different state-of-art photoresists used as standard materials at imec and 7 different illumination sources, which are dedicated to the test masks used for the experiments. Amongst the different process approaches, single exposure with immersion lithography has shown good results for 40 nm orthogonal array pillar CD at 80 nm pitch using a combination of LF mask with PTD photoresist. The pitch size could be scaled down to 78 nm with double exposure immersion lithography approach and to 42 nm for the EUV single exposure approach.

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