Low-frequency noise assessment of ferroelectric field-effect transistors with Si-doped HfO_2 gate dielectric

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ABSTRACT

The low-frequency noise of planar transistors with ferroelectric Si-doped HfO_2 as a gate dielectric is investigated and compared with that of undoped HfO_2 reference devices. Predominantly 1/f-like spectra have been observed, which are governed by carrier number fluctuations or trapping in the gate stack. The corresponding noise power spectral density is about a factor of three higher for the reference devices, indicating that Si-doping reduces in a way similar to the trap density in the HfO_2 layer.

Early on, it was realized that ferroelectric (FE) HfO_2-based gate dielectrics have strong potential for future memory applications.[1–4] The FE properties of doped HfO_2 were maintained over a wide thickness range, opening the door for further downscaling[5–7] and low-power operation. In addition, the compatibility with Complementary Metal–Oxide–Semiconductor (CMOS) processing led to several implementations of FE Field-Effect Transistors (FEFETs) as embedded Non-Volatile Memory (NVM) in bulk[8,9] and Silicon-on-Insulator (SOI)[10] CMOSs.

Despite the encouraging results obtained so far, some obstacles remain to be overcome, in order to reach memory operation with sufficient retention and endurance.[11–15] Charge trapping and trap creation in the high-κ oxide have been pointed out as major operation and reliability issues, giving rise to many dedicated defect studies of doped HfO_2-based FEFETs.[11–15]

One of the powerful methods to investigate charge traps in high-κ dielectrics is low-frequency (LF) noise spectroscopy.[16] The type of oxide trap information that can be derived will largely depend on the type of noise present in the material: flicker or 1/f noise enables the study of so-called border traps in the gate dielectric, at tunneling distance (1 nm–2 nm) from the Si/SiO_2 interface,[17–19] while Generation–Recombination (GR) noise probes either individual defect centers in the gate stack giving rise to Random Telegraph Signals (RTSs)[20] or single defect levels in the semiconductor depletion region of a transistor.[21]

Here, LF noise data are presented for planar FEFETs with 9.5 nm Si-doped HfO_2/TiN[14] and benchmarked to undoped HfO_2/TiN stacks subjected to a similar thermal budget, which display ferroelectric and paraelectric behaviors, respectively. The high-κ dielectric has been deposited by Atomic Layer Deposition (ALD) atop of a 1.2 nm *in situ* steam generated (ISSG) SiO_2 interfacial oxide layer. The corresponding equivalent oxide thickness (EOT) is given in Table I and amounts to 1.94 nm (HfO_2:Si) and 2.75 nm (HfO_2 Ref.).

LF noise measurements have been performed on 1 μm wide and 0.5 μm long nMOSFETs (W = 1 μm; L = 0.5 μm); at least ten devices per wafer have been measured to account for noise variability. A Keysight Advanced Low Frequency Noise Analyzer (A-LFNA E4727A) in combination with an Agilent B1500A semiconductor parameter analyzer has been employed. Noise was evaluated in linear operation (V_{DS} = 0.05 V) while stepping the gate bias V_{GS} from weak to strong inversion, around the threshold voltage V_T. The maximum V_{GS} has been kept well below the threshold for ferroelectric switching (<1.8 V) in the case of FEFETs[14,22] in order to assess the "pristine" gate oxide quality by LF noise. This is also illustrated in Fig. 1, showing the input I_D–V_{GS} characteristics (I_D, drain

TABLE I. Relevant parameters for the two types of nMOSFETs studied.

High-κ dielectric	EOT (nm)	V_T (V)	$\langle S_{VG}fWL \rangle$ ($\mu V^2\ \mu m^2$)
HfO_2	2.75	0.785	5×10^3
HfO_2:Si	1.94	0.325	1.7×10^4

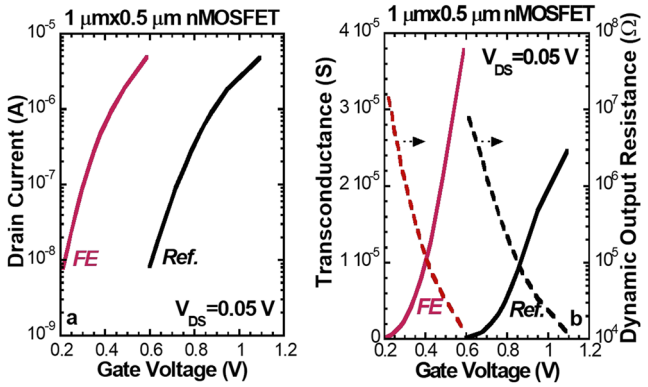

FIG. 1. (a) Input characteristics in linear operation (V_{DS} = 0.05 V) of a HfO_2:Si and a reference HfO_2 MOSFET (b) Transconductance and dynamic output resistance as a function of V_{GS} for the same devices.

current), corresponding to the noise measurement range. It is evident that the V_T of the FEFET is significantly lower than that of the reference device (see Table I). The smaller EOT is related to the higher dielectric constant of Si-doped HfO_2.[14,22] Also shown are the transconductance g_m in linear operation [Fig. 1(b)] and the dynamic output resistance of a typical device; the latter is used to select the load resistor for the noise measurements, using a voltage amplifier. The electron mobility extracted from the Y-function method is 174.6 (Ref.) and 177.0 cm^2/Vs (FE), respectively

Typical spectra of the drain current noise power spectral density (PSD) (S_I) are compared in Fig. 2(a), showing predominantly

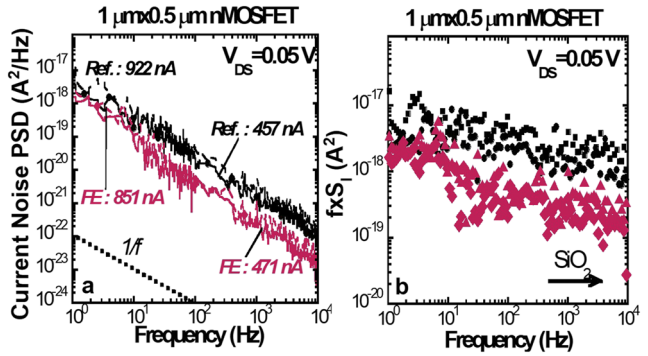

FIG. 2. (a) LF noise spectra for a FEFET (red) and a HfO_2 reference (black) at two different drain currents around V_T. (b) Frequency-normalized drain current noise PSD at 457 nA (full circles), 922 nA (full squares), 471 nA (red diamonds), and 851 nA (red triangles) (~V_T). The transistors were biased in linear operation (V_{DS} = 0.05 V).

1/f noise with a slope γ higher than 1, i.e., 1.3 ± 0.1 for the FE transistor and 1.15 ± 0.1 for the reference transistor. It is also evident that the S_I of the FEFET is significantly lower than that of the reference HfO_2 nMOSFET at a similar I_D. Presenting the frequency-normalized spectra, i.e., f × S_I, in Fig. 2(b) demonstrates that the slope is higher than 1. Occasionally, gate-voltage dependent GR noise can be found, giving rise to a Lorentzian noise component in the spectra and pointing to the presence of Random Telegraph Signals (RTSs) in the gate stack. Here, the focus is on the dominant flicker noise.

To establish the origin of the 1/f noise, S_I at a fixed frequency of 10 Hz [Fig. 3(a)] has been normalized by the drain current squared (I_D^2). This is compared with the $(g_m/I_D)^2$ function, showing a good proportionality between the two curves in Fig. 3(b), for both the reference and the FEFET. This demonstrates that so-called number fluctuations—in other words, charge trapping/detrapping in the gate stack by border traps—dominate the flicker noise.[16–19] In other words, a density of oxide traps (N_{ot}) can be derived from the 1/f noise PSD. The fact that the value is significantly higher for the reference HfO_2 nMOSFET, compared with the FEFET, thus, translates into a higher trap density in the undoped, crystallized HfO_2 layer. In addition, since the slope γ of the $1/f^{\gamma}$ spectra becomes larger than 1 at lower frequencies in Fig. 2(b), the trap density profile increases for a deeper tunneling depth in HfO_2.[19] Assuming an elastic tunneling parameter of 10^8 cm^{-1} yields a trap depth between about 1 nm (f = 10 kHz) and 2 nm (f = 10 Hz). The latter value is clearly in the high-κ layer. As it is well-established that the oxide trap density in HfO_2 is markedly higher than that in thermal SiO_2,[23–25] the slope γ > 1 can be interpreted in terms of an increasing N_{ot} when moving from the interfacial oxide layer (f~10 kHz) toward the high-κ layer (f = 10 Hz).

Figure 4 presents the input-referred voltage noise PSD (S_{VG}) at 10 Hz vs the gate voltage overdrive ($V_{GT} = V_{GS} - V_T$) for a typical device of each kind. S_{VG} has been calculated from S_I by dividing with the corresponding g_m^2. While, for the reference transistor, the S_{VG} vs V_{GT} plot is, on average, rather constant, fluctuating around an average level of ~3×10^{-9} V^2/Hz, the trend for the FEFET shows an increase with V_{GT} from about 3×10^{-10} V^2/Hz to about 8×10^{-10} V^2/Hz. This suggests an increase in the oxide trap

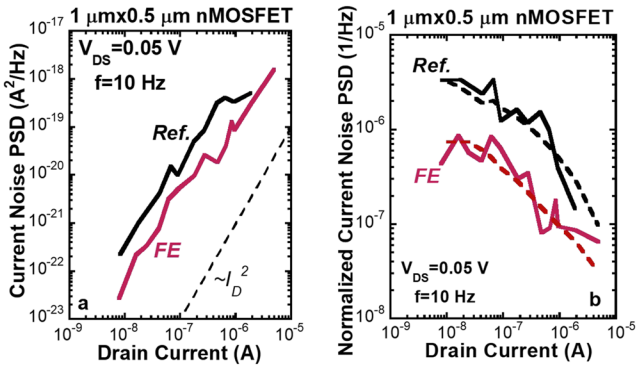

FIG. 3. (a) Drain current noise PSD vs drain current for a FE and a reference nMOSFET. (b) Normalized current noise PSD (full lines) and ~$(g_m/I_D)^2$ (dashed lines) for the same devices. f = 10 Hz and V_{DS} = 0.05 V.

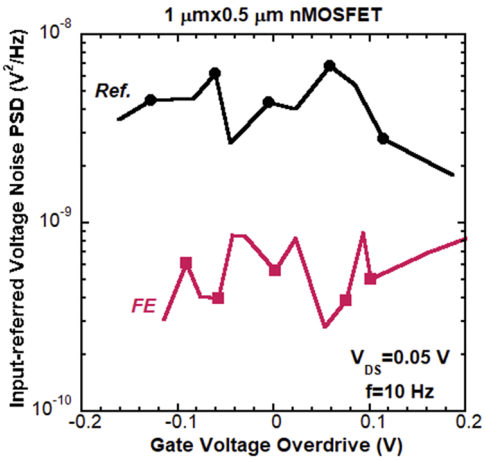

FIG. 4. Input-referred voltage noise PSD vs gate voltage overdrive at f = 10 Hz for a reference and a FEFET.

density at about 2 nm depth (f = 10 Hz) with V_{GT} or with the increasing energy toward the conduction band in silicon.[19]

Finally, Fig. 5 presents the frequency-normalized and area-normalized (W × L) S_{VG} for the two wafers studied, approximately corresponding to $V_{GS} = V_T$. The data have been normalized to the EOT of reference devices (2.75nm) by considering the EOT^2 dependence of the number fluctuations 1/f noise.[17–19] One can derive again that the values for FEFETs are about three times smaller than those for the reference HfO_2 devices. The averages are given in Table I and allow us, in principle, to calculate a trap density in the high-κ layer (at an elastic tunneling distance of about 2 nm from the interface, corresponding to f = 10 Hz). Average N_{ot} values on the order of 1.2×10^{19} cm^{-3} eV^{-1} and 4.0×10^{19} cm^{-3} eV^{-1} can be derived for FEFETs and the reference nMOSFETs, respectively. Note that the normalized noise in Fig. 5 is about a factor 10 to 30 higher than what is foreseen by the International Technology Roadmap for Semiconductors (ITRS) for logic devices with a similar EOT. It means that the trap density of the studied HfO_2 layers is significantly higher than what is achieved for state-of-the-art logic transistors.[26,27] This is most probably related to the defects present along grain boundaries in the crystallized stacks, which are required to obtain the ferroelectric orthorhombic phase, but introduce enhanced defectivity. The non-doped HfO_2 sample is also more susceptible to crystallization during sample processing due to the combination of thick oxide and high thermal budget.

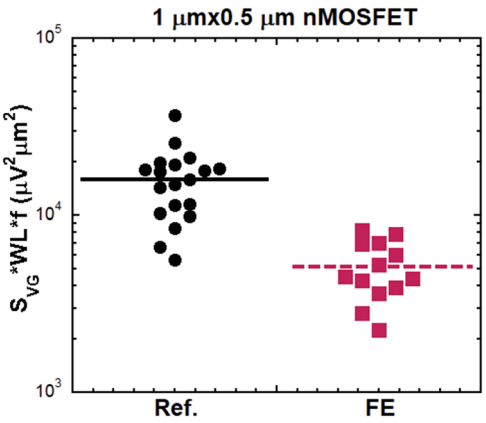

FIG. 5. Area-normalized and frequency-normalized input-referred voltage noise PSD for all measured references and FEFETs.

Finally, one can also observe in Fig. 5 that a similar device-to-device noise dispersion is found for both wafers; about one order of magnitude spread is in agreement with results that are obtained for typical HfO_2-based MOSFETs.

To conclude, it has been shown that the LF noise of FEFETs with a Si-doped HfO_2 gate dielectric exhibits predominantly $1/f^{\gamma}$ noise with $\gamma > 1$. This is interpreted in terms of a trap density in the gate stack that increases with tunneling depth from the Si/SiO_2 interface. While the LF noise PSD is, on the average, a factor three smaller than that for HfO_2 reference transistors subjected to the same thermal budget, the values are significantly higher than those for non-crystalline, thin-oxide logic stacks and are believed to be a consequence of the crystal structure of the stack, which is required to attain the ferroelectric orthorhombic phase.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request

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