Impact of PECVD-prepared interfacial Si and SiGe layers on epitaxial Si layers grown by PECVD (200 °C) and APCVD (1130 °C)

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Abstract

The homoepitaxy of Si is particularly interesting for the purpose of kerfless wafer production, for example in the photovoltaic domain. Substrate surface engineering is a key step prior to epitaxial growth, which will affect the quality of the epitaxial layer and its detachment for layer transfer. In this work, we propose two plasma-based surface engineering methods including the deposition of a bilayer homoepitaxial interface and a SiGe heteroepitaxial interface. Their impact on the crystalline quality of epitaxial Si layers grown both by plasma enhanced chemical vapor deposition (PECVD) at 200 °C and by atmospheric pressure chemical vapor deposition (APCVD) at 1130 °C are explored. Stacking faults are observed in epitaxial Si layers with an ultra-thin epitaxial Si interface layer. For surface engineering method based on the

addition of an interfacial heteroepitaxial SiGe layer, higher interfacial hydrogen content and better bulk epitaxial Si quality are observed in comparison with interfacial homoepitaxial Si layer.

Key words: Epitaxial Si; Interfacial epitaxy; Homoepitaxy; Heteroepitaxy

1. Introduction

The standard Cz wafering technique results in a huge waste of Si material during ingot shaping and wafering. For example, the kerf loss in diamond wafer sawing is around 70 μm per wafer in 2020 according to ITRPV report [1]. Another challenge for such conventional wafering technology, especially sawing of thin Si wafer (< 100 μm), comes from the high total thickness variation. For example, a wafer thickness of 90 ± 37 μm is obtained in contrast to 154 ± 5 μm when cut with diamond wire [2]. Therefore, the standard wafering is not suitable to produce c-Si thin layers (< 50 μm), which can be used as micro electromechanical system (MEMS) devices [3], sensors [4] photovoltaic (PV) cells [5], transistors. Moreover, handling of the thin c-Si wafers requires their transfer on glass [6], or on flexible substrates such as plastic [7] and metal tape [8] and polyimide [9]. As a consequence, kerfless layer-transfer or lift-off techniques have been studied and developed which can be either based on "top-down" or "bottom-up" approaches. The former approach consists of kerfless wafering of Si ingots or wafers, while the latter one includes c-Si growth either from liquid or gas phases. For the "top-down" approach, methods can be found such as direct film transfer by H^+ ion implantation near wafer surface [10] and epifree process with H_2 annealing at 1100 °C of Si trenches fabricated by reactive ion etching [11]. In the "bottom-up" approach, when the melt-assisted epitaxial growth is concerned, there

exist wafer equivalent techniques such as string ribbon growth [12]. Also, there are methods based on liquid-phase epitaxy (LPE), such as the epi-lift technique, which can grow a Si epitaxial layer on a c-Si substrate with partial mask [13]. As far as the gas phase epitaxy (GPE) is considered, there are several methods such as ELTRAN on non-sintered porous Si [14]; epitaxial foil on sintered porous Si using atmospheric pressure chemical vapor deposition (APCVD) [15] and epitaxial Si growth from plasma enhanced chemical vapor deposition (epi-PECVD) [16, 17].

Different seed wafer treatment methods have been developed prior to epitaxial growth. For example, wafer surface cleaning methods such as HF-based wet cleaning [18, 19] and plasma-based dry cleaning with SiF_4 [20, 21], Ar [22], H_2 [23, 24]. Moreover a wide variety of surface preparation methods has been studied, such as (i) epitaxial Si layer on Si substrate by a bilayer interface with hydrogen incorporation [25]; (ii) epitaxial Si growth on HF-prepared porous Si surface [26]; (iii) Ge epitaxial layers on Si substrate with an Fe_3Si insertion layer [27]; (iv) GaAs substrate with Ga-rich surface for Ge epitaxy [28]; (v) Ge buffer layers on Si substrate for epitaxial III-V layer [29]; (vi) SiGe graded buffer layer for SiGe growth on Si [30]; (vii) lapped and chemically polished Si substrate for epitaxial Si layer [31]; (viii) strained Si layer grown by He ion implantation into Si/SiGe heterostructures [32]; and (ix) heteroepitaxial growth of GaSb on Si [33] or Ge on Si [34] with the help of nanodot crystals contacted through nanowindows in an interfacial SiO_2 layer on Si substrates. Here, we propose to use a hydrogenated bilayer interface prepared by PECVD. To investigate the influence of this bilayer interface on epitaxial Si layer quality, we use it in conjunction with two types of epitaxial techniques with different growth temperatures: PECVD (200 °C) and APCVD (1130 °C).

Besides H^+ ion implantation or PECVD with a hydrogen plasma, H atoms can also be introduced by post H_2 plasma treatment, for example, plasma hydrogenation of strained Si/SiGe/Si heterostructures [35] with a two-step approach including growth of the strained intermediate SiGe film by molecular beam epitaxy (MBE) together with post plasma hydrogenation. The drawback of this technique is its long hydrogenation time as it uses a hydrogen plasma at 250-300 °C for 1 h and then at 300-350 °C for 2 more hours [35]. Here, we develop an effective interface modification method based on *in-situ* H-containing plasma treatment by depositing a thin epi-PECVD SiGe layer at the low temperature of 200 °C, within 2 minutes. We compare this technique to the H_2-plasma assisted CVD interfaces that we have presented above. Samples with standard HF-wet cleaning are used as references.

The quality of the epi-Si films and their interfaces was studied by various techniques such as High-Resolution Transmission Electron Microscopy (HRTEM), Annular Dark Field (ADF) Scanning Transmission Electron Microscopy (STEM), Secondary Ion Mass Spectrometry (SIMS) and Energy Dispersive X-Ray Spectroscopy (EDX). The influence of interfacial structures on epitaxial Si layer is presented and discussed.

2. Experiments

Highly boron-doped c-Si wafers (resistivity of 0.001 Ω·cm, 500 μm thick, single side polished, 100-oriented) were chosen as the seed substrate. The standard dipping into 5 % HF for 30 seconds is applied to the substrates (4-inch wafer) in order to remove the native oxide before loading into the reactor chamber. Three

types of substrate surface engineering methods are used here. Then, in order to grow epitaxial Si layers, either PECVD (1 μm for both sample A and B) or APCVD (4 μm for sample C; 10 μm for sample D) is applied to surface-treated Si wafers (Figure 1 (b)). The bulk epi-PECVD growth condition was obtained at a substrate temperature of 200 ˚C, a pressure of 2.3 Torr, a power density of 70 mW/cm^2, SiH_4: 4 SCCM, H_2: 200 SCCM, time: 1800 sec, in a semi-industrial PECVD reactor cluster tool from MVSystems LLC. The growth rate of epi-PECVD is around 12 nm/min. The growth temperature of epi-APCVD is 1130 °C with $SiHCl_3$ as precursor and H_2 as carrier gas at 1 atm, in an EPSILON2 reactor from ASM. A much higher growth rate of epi-APCVD can be achieved (4 μm/min). Note that there is a ramp up and pre-bake in H_2 before APCVD epitaxial growth.

The substrate engineering methods, illustrated in Figure 1(a), were the following:

I. In the first case, the c-Si substrate was treated only with HF dipping prior to epitaxial Si growth via PECVD (sample A) and APCVD (sample C).

II. The second surface engineering method consists of adding an ultra-thin homoepitaxial bilayer with lower crystallinity as compared to bulk epi-PECVD. The corresponding growth conditions at a substrate temperature of 200 °C are as follows: i) at the total pressure of 1.8 Torr, an RF power of 35 mW/cm^2, SiH_4 and H_2 flow rates of 2 and 200 SCCM respectively, were applied during a growth time of 60 sec; ii) then at a pressure of 1.7 Torr, power density of 17 mW/cm^2,

SiH_4: 1 SCCM, H_2: 200 SCCM, were applied during a growth time of 60 sec. The bilayer thickness is around 20 nm by fitting ellipsometry measurements. This interface preparation was then followed by either PECVD (sample B) or APCVD (sample D). Note that PECVD is realized with one pump-down process, whereas for loading in the APCVD reactor the samples must be unloaded and brought back to atmosphere.

III. In the third engineering method an interfacial heteroepitaxial SiGe layer was grown in the same PECVD reactor prior to bulk epitaxial Si growth, where 1 SCCM of GeH_4 with a dilution of 1 at. % in H_2 is added to the same growth condition as for the bulk Si epitaxy, for a growth time of 2 min followed by PECVD epitaxial growth (sample E). The detailed growth conditions for these samples can be found in Table 1.

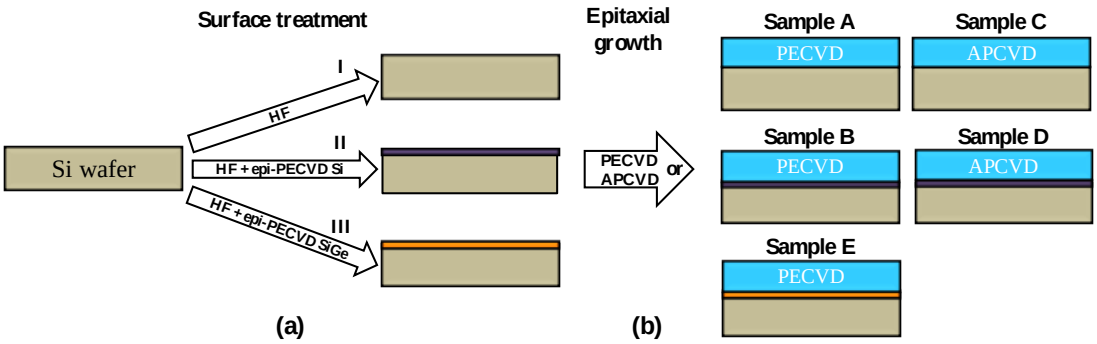

Figure 1. Schematic illustration of process chart with three surface engineering methods. (a) Three surface treatment methods including (I) HF; (II) HF + epi-PECVD Si and (III) HF + epi-PECVD SiGe are applied to a given Si substrate. (b) Epitaxial Si films grown on these Si wafers treated with either PECVD or APCVD.

Table 1. Detailed epitaxial growth conditions for different samples.

Samples	**Epitaxial region**	**Temperature (°C)**	**H_2 (SCCM)**	**SiH_4 (SCCM)**	**GeH_4 (1 % in H_2;**	**$SiHCl_3$ (SCC**	**Pressure (Torr)**	**Power (mW/cm^2)**	**Time (seconds)**
A	Bulk	200	200	4			2.3	70	1800
B	Bilayer Si	200	200	2			1.8	35	60
		200	200	1			1.7	17	60
	Bulk	200	200	4			2.3	70	1800
C	Bulk	1130	200				760		1800
D	Bilayer Si	200	200	2			1.8	35	60
		200	200	1			1.7	17	60
	Bulk	1130	200				760		1800
E	SiGe	200	200	2	1		2.3	70	120
	Bulk	200	200	4			2.3	70	1800

TEM lamellar were prepared with precision ion polishing system (PIPS) and its characterization was performed with a Thermo Fisher Titan 60-300 equipped with a Cs-corrector of the objective lens delivering a point-resolution of 0.08 nm at 300 kV. The images were recorded at that voltage.

3. Results

Figure 2 shows the cross-sectional TEM images of four types of epitaxial layers on c-Si substrate. Epi-PECVD Si thin film without (sample A) and with an ultra-thin epi-PECVD interface bilayer (sample B) are presented in Figure 2 (a) and (b). Hydrogen platelets (marked with white arrows in Figure 2 (a)) can be observed in sample A, which is typical for PECVD-grown epitaxial layers. Interestingly, only few platelets can be found in sample B when an ultra-thin epi-PECVD interface bilayer

exists. However, a stacking fault is observed, marked with a red arrow in Figure 2 (b). In order to verify the suitability of the above interface modification methods, and to better discriminate the role of the interface layer and the growth technique, we apply them to APCVD epitaxial Si growth, since the growth temperatures for APCVD and PECVD are very differences: 1130 °C for APCVD and 200 °C for PECVD. Figure 2 (c) and (d) show the epi-APCVD Si thin films without (sample C) and with an ultra-thin epi-PECVD interface bilayer (sample D), respectively. Under HF wet cleaning condition (sample C), we observe a defect-free interface and bulk in comparison with sample A, which can be explained by the higher deposition temperature (faster growth rate; lower impurity content) during epi-APCVD growth and absence of ion bombardment. However, when sample D with epi-PECVD interface layer is considered, large stacking faults can be observed as shown in the inset of Figure 2 (d).

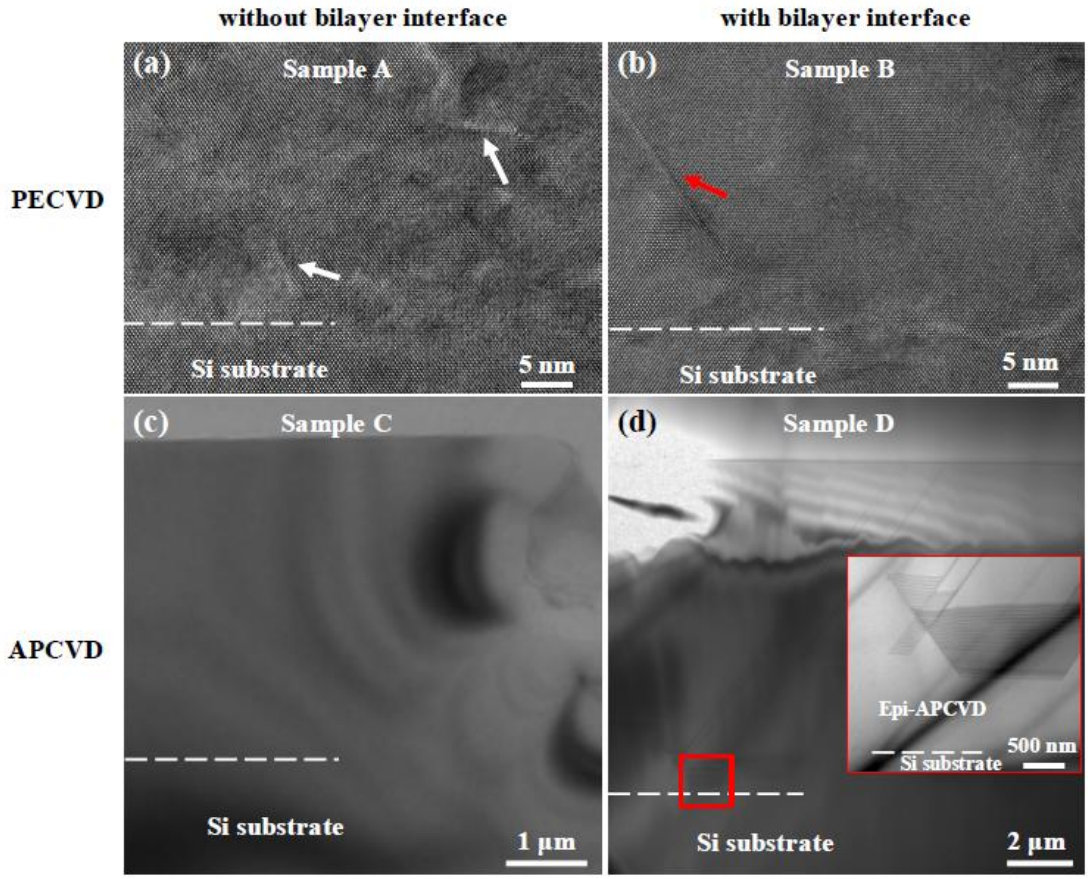

Figure 2. Cross-sectional TEM images of four types of epitaxial Si layers on c-Si. Epi-PECVD (a) without an intermediate layer and (b) with an ultra-thin epi-PECVD layer prior to the deposition of the bulk epi-PECVD. Epi-APCVD (c) without an intermediate layer and (d) with an ultra-thin epi-PECVD interface layer. Inset in (d) shows an enlarged view of the region marked by the red square.

The stacking faults in epi-APCVD Si layer with bilayer interface (sample D) are analyzed with the help of TEM characterization. Faults usually start at the interface [36-38]; however, for the present TEM samples, the faults start inside the epitaxial Si. The reason is probably that the sample cut is not the origin of stacking fault. One of the faults is shown in Figure 3 (b). Figure 3 (c) and (d) present the enlarged image of faults, which are marked by a big red square and a small red square in Figure 3 (b),

respectively. We can observe that the faults go by pairs, separated at the beginning by a dark area in the bright-field TEM.

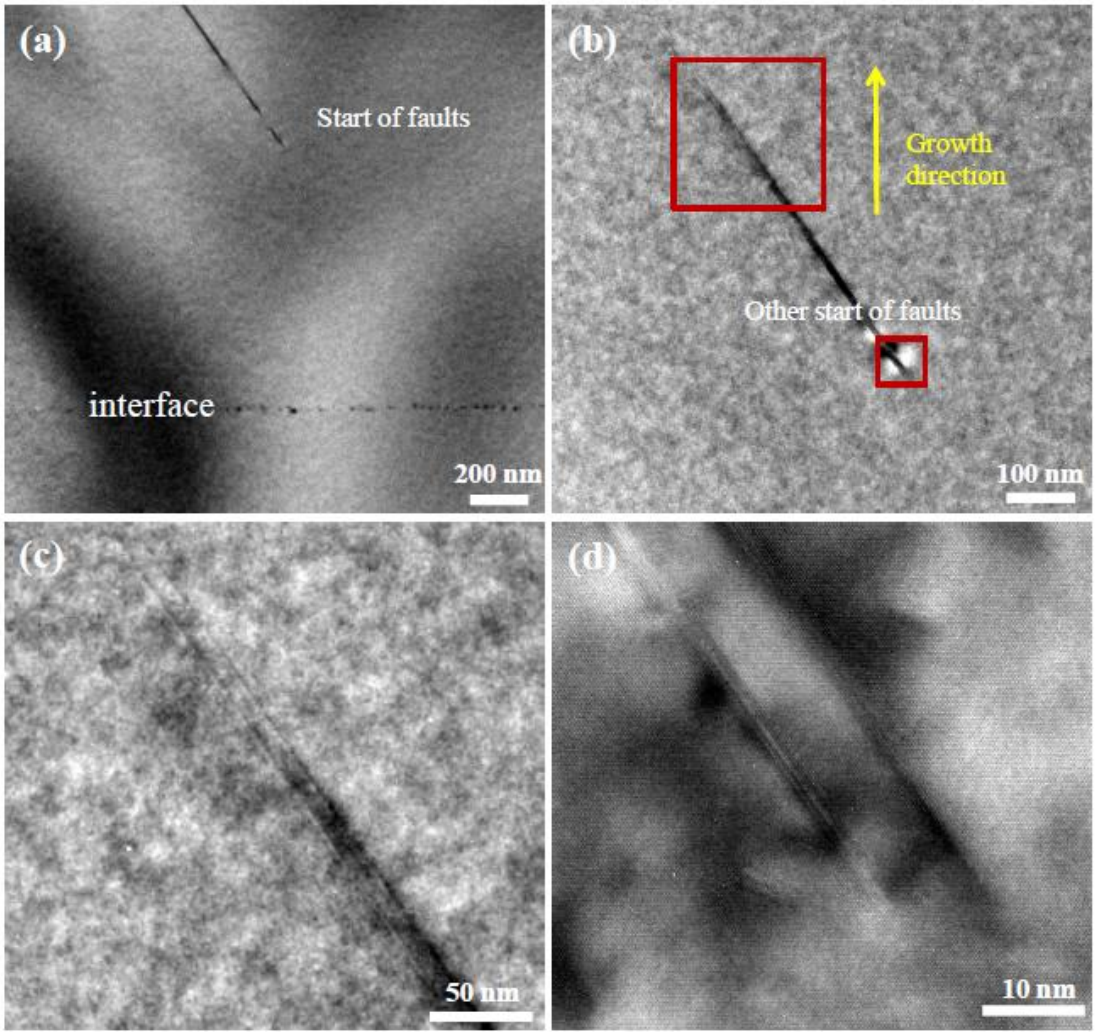

Figure 3. (a) Cross-sectional TEM image of epi-APCVD film grown on bilayer interface. (b) TEM image showing the faults of epitaxial layer. (c) and (d) TEM images showing the enlarged image of faults marked by big red square and small red square in (b), respectively.

To further characterize these faults, STEM (Figure 4 (a) and (b)) and HRTEM (Figure 4 (c) and (d)) are applied. We can observe several parallel bright line shape

defects accompanied by inverted-V-shaped defects as indicated by a red arrow in Figure 4 (a). A zoom on parallel line shape defects is shown in Figure 4 (b) revealing some possible impurity precipitates. However, such kind of impurity precipitate cannot be detected by EDX. Figure 4 (c) is a HRTEM image of an inverted-V-shaped defect, from which we can see that the fault with opposite displacement vector is annihilated (as pointed by the arrow). Note that this inverted-V-shaped defect comes from the stacking faults as shown in the inset of Figure 2 (d). Figure 4 (d) displays an atomic-resolution image of the region marked by the red box in Figure 4 (c), which presents the atomic structure of the intrinsic stacking fault of ABCBCABC, obtained here by shifting one atomic plane from face centered cubic (fcc) stacking of ABCABC.

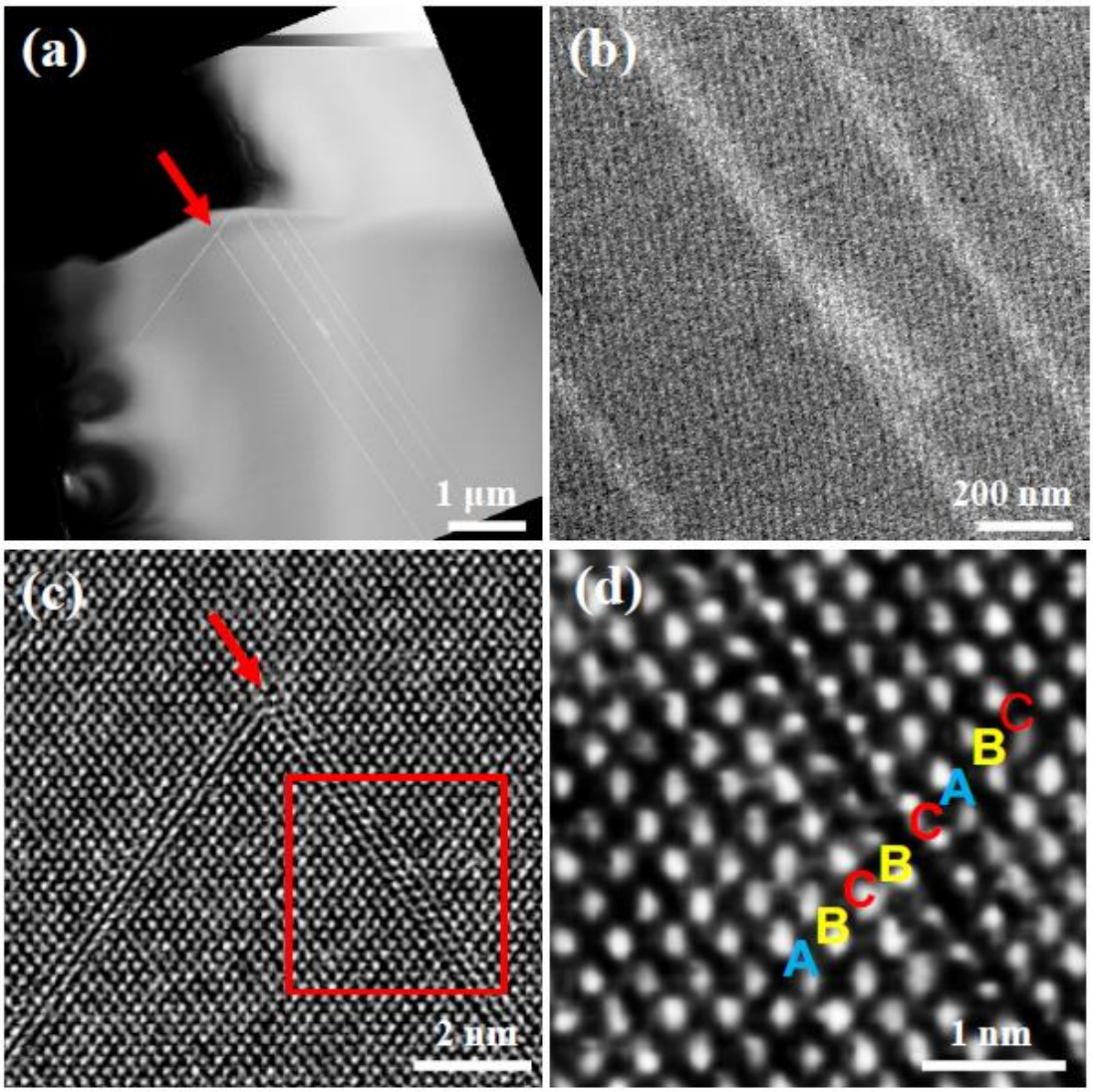

Figure 4. ADF-STEM/HRTEM images of epi-APCVD based on bilayer interface. (a) ADF-STEM. (b) is a zoom of blue square in (a). (c) HRTEM of an inverted-V-shape defect. (d) is a zoom on the red square in (c) showing the intrinsic stacking fault of ABCBCABC.

Since the incorporation of H_2 atoms at the interface favors the detachment of the c-Si thin film, we study the effect of heteroepitaxy with H_2 incorporation (sample E). The growth time (2 min) of the 20 nm SiGe layer is very short as compared to the

hydrogenation time of 3 hours in the case of MBE-grown SiGe strained films [35]. Figure 5 (a) shows the SIMS profiles (CAMECA IMS7f) in epitaxial films with two interface engineering methods. The red dashed curve corresponds to the homoepitaxial Si interface with a gradient showing 2.5×10^{21} at./cm^3 of H_2 at the interface. The blue solid line shows the H-profile in the case of adding a heteroepitaxial SiGe interface layer (20 nm), where a much higher H_2 concentration (7×10^{21} at./cm^3) is measured. This H_2 concentration is also much higher than that obtained with hydrogenation of MBE-grown SiGe strained films (3.5×10^{20} at./cm^3) [35]. The higher H_2 concentration in SiGe layer could be due to a higher concentration of defects in our PECVD-grown film as compared the reported MBE-grown film. We can see that, despite the very small amount of Ge atoms (0.7 at. % in Si), they have a huge impact on H incorporation at the interface. Figure 5 (b) shows a cross-section high-angle annular dark-field STEM (HAADF-STEM) image presenting a stack of c-Si/c-SiGe/c-Si. The chemically sensitive Z contrast in the STEM image in Figure 5 (b) reveals the presence of a thin SiGe layer since Ge atoms have larger atomic number and the signal intensity of the STEM image varies monotonously with the atomic number of the elements in the sample. Note that the bright particles in Figure 5 (b) are artifacts produced by the ion milling process during the TEM lamella preparation. To further analyze the structure of the interface, EDX is used to characterize the distribution of Ge atoms as well as their concentration. Figure 5 (c) presents the EDX mapping of Ge atoms (Ge-K) showing that their presence corresponds exactly to the bright zone in Figure 5 (b). The composition profile of Ge atoms across the interface is shown in Figure 5 (d). The average Ge composition in the epitaxial SiGe film can be calculated to be 0.7 at. % with respect to Si atoms.

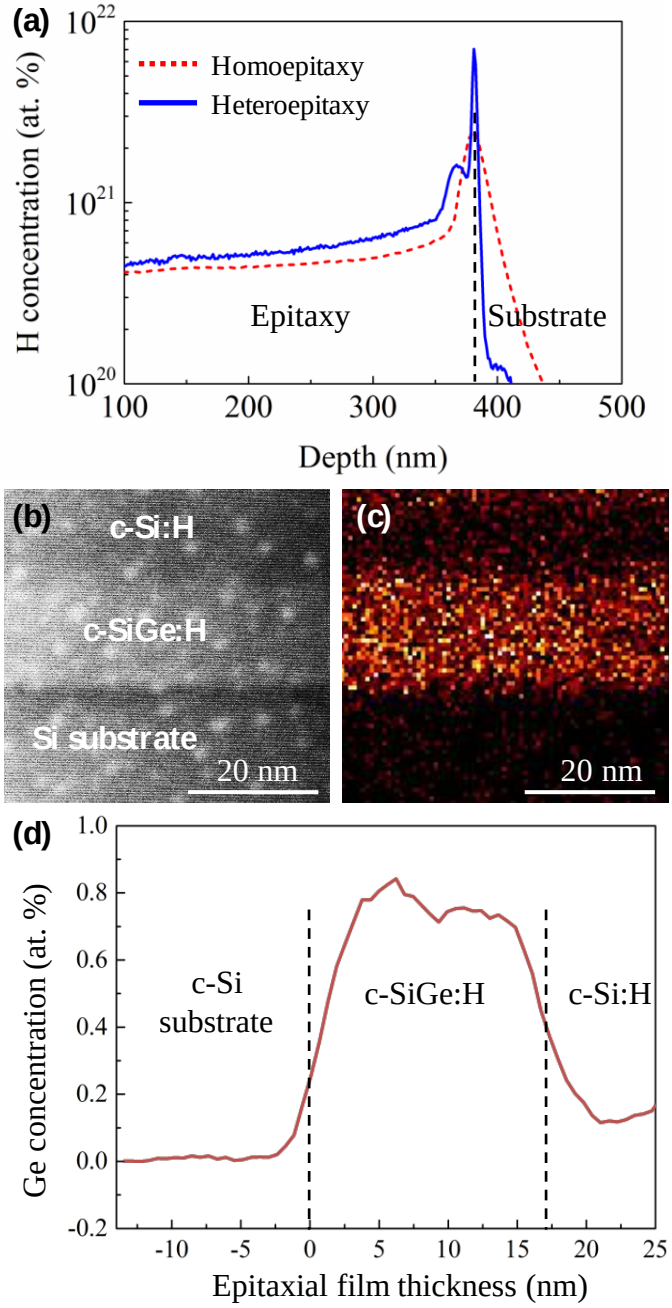

Figure 5. (a) SIMS profiles of H atoms across the interface between the epitaxial films and the substrate for two types of epitaxial growth including homoepitaxy of Si on Si (red dashed curve) and heteroepitaxy of Si on SiGe (blue solid curve). (b) HAADF-STEM image of an epitaxial Si film on a Si substrate with a thin SiGe interfacial film (the white nanoparticle-like features are artifacts due to ion milling during the preparation of the TEM lamellar). (c) EDX mapping of Ge atoms (Ge-K) at

the same location as (b). (d) EDX profile of Ge atoms across the interface between the epitaxial Si films and the substrate.

Figure 6 shows the TEM and HRTEM images used to investigate the microstructures of the heteroepitaxial Si film deposited on the SiGe interface layer. A low magnification image of the TEM cross-section is shown in Figure 6 (a). The HRTEM image (Figure 6 (b)) shows the good crystallinity of the epi-PECVD film near its surface. A low magnification TEM image in Figure 6 (c) reveals the H_2 platelets (marked as white arrow) in the bulk of the epi-PECVD film. Note that the TEM image acquisition is realized by defocusing the electron beam of TEM to enhance the contrast due to platelets. The existence of such kind of H_2 platelets has been observed many times in our previous studies of epitaxial Si films on Si substrates without any intermediate layers [39, 40]. The inset in Figure 6 (a) shows the fast Fourier transform (FFT) of the image, which exhibits some streaks due to planar defects. A stack consisting of the c-Si substrate, the c-SiGe epitaxial interface and the c-Si epitaxial film can be observed in the HRTEM image of Figure 6 (c). The higher H_2 incorporation, at the interface in the case of c-SiGe can be related to a higher defect concentration in the c-SiGe interfacial layer.

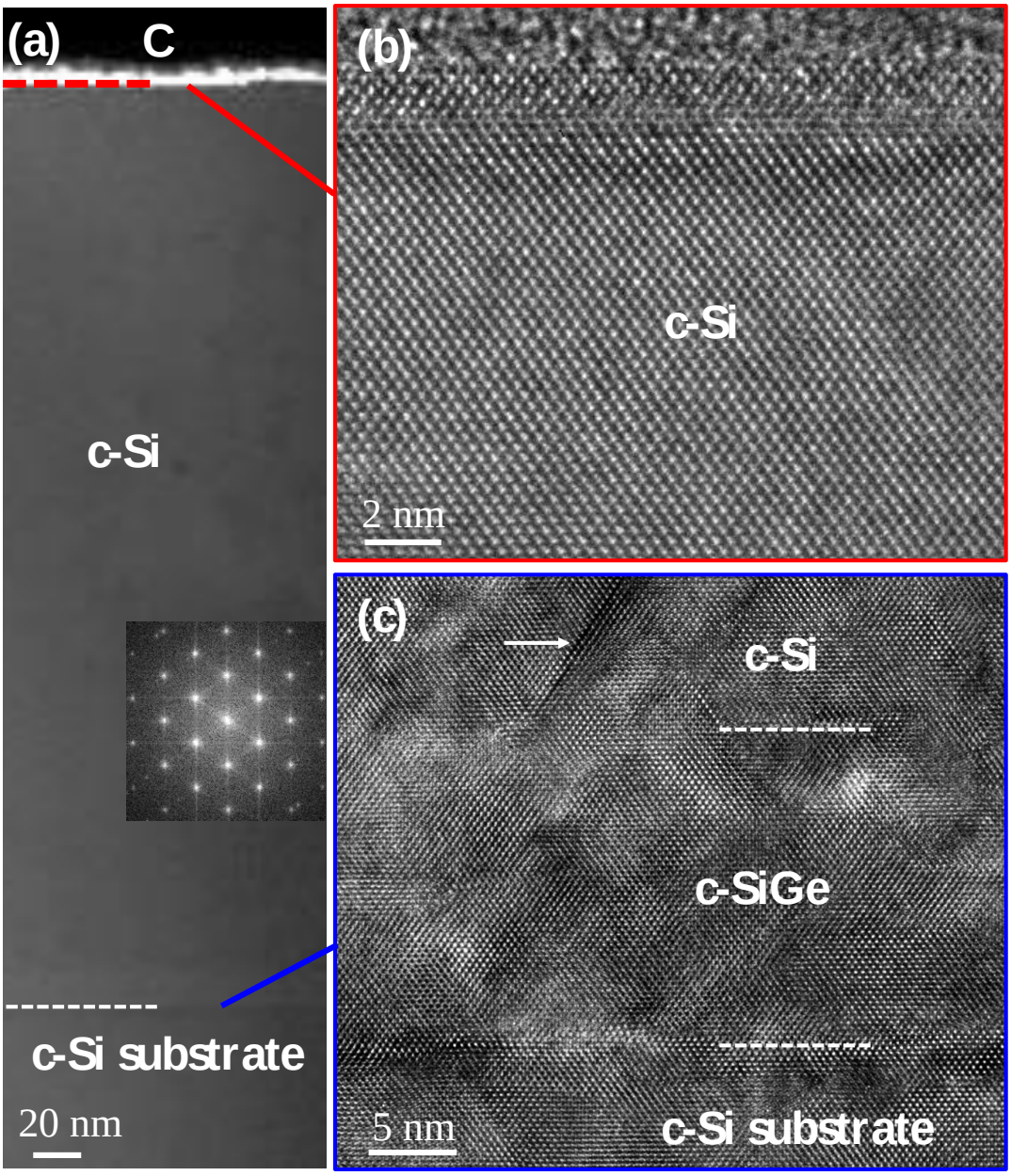

Figure 6. (a) Cross-sectional ADF-STEM image of epi-PECVD film with a heteroepitaxial interface layer. Inset in (a) shows the FFT of the image. (b) and (c) HRTEM images showing the surface of the c-Si layer and its interface with the c-Si substrate, respectively, including the c-SiGe heteroepitaxial layer.

4. Discussion

The influence of the interface structure on epitaxial Si is discussed as follows. As expected, and according to the above characterization results, the quality of epitaxial Si grown by APCVD depends on the interface structure. Three interface modification approaches were studied in this work including HF wet cleaning, epi-PECVD Si interface layer and PECVD heteroepitaxial SiGe interface layer. The quality of epi-PECVD Si based on bilayer interface is close to that of epi-PECVD Si based on standard HF wet cleaning. When epi-APCVD is considered, a good epitaxial quality (both interface and bulk) of APCVD with HF wet cleaned interfaces can be observed, however, the Epi-PECVD thin interface layer introduces stacking faults in the bulk of the epi-APCVD film. The presence of faults within the epitaxial layer is probably due to the interface-induced strain, which may be relaxed in the form of the faults. The source of strain could be due to the higher disorder of Si lattice in PECVD epitaxial Si in contrast to the one in Si wafer. For the SiGe heterogeneous interface, the higher interfacial H_2 incorporation in epitaxial layer can be attributed to the defective SiGe layer, probably due to the lattice mismatch between the Si and SiGe layer. The defects offer possible sites for H_2 bonding [41]. Interestingly, no stacking fault is observed in epi-PECVD layers grown on c-SiGe interfacial layer, showing that a better epitaxial Si quality (Figure 6 (a)) has been achieved compared to the case of a homoepitaxial bilayer interface (Figure 2 (b)(d)). Considering the SIMS data in Figure 5 (a), a claim can be made that surface engineering method via c-SiGe interfacial layer can

guarantee not only higher interfacial H concentration (more fragile interface), but also better bulk epitaxial Si quality.

5. Conclusion

As a conclusion, we developed built-in interfaces that could ease the lift-off of Si homoepitaxial layers. Here, we investigated the influence of different interface treatment methods on the quality of the to-be-lifted epitaxial Si layer: traditional HF wet cleaning, ultra-thin epi-PECVD Si bilayer interface and heteroepitaxial SiGe interface layer with high H_2 content. We performed these preparations for two kinds of epi layers: epi-APCVD and epi-PECVD. Due to the high-temperature conditions of epi-APCVD, the epitaxial Si layers obtained with this method have a better quality than epi-PECVD layers when wafers were treated with HF dipping. It is worth noting that stacking faults appear in the epi-APCVD Si grown based on the ultra-thin epi-PECVD Si bilayer. Such kind of stacking faults may be caused by the stress relaxation in the epitaxial Si layer. In contrast, the defect content of epi-layers grown by epi-PECVD on the epi-PECVD interface is differently affected: the interface preparation seems to introduce stacking faults but helps decreasing the density of platelet defects. For the heteroepitaxial SiGe interface with a very small amount of Ge atoms (0.7 at. %), defects are localized at the interface which also has a high H_2 concentration (7×10^{21} at./cm^3) compared to 2.5×10^{21} at./cm^3 in the case of homoepitaxial Si layer, which could be beneficial for layer transfer.

6. Credit author statement

W.C., J.A. and P.R.i.C designed and conducted the experiments, analyzed the data, wrote the main text and prepared the figures. J.L.M. performed the TEM experiments.

V.D. conducted APCVD experiments. All authors participated in discussing and reviewing the manuscript.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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