Cumulated charging mechanisms at gate processing in high-κ first planar NMOS devices

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***Abstract*—In this work, different charging mechanisms occurring during processing of the high-κ (HK) first gate stack of planar NMOS devices are disentangled by comparing various shapes of gate-on-field antennae. Based on different electrical measurements, the distinct electrical signatures of the charging damage related to these mechanisms are shown. Finally, a qualitative explanation is proposed in terms of oxide traps/charges and plasma bias polarity to account for this difference.**

***Index Terms*—charging, plasma-induced damage, antenna**

I. Introduction

It is well-known that MOSFET gate etching with plasma can lead to undesirable degradation of the device oxide due to charging [1], [2]. This issue is particularly critical in HK-first integration, since the gate oxide is exposed to all the gate processing steps compared to HK-last integration.

Many works have investigated the impact of charging damage on high-κ oxides with gate antennae [3], sometimes using both comb and plate antennae [4], [5], [6]. However, it seems that there has been no attempt to discriminate the impact of the different etch steps causing charging-related degradation of the FET devices depending on the type of antenna. Although some authors have compared charging damage in comb and plate antennae, they have obtained conflicting results: comb and plate configurations were reported to result in the same level of degradation in [5], while the damage was clearly higher for the comb layout in the results from [6] and [4].

In this work, time-zero metrics and reliability tests are exhaustively employed to clarify the compounded degradation occurring with both types of antenna in a high-κ-first metal-replacement planar NMOS technology. It is shown that two plasma process can contribute to damage the devices in different ways depending on the antenna configuration, which may be the reason why previous works report conflicting results.

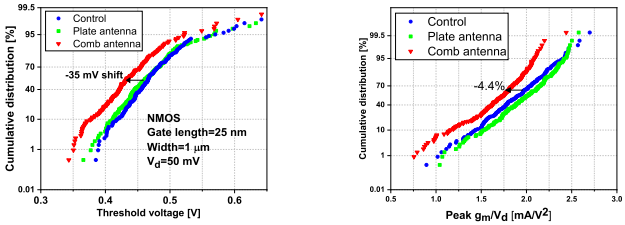
First, the test structures are described, and the electrical measurements are reported. Then, an explanation is proposed for these observations based on plasma physics and HK sensitivity to electrical stress.

II. Test structure description and measurements

The planar MOS devices are integrated with a HK first replacement metal gate (RMG) approach. The interlayer (IL) is grown to 0.9 nm through in-situ steam anneal, before the HK (1.9 nm) and TiN (5 nm) metal etch stop layer are deposited. The poly-Si is patterned with a SiN Hard Mask (HM), which is later removed with a dry etch. The poly-Si gate is then replaced by metal later in the flow, through a wet etch process which is hence not expected to induce charging damage. Finally, there is a 420°C Forming Gas Anneal (FGA) at the end of the process, which can passivate or mask the defects created by charging [7], [8], [9].

Parameter	Control	Plate	Comb
Area [μm^2]	0.74	150.79	160.37
Perimeter [μm]	15.96	83.74	2071
Aspect Ratio [-]	29.6	6.03E3	6.41E3
Sensitivity	None	HM etch	gate patterning and HM etch

TABLE I: Antennae parameters

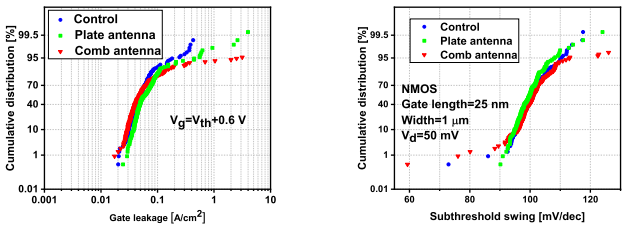


(a) (b)

Fig. 1: Cumulative distribution of V_{th} (a) and g_m (b).

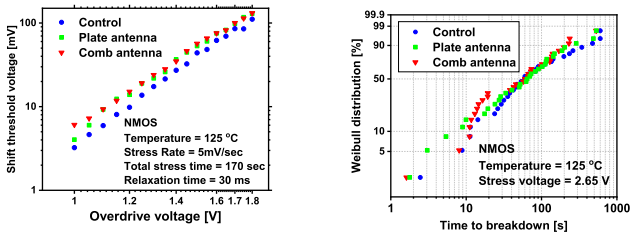
The antennae parameters are listed in Tab. I. The control device antenna has small area and perimeter, it is used as a reference for the measurements on the other antennae. The plate antenna is mostly sensitive to plasma steps landing on the gate surface due to its high area/perimeter ratio, such as HM etch. Finally, the comb antenna is expected to undergo the same degradation as the plate layout from the HM etch due to its similar area, but with the additional effect of the gate patterning step through its high perimeter (both gate patterning and HM etch are performed with inductively coupled plasmas).

The following time zero metrics are considered: threshold voltage (V_{th}), transconductance (g_m), gate leakage (J_G), subthreshold swing (SS) and Gate Induced Drain Leakage (GIDL). They are reported respectively in Fig. 1a, Fig. 1b, Fig. 2a, Fig. 2b and Fig. 3a. It is clear from these measurements that PID induces a selective deterioration of a limited set of parameters (in this case V_{th}, g_m and GIDL) while not the others (J_G, SS). Although the GIDL increase is particularly



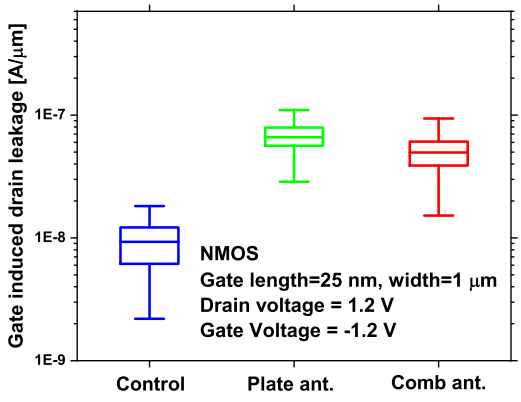
(a) (b)

Fig. 2: Cumulative distribution of the gate leakage (a) and the subthreshold swing (b).

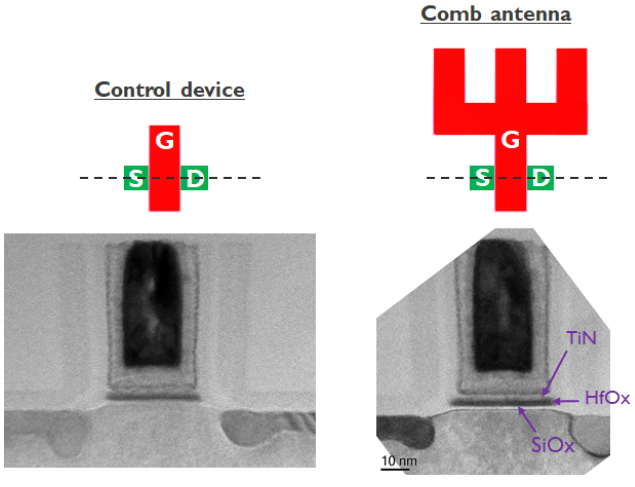


(a) (b)

Fig. 4: Positive bias temperature instability (a) and time-dependent dielectric breakdown (b).

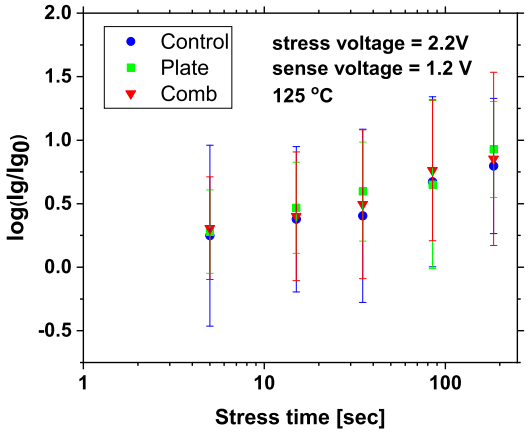


(a)

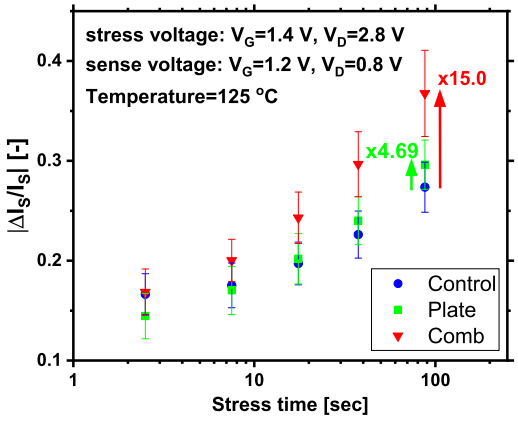


(b)

Fig. 3: (a) Gate induced drain leakage measurement. (b) TEM cross-sections of the control device and the comb antenna device.



(a)



(b)

Fig. 5: (a) Stress-induced leakage current, reported as relative increase of gate current (I_g) over the initial value (I_{g0}). (b) Hot carrier injection evaluated through the relative reduction of the source current (I_s) with respect to stress time.

Measurement	Plate/Control	Comb/Control
$\mathbf{V_{th}}$	∅	-35mV
max $\mathbf{g_m}$ (linear regime, V_d=50 mV)	∅	-4.4%
SS	∅	∅
$\mathbf{J_G}$ (V_{th}+0.6V)	∅	∅
GIDL (V_g=-1.2V, V_d=1.2V)	x7.11	x5.34
PBTI (ramp 5mV/sec, 170sec, 125°C)	+16.6%	+18.2%
TDDB (2.65V, 125°C)	∅	∅
SILC (sense/stress=1.4V/2.2V, 125°C)	∅	∅
HCI (V_g=1.4V, V_d=2.8V)	+4.69%	+15%

TABLE II: Parameter degradation of the plate and comb antennae compared to the control device (V_g is gate voltage and V_d is drain voltage).

preeminent, it is in the same range as in previous work [10]. To determine whether this degradation was purely electrical or linked to differences in the gate profile induced by the antenna, TEM pictures were taken on the control and the comb antenna device, which are compared in Fig. 3b. No physical difference can be observed on the two structures, hence confirming that the degradation observed are linked to electrical charges accumulated during processing and not physical impact of the plasma etch.

The following reliability tests have also been performed to detect charging damage: Positive Bias Threshold Instability (PBTI), Time Dependent Dielectric Breakdown (TDDB), Stress Induced Leakage current (SILC) and Hot Carrier Injection (HCI). They are shown respectively in Fig. 4a, Fig. 4b, Fig. 5a and Fig. 5b. Here also, the impact of PID is very selective, affecting exclusively PBTI and HCI. The results of the time-zero and reliability measurements are reported for the plate and comb antennae in Tab. II as differences from measurements on the control antenna. The symbol ∅ means that there is no statistical difference with the control device.

III. Analysis

It is apparent from Tab. II that V_{th} and g_m are only affected by the perimeter-intensive comb antenna, hence suggesting that they are caused by gate patterning. It can be inferred from the sign of the V_{th} shift and the lack of change in J_g and SS that the degradation is due to fixed positive charges, consistent with the trapped holes hypothesis reported in [4], [11]. The presence of these trapped holes may be explained by the negative sidewall charging occurring during gate patterning due to the isotropic behavior of the electrons in the plasma sheath, as represented schematically in Fig. 6a. These negative sidewall charges bias the gate voltage (V_g) negatively, hence resulting in hole injection into the gate oxide.

In contrast, the degradation of the GIDL and PBTI are similar in both types of antenna, thus suggesting that they are related to its area rather than its perimeter. This can be explained by the top area exposure of the antenna during HM etch as represented in Fig. 6b. It should be noted that the accumulation of positive charges on the gates during HM removal is not only due to electron shading [12] (which would also be perimeter-dependent) but mostly comes from the discharge of ions occurring when the plasma is turned off

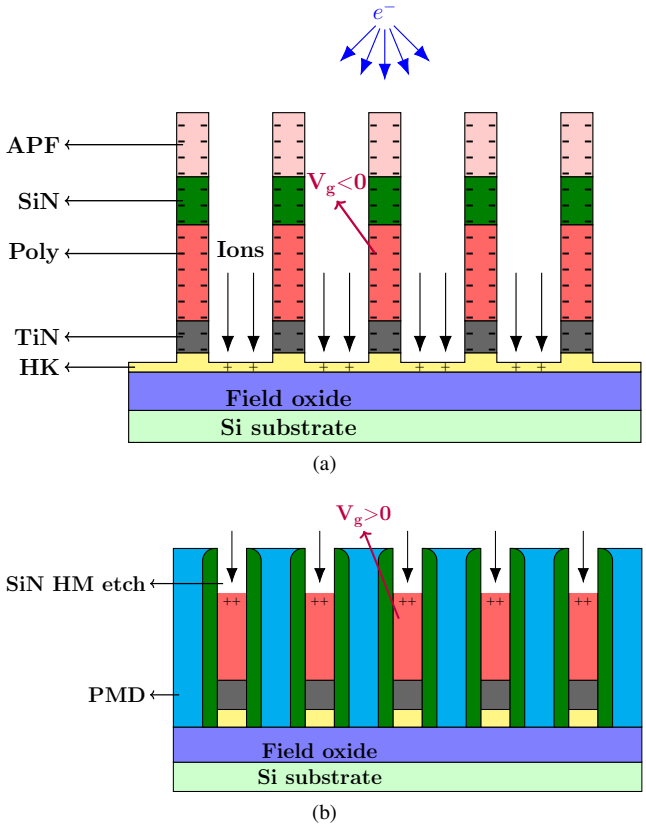


Fig. 6: (a) Poly-Si sidewall charging during gate patterning dry etch (affecting only comb antenna). (b) Poly-Si top surface charging during SiN HM etch (affecting both plate and comb antennae).

[13]. Indeed, the wafer first accumulates electrons during the ignition of the plasma, which are stored on the tool blocking capacitor. The ion flux impinged on the wafer at the end of the plasma process compensates this negative charge, and induces a net positive current expected to be proportional to the area exposed (gate area) [13].

The PBTI deterioration observed in Fig. 4a indicates electron traps creation in the HK [14], hence pointing to positive stress of the gate during the HM etch process (ion charging), consistent with the mechanism described previously and in Fig. 6b. Further, the GIDL component is known to correlate with HK traps [15].

The hypothesis proposed in this section is summarized in Fig. 7. Area-dependent positive charging occurring in both types of antennae generates electron traps in the HK, while perimeter-dependent negative sidewall charging during dummy gate patterning drives fixed positive charges into the gate oxide for the comb antenna.

Finally, inline measurements performed on a different wafer before and after the FGA confirm that the V_{th} and g_m degradation (attributed to gate patterning) behave very differently from the HK electron traps (attributed to HM etch). Indeed, the deviation of V_{th} and g_m in the comb antenna is much

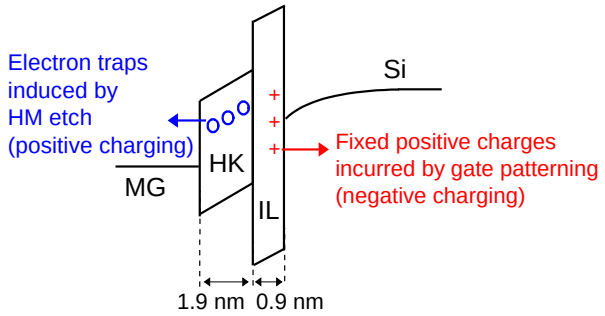
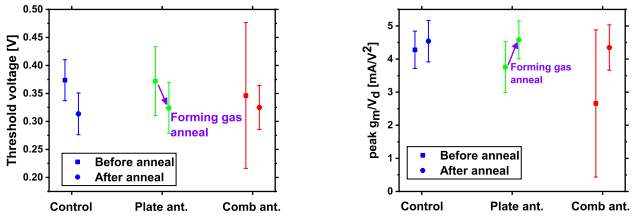


Fig. 7: Sketch of the band diagram with hypothesis of degradation induced by charging damage.



(a) (b)

Fig. 8: Cumulative distribution of V_{th} (a) and g_m (b) comparing data before and after FGA (different wafer).

stronger before anneal as shown in Fig. 8a and Fig. 8b. In contrast, PBTI is not affected by the FGA, as can be observed from the comb antenna results in Fig. 9.

Remarkably, the SILC and TDDB (which are known to be correlated [16]) are not affected by either antenna (as in [4]), which may be due their primary dependence on the IL (or IL/HK interface [16]). It is thus possible that the traps created in the HK do not influence the SILC and TDDB, especially with the relatively thick IL used in this work. Finally, HCI is degraded by the presence of both antennae, which can

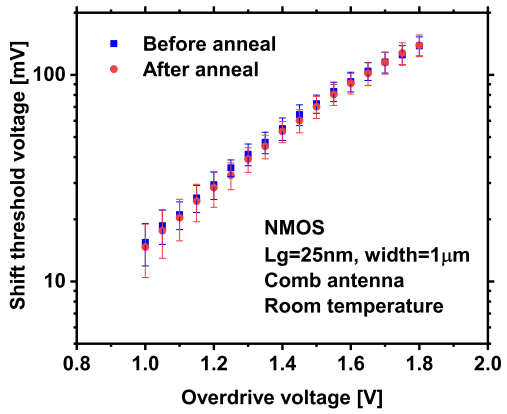


Fig. 9: PBTI before and after FGA on the comb antenna.

be linked to the presumed creation of HK traps in both configurations. The worsening of HCI in the Comb antenna may be due to edge effects related to sidewall charging.

IV. Conclusion

By comparing comb and plate antennae, the multiple types of charging damages observed in the NFETs could be attributed to different plasma processing steps during HK-first RMG fabrication. Based on these results, it was hypothesized that gate patterning induces fixed positive charges in the gate oxide, while the HM etch creates electron traps in the HK. More generally, these results also show that a holistic view of the electrical parameters degradation should be considered when analyzing charging damage.

References

[1] C. T. Gabriel, "Analytical model for electrical and thermal transients of self-heating semiconductor devices," *J. Vac. Sci. Technol. B*, vol. 9, no. 2, p. 370, March 1991.

[2] S. Fang *et al.*, "Thin-oxide damage from gate charging during plasma processing," *IEEE Electron Device Letters*, vol. 13, no. 5, pp. 288–290, 1992.

[3] M. M. Hussain *et al.*, "Plasma-induced damage in high-*k*/metal gate stack dry etch," *IEEE Electron Device Letters*, vol. 27, no. 12, pp. 972–974, 2006.

[4] P. J. Liao *et al.*, "Physical origins of plasma damage and its process/gate area effects on high-k metal gate technology," in *2013 IEEE International Reliability Physics Symposium (IRPS)*, April 2013, pp. 4C.3.1–4C.3.5.

[5] C. D. Young *et al.*, "Comparison of plasma-induced damage in SiO_2/TIN and HfO_2/TIN gate stacks," in *2007 IEEE International Reliability Physics Symposium Proceedings. 45th Annual*, April 2007, pp. 67–70.

[6] K. S. Min *et al.*, "Plasma induced damage of aggressively scaled gate dielectric (EOT $<$ 1.0nm) in metal gate/high-k dielectric CMOSFETs," in *2008 IEEE International Reliability Physics Symposium*, April 2008, pp. 723–724.

[7] A. Martin, "Review on the reliability characterization of plasma-induced damage," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena*, vol. 27, no. 1, pp. 426–434, 2009.

[8] G. Hiblot *et al.*, "Impact of 1 μm TSV via-last integration on electrical performance of advanced FinFET devices," in *2018 IEEE 2nd Electron Devices Technology and Manufacturing Conference (EDTM)*, March 2018, pp. 122–124.

[9] G. Hiblot *et al.*, "Observation of plasma-induced damage in bulk germanium *p* -type FinFET devices and curing in high-pressure anneal," *IEEE Transactions on Device and Materials Reliability*, vol. 19, no. 2, pp. 468–470, 2019.

[10] Siguang Ma *et al.*, "Gate-induced drain leakage current enhanced by plasma charging damage," *IEEE Transactions on Electron Devices*, vol. 48, no. 5, pp. 1006–1008, 2001.

[11] G. Hiblot *et al.*, "Electrical characterization of BEOL plasma-induced damage in bulk FinFET technology," *IEEE Transactions on Device and Materials Reliability*, vol. 19, no. 1, pp. 84–89, March 2019.

[12] K. Hashimoto, "Charge damage caused by electron shading effect," *Japanese Journal of Applied Physics*, vol. 33, no. 10R, p. 6013, 1994.

[13] V. Šamara *et al.*, "A dc-pulsed capacitively coupled planar langmuir probe for plasma process diagnostics and monitoring," *Plasma Sources Science and Technology*, vol. 21, no. 6, p. 065004, oct 2012.

[14] G. Rzepa *et al.*, "Complete extraction of defect bands responsible for instabilities in n and pFinFETs," in *2016 IEEE Symposium on VLSI Technology*, 2016, pp. 1–2.

[15] M. Gurfinkel *et al.*, "Enhanced gate induced drain leakage current in HfO_2 MOSFETs due to remote interface trap-assisted tunneling," in *2006 International Electron Devices Meeting*, 2006, pp. 1–4.

[16] G. Bersuker *et al.*, "Breakdown in the metal/high-k gate stack: Identifying the "weak link" in the multilayer dielectric," in *2008 IEEE International Electron Devices Meeting*, 2008, pp. 1–4.