Gate-Induced-Drain-Leakage (GIDL) in CMOS enhanced by Mechanical Stress

Kookjin Lee, Ben Kaczer*, Anastasiia Kruv, Mario Gonzalez, Geert Eneman, Oguzhan Orkut Okudur, Alexander Grill, and Ingrid De Wolf*

***Abstract*—The impact of mechanical stress on MOSFET gate-induced-drain-leakage (GIDL) current is investigated. The tests were performed on planar short channel p- and n-type MOSFETs. Vertical compressive mechanical stress was induced in the devices by applying a vertical load with a nanoindenter. The applied stress was ranging from several hundred MPa to a GPa range, estimated by finite element modeling. It is reported that GIDL current increases exponentially with mechanical stress. This effect is attributed to mechanical stress-induced reduction in the Silicon band gap and effective mass, leading to enhanced band-to-band tunneling. Furthermore, the GIDL currents are found to change depending on the location where the vertical force is applied, with a higher influence of force on GIDL above the channel.**

***Index Terms*—Band-to-band tunneling, gate-induced-drain-leakage (GIDL), mechanical stress, MOSFET**

I. Introduction

MECHANICAL STRESS (MS) is present in various components of modern very-large-scale integration (VLSI) circuits as the result of the chips fabrication and packaging [1], [2]. Depending on the device structures and processing conditions, intentional and residual MS can vary from a few hundred MPa to several GPa [3]–[7]. MS is known to affect the band structure of semiconductor materials and thus their electrical properties (e.g., energy band gap, carrier mobility) [8]–[12]. Consequently, controlling and deliberately engineering MS presents attractive prospects for improving the performance of advanced CMOS devices. Although previous studies reported various effects of MS on the device performance [8], [11]–[15], the literature on the impact of MS on the off-state leakage current remains relatively scarce due to the limited magnitudes of stress and types of devices [16], [17].

Minimizing the off-state leakage current of CMOS devices is essential for producing reliable low-power CMOS devices for next-generation VLSI circuit design [18]–[21]. One of the most prominent leakage mechanisms in modern CMOS devices is referred to as Gate-induced-Drain-Leakage (GIDL) [22], [23]. It occurs in the gate-to-drain overlap region and is dominated by band-to-band tunneling (BTBT) caused by a high electric field between the gate and the drain [24]–[26]. GIDL current is especially severe at the edge of the gate oxide near the drain region where the electric field is the strongest [18], [26], [27]. It has been shown to have a significant impact on (i) power consumption as the sum of dynamic and static power [20] and (ii) device reliability and lifetime, e.g., time dependent dielectric breakdown (TDDB) [26], [28].

In this study, we report that GIDL current increases exponentially with vertical compressive MS induced by mechanical force application with a nanoindenter. The induced MS, ranging from a few hundred MPa to several GPa, causes (i) a decrease of the channel band gap and (ii) effective mass reduction caused by a sub-band splitting/warping. That, in turn, enhances BTBT and GIDL current. In addition, sensitivity maps were obtained for n- and p-type devices by locally inducing stress at different locations of 54 identical devices-under-test (DUTs). The collected MS-sensitivity maps indicate that GIDL current is especially sensitive to MS above the channel, which means that GIDL currents are strongly dependent on the force applied to the channel.

II. Experiment

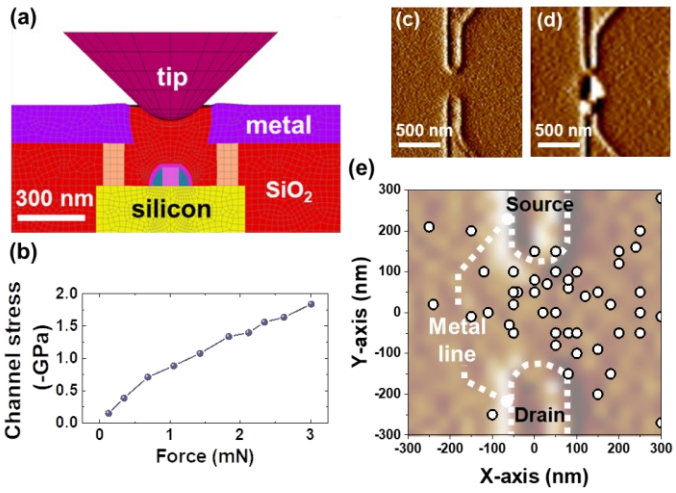

Fig. 1. (a) Cross-sectional illustration of a FEM model used for channel MS calculations for 1.5 mN applied to the tip. The stress at the surface just below the diamond tip is about 10× larger than the stress at the channel. Metal interconnects and vias were considered in the MS calculation. (b) Calculated MS in the channel as a function of the external force applied at the middle of the channel. The SPM topography of n- channel device (c) before and (d) after the measurements. (e) The device topography scan indicating the locations of the indents in the tests repeated on 54 (n-channel) identical devices.

The experiments were performed on p- and n-channel planar *W*

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 https://doi.org/10.1109/TED.2022.3154341

× L = 90 × 70 nm^2 Si MOSFETs with a 1.8 nm thick SiON gate oxide layer (the effective channel length of a pristine device is ~40 nm). Vertical MS was induced in the DUTs by applying an external force with a cube-corner diamond tip of a Bruker's Hysitron TI 950 nanoindenter, as shown in **Fig. 1(a)** [11], [12]. The values of the external force used in this experiment have been selected so that the device would be still fully functional after the force removal. The corresponding mechanical stress ranged from a few hundred MPa to several GPa, which coincide with typical levels occurring in devices due processing and packaging [3]–[7]. These induced MS values were calibrated and calculated using 3D Finite Element Modelling (FEM) in MSC Marc/Mentat software, **Fig. 1(b)** [11], [12], [29], [30]. The load-displacement curves were measured using a standard fused silica sample, then the tip geometry is extracted using the area function obtained from these measurements [30]. The calibrated cube corner tip is used in the simulations of the actual device (SiO_2 layer with a thickness of > 240 nm) and the force-displacement response from modeling and experiments are compared for dual verification. To create GIDL current MS-sensitivity maps, a mechanical force of 1.5 mN was applied at different locations of 54 identical n- and p-channel devices, targeted via topography scans obtained with *in-situ* scanning probe microscopy (SPM), **Figs. 1(c)-(e)**. The precise location where the force was applied was established by finding the intersection of the deepest point (indentation point) along the x and the y axes in topography scans. Device transfer characteristics (I_D-V_G) were measured at $|V_D|$ = 0.05 V and 0.5 V (i) before, (ii) during, and (iii) after the force has been applied. The GIDL current before the force application was extracted + 0.3 V (p-type channel) and - 0.2 V (n-type channel) from V_G at

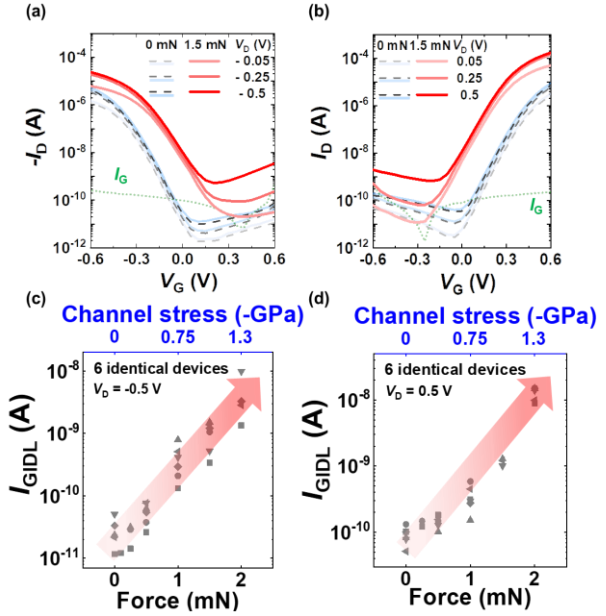

Fig. 2. I_D-V_G before (dashed black line), during (solid red line), and after (solid blue line) application of a mechanical force of 1.5 mN in (a) p- channel ([x, y] = [100 nm, -100 nm]) and (b) n- channel ([x, y] = [20 nm, 0nm]). Note the coordinates in **Fig 1(e)**. I_G have a constant value of less than 0.5 nA regardless of the channel type, drain bias level, and the presence or absence of force. After the application of the force, I_D-V_G curves are completely recovered. I_{GIDL} variations of (c) p-channel and (d) n-channel as a function of force. Channel stress was calculated from FEM simulation by known applied force when the external force is exactly centered on the DUT.

which the minimum value of I_D was observed. The GIDL current during the force application was determined by considering the V_{TH} shift induced by the force application. This extraction method was used to account for different V_{TH} shifts observed in the tested devices due to variations in the applied MS. The devices were diced from a 300 mm wafer and individually attached to a metal sample holder for placement in the nanoindenter system. Next a topography scan was done with the indenter tip at low forces to identify the precise indentation location, and the devices were probed using nanoprobes (MiBots, Imina Techn. SA). In-situ electrical measurements were done during larger force application, making the experiments labor and time intensive.

III. Results and Discussion

The application of mechanical force (MS) significantly impacts the device characteristics, as can be seen from the transfer curves of p- and n- channel devices measured before and during application of 1.5 mN force, **Figs. 2(a)-(b)**. After force application removal, both p- and n-channel devices completely recovered their pristine curves, showing that no damage was induced by the nanoindenter tip. Channel stresses induced by a known applied force were computed using FEM for the case where the external force is exactly centered on the DUT. It was observed that, first, on current and threshold voltage demonstrate an expected MS-induced change that can be attributed to mobility and band gap modification under MS [8], [11], [31], [32]. The threshold voltage shifts extracted by the constant current method were larger than those extracted by the second derivative method, which can show that the mobility increase by effective mass reduction also contributes to the threshold voltage shift. Second, GIDL current showed an exponential increase with MS (up to 3 orders of magnitude at -1.3 GPa), as can be seen from **Figs. 2(c)-(d)** showing data obtained on 6 p- and n-channel devices, respectively. This effect could not be explained by the gate leakage, which remained under 0.5 nA regardless of the channel type, drain bias, and the presence of force (see **Figs. 2(a)-(b)**)

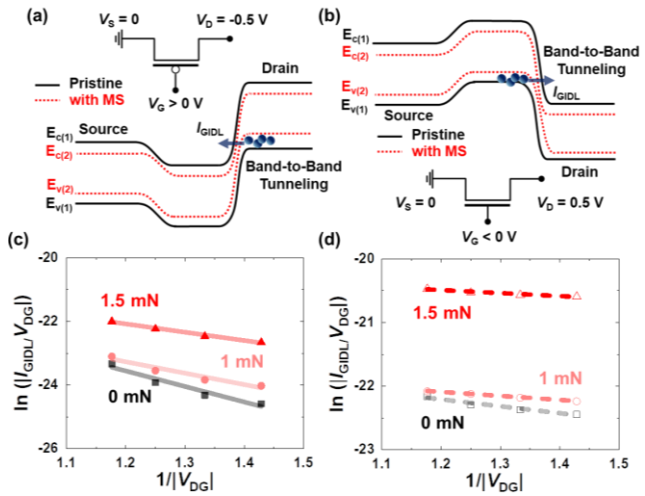

Fig. 3. Energy band diagrams of (a) p- and (b) n-channels in the accumulation region before and during application of the force at high V_D. ln(I_{GIDL}) as a function of V_{DG}^{-1} of (c) p- and (d) n-channels before and during application of the force (1 mN and 1.5 mN).

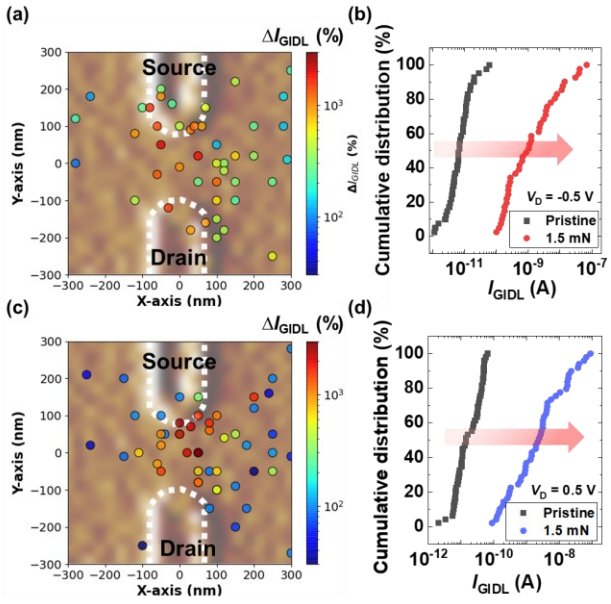

Fig. 4. The GIDL current-sensitivity maps of (a) p-channel and (c) n-channel according to the different MS indentation locations. ΔI_{GIDL} at $|V_D|$ = 0.5 V are the values calculated before and during the force application. The CDFs of I_{GIDL} before and during applying the 1.5 mN of force in (b) p- and (d) n- channels.

A. *Impact of MS on BTBT and GIDL currents*

The reported exponential increase in GIDL current with MS can be attributed to MS-induced change in the channel energy band gap and effective mass. According to previous studies on BTBT and GIDL current, I_{GIDL} can be expressed as [18], [24]–[26], [33]

$$I_{GIDL} = AE_S \exp\left[-\frac{\pi^2\sqrt{m^*}E_g^{\frac{3}{2}}}{\sqrt{2}qh}\frac{1}{E_S}\right], \quad (1)$$

where A is a preexponential constant, m^* is the effective mass, E_g is band gap, and E_S is the vertical electric field at the silicon surface. It is known that application of compressive MS shrinks the Si band gap, which leads to a decrease in the tunneling distance for electrons that travel from the valence to the conduction band *via* BTBT, as depicted in **Figs. 3(a) and (b)** [18], [24], [27], [33]. In addition, MS is also known to affect the effective mass of electrons [10]. Given the exponential dependence of GIDL current on the band gap and effective mass (Eq. 1), MS-induced decrease in those two parameters can explain the exponential increase in the GIDL current, observed in the presented study. Interestingly, as shown in **Figs. 3(c) and (d)**, the absolute values of the slopes of $\ln(I_{GIDL})$ as a function of V_{DG}^{-1}decreased as the mechanical force increased in both p- and n-channels. According to eq. (1), the corresponding band gap decrease was ~67 % and ~60 % for the p- and n-channels, respectively, when 1.5 mN of force was applied. However, (i) E_S is also affected by the band gap, therefore the fitting should strictly be performed using reciprocal functions, and (ii) the effective mass reduction included in the slope cannot be completely ignored. Overall, we conclude based on Figs. 3(c) and (d) that the band gap does decrease with increasing applied force, as expected, but further experiments with additional data are required to estimate the precise band gap changes with the applied MS.

B. *Strong GIDL currents directly above the channel*

The most MS-sensitive areas of the device can be identified using the GIDL current-sensitivity maps for p- and n-channel devices in **Figs. 4(a) and (c)**, respectively. For this purpose, the 1.5 mN force was *locally* applied at different locations in 54 identical devices located within 300 nm × 300 nm area around the channel. The GIDL current increase ΔI_{GIDL} was calculated as the percentage increase in I_{GIDL} at $|V_D|$ = 0.5 V during the force application relative to the value before force application.

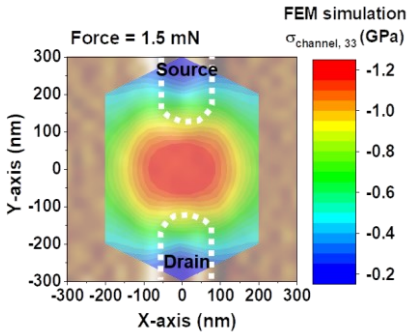

Fig. 5. Simulated channel stress values at the center of the channel as a function on the position where vertical force of 1.5 mN is applied (The shape of this simulated channel stress distribution is affected by metal interconnects and vias).

As can be seen from the measured maps, ΔI_{GIDL} is the largest around the channel in both the p- and n- channels. This is expected, because the greatest level of the stress is applied to the channel when the indentation position is located at the center of the channel as shown in **Fig 5**. Since the channel stress is highly dependent on various extrinsic factors (e.g., tip radius, thickness and properties of SiO_2, and metal layer), repeatable and comparable maps which directly reflect the channel stress can be a good guidance for strain engineering in the future. The cumulative distribution functions (CDFs) of GIDL current of p- and n-channel devices before and after applying the same 1.5 mN force, used in the GIDL current-sensitivity maps, are shown in **Figs. 4(b) and (d)**. The median values of the distribution increase by ~100 times in p- and n- channels, from 6.3 pA and 13.8 pA to 519 pA and 969 pA, respectively. As shown in *Section A*, the distributions of I_{GIDL} values in both p- and n-channels increase exponentially after the 1.5 mN of force is applied to DUTs.

IV. Conclusion

In this study, the impact of externally applied vertical compressive MS on gate-induced-drain-leakage (GIDL) current of short p- and n-channel CMOS transistors has been investigated. It was demonstrated that application of a GPa level mechanical stress (MS) induces an exponential increase in GIDL current. The observed effect can be attributed to MS-induced reduction of Silicon channel band gap and effective mass, leading to enhanced band-to-band tunneling (BTBT). In addition, GIDL current-sensitivity maps were extracted by applying local MS at different locations on 54 identical devices. It was demonstrated that the GIDL current increase is strongest when the MS is applied in the mid-channel regions of the

devices. The presented findings indicate the importance of MS control (especially in the channel region) for creating reliable low-leakage devices, required for low-power applications.

ACKNOWLEDGMENT

All the authors sincerely appreciate Jacopo Franco, Adrian Vaisman Chasin, Simon Van Beek, Andrea Vici, Joao Bastos, Kris Vanstreels, Yao Yao, Kristof Croes, and Dimitri Linten for discussions and advice. It has been in part supported by the European Commission under the 7th Framework Programme (Collaborative project MORDRED, contract No. 261868).

REFERENCES

[1] G. Eneman, E. Simoen, P. Verheyen, and K. De Meyer, "Gate Influence on the Layout Sensitivity of Si1−xGex S/D and Si1−yCy S/D Transistors Including an Analytical Model," *IEEE Trans. Electron Devices*, vol. 55, no. 10, pp. 2703–2711, 2008, doi: 10.1109/TED.2008.2003231.

[2] P. Hashemi, L. Gomez, and J. L. Hoyt, "Gate-All-Around n-MOSFETs With Uniaxial Tensile Strain-Induced Performance Enhancement Scalable to Sub-10-nm Nanowire Diameter," *IEEE Electron Device Lett.*, vol. 30, no. 4, pp. 401–403, 2009, doi: 10.1109/LED.2009.2013877.

[3] K. Lee, T. Fukushima, T. Tanaka, and M. Koyanagi, "3D integration technology and reliability challenges," *2011 IEEE Electr. Des. Adv. Packag. Syst. Symp. EDAPS 2011*, pp. 328–334, 2011, doi: 10.1109/EDAPS.2011.6213770.

[4] W. Guo *et al.*, "Impact of through silicon via induced mechanical stress on fully depleted Bulk FinFET technology," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 431–434, 2012, doi: 10.1109/IEDM.2012.6479066.

[5] G. Eneman *et al.*, "(Invited) Stress Simulations of Fins, Wires, and Nanosheets," *ECS Meet. Abstr.*, vol. MA2020-02, no. 24, pp. 1737–1737, 2020, doi: 10.1149/ma2020-02241737mtgabs.

[6] V. Cherman *et al.*, "Evaluation of mechanical stress induced during IC packaging," *Proc. - Electron. Components Technol. Conf.*, pp. 2168–2173, 2018, doi: 10.1109/ECTC.2018.00325.

[7] M. Gonzalez *et al.*, "Chip package interaction (CPI): Thermo mechanical challenges in 3D technologies," *Proc. 2012 IEEE 14th Electron. Packag. Technol. Conf. EPTC 2012*, pp. 547–551, 2012, doi: 10.1109/EPTC.2012.6507142.

[8] R. Degraeve, G. Groeseneken, I. De Wolf, and H. E. Macs, "The effect of externally imposed mechanical stress on the hot-carrier-induced degradation of deep-sub micron nMOSFET's," *IEEE Trans. Electron Devices*, vol. 44, no. 6, pp. 943–950, 1997, doi: 10.1109/16.585549.

[9] C. Claeys, E. Simoen, S. Put, G. Giusi, and F. Crupi, "Impact strain engineering on gate stack quality and reliability," *Solid. State. Electron.*, vol. 52, no. 8, pp. 1115–1126, 2008, doi: 10.1016/j.sse.2008.04.035.

[10] M. Chu, Y. Sun, U. Aghoram, and S. E. Thompson, "Strain : A Solution for Higher Carrier Mobility in Nanoscale MOSFETs," *Annu. Rev. Mater. Res.*, vol. 39, pp. 203–229, 2009, doi: 10.1146/annurev-matsci-082908-145312.

[11] K. Lee *et al.*, "Hot-Electron-Induced Punch-Through (HEIP) Effect in p-MOSFET Enhanced by Mechanical Stress," *IEEE Electron Device Lett.*, vol. 42, no. 10, pp. 1424–1427, 2021, doi: 10.1109/LED.2021.3104885.

[12] A. Kruv *et al.*, "On the impact of mechanical stress on gate oxide trapping," *2020 IEEE Int. Reliab. Phys. Symp.*, pp. 1–5, 2020, doi: 10.1109/IRPS45951.2020.9129541.

[13] J. Franco, B. Kaczer, A. Chasin, E. Bury, and D. Linten, "Hot electron and hot hole induced degradation of SiGe p-FinFETs studied by degradation maps in the entire bias space," *IEEE Int. Reliab. Phys. Symp. Proc.*, vol. 2018-March, pp. 5A.11-5A.17, 2018, doi: 10.1109/IRPS.2018.8353601.

[14] P. Su and J. J. Kuo, "On the Enhanced Impact Ionization in Uniaxial Strained p-MOSFETs," *IEEE Electron Device Lett.*, vol. 28, no. 7, pp. 649–651, 2007, doi: 10.1109/LED.2007.900297.

[15] T. Irisawa, T. Numata, N. Sugiyama, and S. I. Takagi, "On the origin of increase in substrate current and impact ionization efficiency in strained-Si n- and p-MOSFETs," *IEEE Trans. Electron Devices*, vol. 52, no. 5, pp. 993–998, 2005, doi: 10.1109/TED.2005.846344.

[16] P. G. Der Agopian, C. C. M. Bordallo, E. Simoen, C. Claeys, and J. A. Martino, "Stress engineering and proton radiation influence on off-state leakage current in triple-gate SOI devices," *Solid. State. Electron.*, vol. 90, pp. 155–159, 2013, doi: 10.1016/j.sse.2013.02.037.

[17] W. Yang, G. Qin, X. Shao, Z. Yu, and L. Tian, "Analysis of GIDL dependence on STI-induced mechanical stress," *2005 IEEE Conf. Electron Devices Solid-State Circuits, EDSSC*, pp. 769–772, 2005, doi: 10.1109/EDSSC.2005.1635390.

[18] T. Y. Chan, J. Chen, P. K. Ko, and C. Hu, "The Impact of Gate-Induced Drain Leakage Current on MOSFET Scaling," *1987 Int. Electron Devices Meet.*, pp. 718–721, 1987, doi: 10.1109/IEDM.1987.191531.

[19] A. O. Adan and K. Higashi, "OFF-State Leakage Current Mechanisms in BulkSi and SOI MOSFETs and Their Impact on CMOS ULSIs Standby Current," *IEEE Trans. Electron Devices*, vol. 48, no. 9, pp. 2050–2057, 2001, doi: 10.1109/16.944195.

[20] N. S. Kim *et al.*, "Leakage current: Moore's law meets static power," *Computer (Long. Beach. Calif).*, vol. 36, no. 12, pp. 68–75, 2003, doi: 10.1109/MC.2003.1250885.

[21] X. Yuan *et al.*, "Gate-Induced-Drain-Leakage Current in 45-nm CMOS Technology," *IEEE Trans. DEVICE Mater. Reliab.*, vol. 8, no. 3, pp. 501–508, 2008.

[22] T. Hoffmann *et al.*, "GIDL (Gate-Induced Drain Leakage) and parasitic schottky barrier leakage elimination in aggressively scaled HfO2/TiN FinFET devices," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, vol. 2005, no. 1, pp. 725–728, 2005, doi: 10.1109/iedm.2005.1609455.

[23] T. Y. Chan, P. K. Ko, C. Hu, and C. Sciences, "The impact of gate-induced drain leakage current on MOSFET scaling," *Int. Electron Devices Meet.*, pp. 718–721, 1987, doi: 10.1109/IEDM.1987.191531.

[24] N. Lindert, M. Yoshida, C. Wann, and C. Hu, "Comparison of GIDL in p+-poly PMOS and ns-poly," *IEEE Electron Device Lett.*, vol. 17, no. 6, pp. 285–287, 1996, doi: 10.1109/55.496459.

[25] S. Gundapaneni, M. Bajaj, R. K. Pandey, K. V. R. M. Murali, S. Ganguly, and A. Kottantharayil, "Effect of band-to-band tunneling on junctionless transistors," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 1023–1029, 2012, doi: 10.1109/TED.2012.2185800.

[26] J. Chen, T. Y. Chan, I. C. Chen, P. K. Ko, and C. Hu, "Subbreakdown Drain Leakage Current in Mosfet.," *IEEE Electron Device Lett.*, vol. 8, no. 11, pp. 515–517, 1987, doi: 10.1109/edl.1987.26713.

[27] X. Yuan *et al.*, "Gate-Induced-Drain-Leakage Current in 45-nm CMOS Technology," *IEEE Trans. Device Mater. Reliab.*, vol. 8, no. 3, pp. 501–508, 2008, doi: 10.1109/TDMR.2008.2002350.

[28] T. Wang, S. Member, T. Chang, and L. Chiang, "Investigation of Oxide Charge Trapping and Detrapping in a MOSFET by Using a GIDL Current Technique," *IEEE Trans. Electron Devices*, vol. 45, no. 7, pp. 1511–1517, 1998, doi: 10.1109/16.701482.

[29] W. C. Oliver and G. M. Pharr, "An improved technique for determining hardness and elastic modulus," *Journal of Materials Research*, vol. 7, no. 06. pp. 1564–1583, 1992, doi: https://doi.org/10.1557/JMR.1992.1564.

[30] O. O. Okudur, K. Vanstreels, I. De Wolf, and U. Hangen, "Extraction of elastic modulus of porous ultra-thin low-k films by two-dimensional finite-element simulations of nanoindentation," *J. Appl. Phys.*, vol. 119, no. 2, p. 025302, 2016, doi: 10.1063/1.4939284.

[31] C. S. Smith, "Piezoresistance effect in germanium and silicon," *Phys. Rev.*, vol. 94, no. 1, pp. 42–49, 1954, doi: 10.1103/PhysRev.94.42.

[32] C. Gallon, G. Reimbold, G. Ghibaudo, R. A. Bianchi, and R. Gwoziecki, "Electrical analysis of external mechanical stress effects in short channel MOSFETs on (0 0 1) silicon," *Solid State Electron.*, vol. 48, pp. 561–566, 2004, doi: 10.1016/j.sse.2003.09.024.

[33] T. Endoh, R. Shirota, M. Momodomi, and F. Masuoka, "An Accurate Model of Subbreakdown Due to Bandto-Band Tunneling and Some Applications," *IEEE Trans. Electron Devices*, vol. 37, no. 1, pp. 290–296, 1990, doi: 10.1109/16.43828.