An Injection-Locked Ring-Oscillator-Based Fractional-N Digital PLL Supporting BLE Frequency Modulation

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***Abstract*—This paper presents an injection-locked (IL) ring-oscillator-based fractional-N digital PLL (DPLL) supporting BLE frequency modulation with an FSK error between 2.4% and 3.3%. As the fractional spur cannot be suppressed by IL-DPLL, this work proposes a random edge injection (REI) to reduce the spur. This technique also speeds up the convergence time of the gain calibration of the digital-to-time converter (DTC). Furthermore, the proposed background calibration schemes allow the DPLL to achieve stable performance across all BLE channels, including both integer-N and fractional-N channels. This work was fabricated in 40-nm CMOS technology occupying a 0.09-mm^2 area. A fractional spur of -44 dBc and a reference spur of are achieved while consuming 2.76 mW when REI is activated. The background calibrations also ensure stable performance across BLE channels.**

***Index Terms*—Bluetooth, injection locking, ring oscillator, fractional-N DPLL, FSK modulation.**

I. Introduction

BLUETOOTH Low Energy (BLE) is widely deployed in Internet-of-Things (IoT) applications. A phase-locked loop (PLL) that can simultaneously synthesize the desired carrier frequency while supporting frequency modulation is typically required in a BLE system. Most of the PLLs in BLE transceivers adopt an LC oscillator to obtain low phase noise to fulfill the required frequency modulation quality. However, it usually occupies a large part of the total die area of the transceiver. It is preferred to replace the LC oscillator with a small-area oscillator, e.g., a ring oscillator (RO) for cost reduction.

ROs usually have around 20 dB lower Figure of Merit (FoM) than LC oscillators, due to their poor phase noise [1]. Injection-locking (IL) techniques have been widely used to suppress phase noise of ROs in an energy-efficient manner, since IL techniques can theoretically suppress phase noise of the oscillators up to 0.4 times the injection frequency. Recently several new IL techniques have been introduced [2][3], but they are restricted to integer-N mode only, which cannot support Gaussian-FSK (G-FSK) modulation in BLE. Nowadays, several digital frequency synthesizers are implemented to fulfill this need by applying two-point modulation [4]. This technique requires an injection-locked digital PLL (IL-DPLL) to be able to operate in fractional-N mode and control precisely the timing of the injection signal in order to avoid high jitter and spurs degrading FSK error.

Furthermore, there are several limitations in adopting IL-DPLLs for BLE. First, fractional spurs due to nonlinearities in the analog blocks cannot be effectively filtered in IL-DPLLs because of their high bandwidth due to IL [5][6], which leads to higher fractional spur level. High fractional spurs degrade the frequency modulation quality when the IL-DPLL is operated at integer channels (e.g., 2432 MHz with f_{REF} of 64 MHz) and the high RMS jitter degrades the modulation quality in fractional channels. Second, the frequency mismatch between the free-running frequency and the target frequency of the oscillator, and the static timing offset (STO) between the injection path and the PLL increase the level of reference spurs. According to [7], the reference spur level can be estimated as

$$Spur_{REF} = 20log10(t_{OS} * f_{OUT}), \tag{1}$$

$$Spur_{REF} = 20log10(f_{ERR}/f_{INJ}), \tag{2}$$

where t_{OS}, f_{OUT}, f_{ERR} and f_{INJ} represent the static timing offset, the output frequency, the frequency error and the injection frequency. At 0-dBm output power, the spurious need to be at least below -41.3 dBc to fulfill the FCC requirements.

To suppress injection spurs caused by different mismatches mentioned above, several techniques are published in recent years. Soft-injection technique [8] has been published to reduce the level of spurs but the noise suppression from the injection is limited. In [9], a frequency-locked loop (FLL) is implemented to compensate for the frequency mismatch between the oscillator and the reference, but the convergence time is long for small frequency mismatch. In [10], dual-loop IL-PLL is applied and a PLL with a replica oscillator is running in parallel with the IL path to track the frequency error continuously. These two oscillators share the same control from the PLL. However, the replica oscillator consumes the same amount of power as the main oscillator and the mismatch between these two oscillators limits the accuracy of the frequency tuning. To avoid using two oscillators, some works combine the PLL and the injection path. In [11][12], the phase or time offset between the PLL and the injection path is compensated by a delay line. Unfortunately, these are foreground calibrations that cannot tune the offset on time if the voltage and temperature change during BLE packets. In [14], the injection will be gated every several reference cycles, which allows the PLL to track the frequency drift.

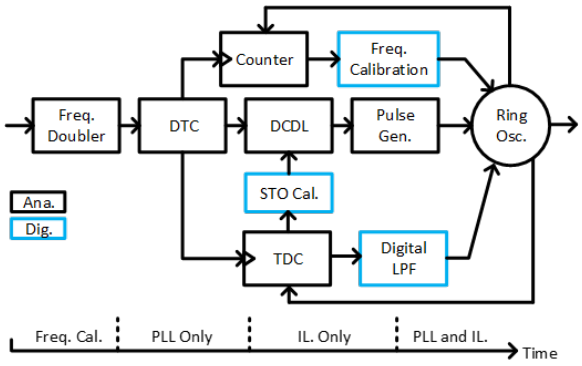

Fig. 1. Proposed injection-locked RO-based DPLL.

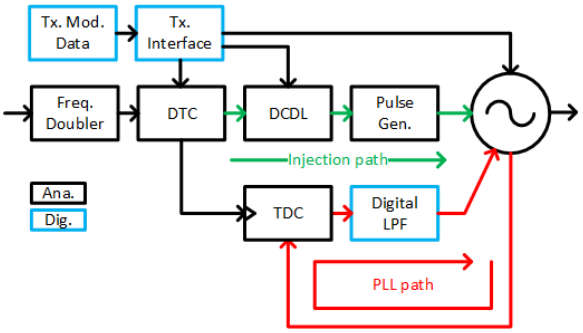

Fig. 2. The proposed injection-locked DPLL with Tx module.

However, it is difficult to balance the effectiveness of the PLL and the injection path for the optimization between the level of reference spurs and the jitter. In [15], a background two-point calibration is proposed to track the frequency drift and compensate for the offset. However, the digital power consumption of this work is high which is not suitable for low power applications.

In this work, three techniques have been proposed to address the challenges mentioned above. (1) A random edge injection (REI) will be proposed to suppress fraction spurs, which also reduce FSK error. (2) Continuous digital background calibrations will be introduced for consistent jitter and spur performance over integer and fractional modes. (3) An injection-locked DPLL with a Tx module will be proposed to isolate the supply pull effect from the modulation.

The rest of this article is organized as follows. In Section II, the architecture of frac-N IL-DPLL will be described. The implementation of the RO will be discussed in Section III and measurement results will be shown in Section IV. Finally, Section V presents conclusions that were made based on this work.

II. The Proposed Fractional-N IL-DPLL-Based Frequency Synthesizer

A. Architecture Overview

Fig. 1 shows the proposed architecture of fractional-N IL-DPLL. IL-ROs usually achieve better phase noise performance with a higher reference clock frequency, as the noise of the reference path dominates the in-band phase noise. However, the reference frequency of the BLE transceivers typically is in the tens of megahertz range. In this proposed work, a 64-MHz XO and the technique of doubling reference clock [16] are adopted. The effective reference frequency of the DPLL and the injection path is doubled by a frequency doubler which increases the noise suppression bandwidth in a power-efficient way. The proposed IL-DPLL works as follows: first, it uses a counter to count the number of edges of the RO in one reference clock to coarsely tune the RO close to the targeted frequency. Then, the counter is shut down to save power and a fine-tuning of the RO frequency starts correcting the phase error between the RO edge and the delayed reference edge from the digital-to-time converter (DTC), which is measured by a self-gated time-to-digital converter (TDC) [17]. During the 'PLL only' phase, the TDC output represents the phase error of the oscillator and with a digital low pass filter (LPF), the phase of the oscillator gradually aligns with the delayed reference. Next, the injection path is enabled while the PLL is frozen temporarily to avoid racing conditions between these two paths. During the 'injection-locked only' phase, the TDC output represents the time offset between the oscillator and the injection signal. Based on the TDC output, the delay of the digital-controlled delay line (DCDL) is tuned to reduce the STO [12]. Finally, the PLL and the injection path are activated at the same time while the STO calibration is running in the background to decrease the level of the reference spurs by reducing the phase offset between the injection path and PLL. During a warm start, the frequency calibration phase and the 'injection-locked only' phase can be omitted to reduce the lock time.

Fig. 2 describes the active blocks of the proposed IL-DPLL when the DPLL is in the transmission mode. The transmission data is sent to not only the DPLL but also the injection path. At the same time, the DCO frequency is tuned based on the transmission data [18], which causes a phase difference between the DPLL and the injection path. As the injection path dominates the control of the DCO phase and the frequency of the DCO will be modulated, it requires an accurate delay control of this path. By calculating the phase difference during the modulation, the delay control mentioned above tunes the setting of the DTC and the DCDL precisely. Please note that, delays in different modulation paths are equalized by digitally programmable delay. Since they are implemented in digital domain, the delay mismatch can be easily predicted and compensated. Furthermore, the DCO gain calibration is a least-mean-square-based (LMS-based) estimator. The benefit of keeping the DPLL activated during the frequency modulation is that the RO can withstand sudden supply pulling,e.g., due to the power amplifier. The delay mismatch for different control wires may degrade the modulation quality [18]. To minimize the mismatch, these signals are retimed at the digital-to-analog interface before sending to the DCO with a maximum data line skew on this interface which is in the order of tens of picoseconds. Furthermore, the frequency banks of the DCO with a row-column-based structure [19] are implemented in order to limit the impact of the data line skew at most a few LSBs. The worst skew results in a modulation error at the

output of the DCO less than 0.01 degree, which is below the noise level at the output of the DCO.

Several non-idealities degrade the modulation quality of the IL-DPLL, including DTC gain mismatch, XO duty cycle error, and two-point modulation gain mismatch. First, the jitter and fractional spur level will increase if the gain of the DTC is not properly calibrated. Recently, several DTC gain calibrations have been proposed and implemented in fractional-N digital PLLs [14][15][20][21][22][23] and an LMS-based background DTC gain calibration in an frac-N IL clock multiplier has been introduced in [14]. Second, the technique of doubling reference frequency has been applied to suppress the noise of the DCO in a power-efficient way, but the duty cycle error of the XO can degrade jitter performance [3][16]. Finally, because two-point modulation is applied in TX mode, a gain calibration between two paths is also needed [4]. These calibrations are preferred to perform in the background to accommodate to dynamic environment, such as temperature variation. However, background calibrations typically require a long convergence time [20][21], which increases energy consumption overhead during startup. To meet the modulation quality requirement in BLE while consuming low power, several background calibrations have been designed in this work which will be explained in detail in Section. II-C.

A simplified noise model has been built to have a better understanding of the noise contribution from different blocks. In Fig. 3, there are two main paths contributing to the output noise, $\phi_{n,OUT}$. One is from the blocks running at reference frequency $\phi_{n,REF}$, such as the XO and the DTC and these noise sources will be up-converted first and added to $\phi_{n,OUT}$ after a zero-order hold function. The other one is from the oscillator $\phi_{n,DCO}$ which will be added to $\phi_{n,OUT}$ after injection-locking. The noise of the TDC after a digital low pass filter can be considered as part of the $\phi_{n,OUT}$. Based on [24], the noise transfer function of $\phi_{n,REF}$ and $\phi_{n,DCO}$ are

$$NTF_{REF}(f) = N \times e^{\frac{-i2\pi f}{2f_{ref}}} \times sinc(\frac{f}{f_{ref}}), \quad (3)$$

$$NTF_{DCO}(f) = \frac{2N-1}{N} \times \frac{(\frac{f}{f_{BW}})^2}{1+(\frac{f}{f_{BW}})^2}, \quad (4)$$

where N is the up-conversion ratio from the reference frequency to the RF frequency and f_{ref} is the reference frequency. f_{BW} is the noise suppression bandwidth due to injection,

$$f_{BW} = 0.39 \times \beta \times f_{ref}, \quad (5)$$

where β is the injection strength, typically smaller than 0.5. From these equations, the requirements of the analog blocks could be defined, such as the phase noise of the oscillator, the XO and the DTC, and the resolution of the DTC. Using the equations above, the phase noise requirements of the critical paths could be estimated to achieve certain noise requirements. To achieve less than 2.5 ps integrated RMS jitter, the phase noise of the reference path and the DCO are set to be less than -136 dBc/Hz and -112 dBc/Hz at 10 kHz and 10 MHz offset frequency respectively and the resolution of the DTC is 1.5 ps. Please note that, the delay range of the DTC needs to cover at least one period of the DCO for frac-N operation, and therefore a 9-bit DTC with 1.5 ps step size is required.

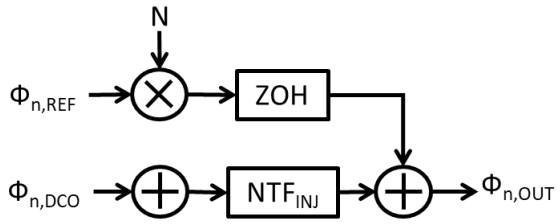

Fig. 3. Simplified system noise model.

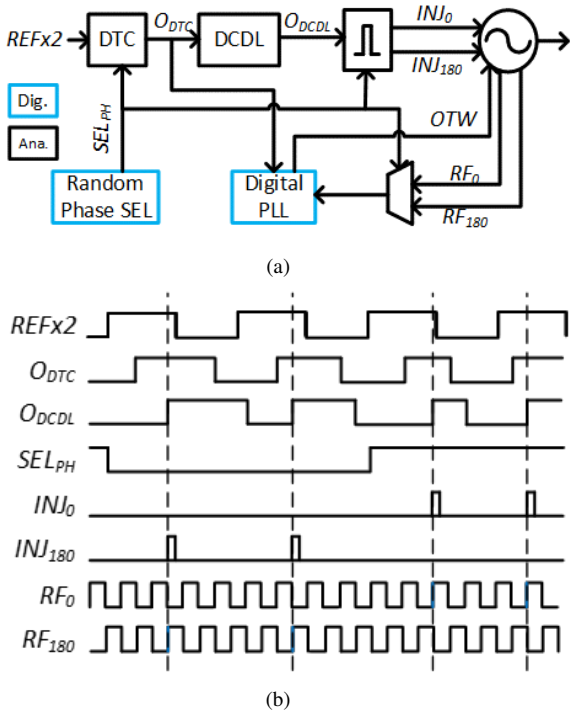

Fig. 4. (a) Block diagram of random edge injection, (b) timing diagrams of random edge injection.

B. Random Edge Injection

In [17], a phase dithering technique is introduced to power-efficiently reduce the power of fractional spurs by scrambling the nonlinearity pattern of the DTC. However, such an approach does not apply to IL-DPLLs because the DPLL keeps aligning the phase between the output of the DTC and the output of the multiplexer (MUX) and if the DTC output is directly used to generate the injection pulses without any compensation for the random pattern, the injection pulses will sometimes be sent to the opposite RO edge, introducing huge disturbances to the oscillator and causing large spurious.

Hereby, an REI technique in Fig. 4(a) is proposed to suppress fractional spur for IL-DPLLs. The DPLL aligns the output of the DTC, O_{DTC}, with rising edges of RF_{180} when the phase select signal, SEL_{PH}, is high and with rising edges of RF_0 when SEL_{PH} is low. To ensure the

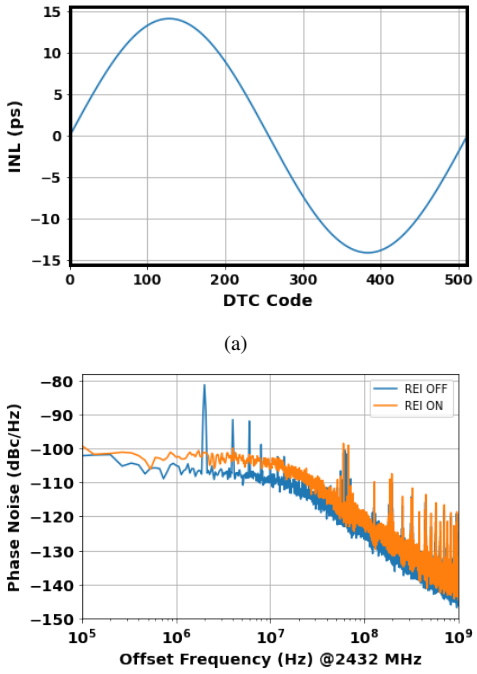

Fig. 5. Simulated fractional spur level. (a) Model DTC INL, (b) simulated fractional spur levels when REI technique is on and off.

polarity of the injection signal, the injection pulse of INJ_0 is generated if SEL_{PH} is high otherwise the injection pulse of INJ_{180} will be generated. At the same time, the control of the DCDL is tuned according to the digital RF duty-cycle and STO calibrations, which will be explained later. The timing diagrams of the related signals of the REI technique are shown in Fig. 4(b).

Simulations are performed to validate the effectiveness of the REI technique. A sinusoidal-shape integral nonlinearity (INL) which is ± 10 LSB, shown in Fig. 5(a), is added into a 9-bit DTC in the system model. Please note that, the INL of the designed DTC in the simulation is around ± 1.5 LSB. The DPLL is programmed to lock at 2434 MHz which is one of the BLE channels. After the system is in a stable state, the phase of the oscillator has been recorded for around 100 μs and the spectrum of the output can be plotted based on the recorded phase information of the IL-DPLL output. In Fig. 5(b), it can be observed that the fractional spurs are reduced by 20 dB when the REI technique is enabled and the phase noise is dominated by the noise of the oscillator. By enabling the proposed REI, the phase noise increases if the INL of the DTC is large but the overall integrated jitter remains the same as the power of the fractional spur will spread across the spectrum.

C. Background Calibrations with the Proposed REI Technique

The proposed REI technique requires a 50% duty cycle of the RF signal as the injection signal injects sometimes at one phase or another. Thus, a DCO duty cycle calibration is implemented, shown in Fig. 6. The product of the phase selection signal and the phase error from the TDC output will be accumulated. The accumulated value will be multiplied

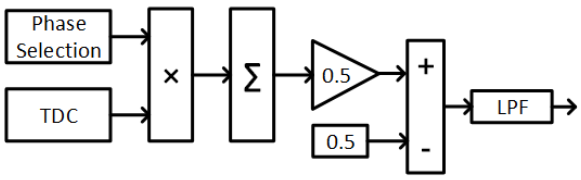

Fig. 6. Block diagram of DCO duty cycle calibration.

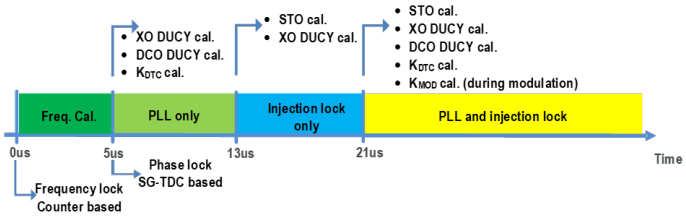

Fig. 7. Sequence of calibrations during locking procedure.

by 0.5 and then 0.5 is added. A digital LPF filters out the high-frequency components. If the duty cycle is not 50%, the output of the LPF will shift away from 0.5 indicating the direction and the amount of the duty cycle error in the loop. Please note that there are two kinds of DCO duty cycle error in the loops: one is the intrinsic error of the oscillator and the other is the error caused by the feedback buffers from the oscillator to the TDC. Based on the calibration output, the duty cycle error will be compensated by the delay code applied to the DTC. A MUX has been employed to select different phases of the DCO for the REI technique, and to simulate the potential delay difference between these two phases, a Monte Carlo simulation has been performed. The simulation with 100 runs shows the delay standard deviation of the MUX is approximately 1 ps. However, this error can be considered as the error caused by the feedback buffer mentioned above and can be compensated by the DCO duty cycle calibration. The implementation of the XO duty cycle calibration is similar to the one for DCO duty cycle. In simulation, the XO duty cycle error up to 10% can be calibrated. Please note that, the TDC is driven to early-late detection when the calibrations are settled. Therefore, the TDC resolution has little impact on the spur level.

The convergence time of the DTC gain calibrations [20][21] typically takes more than tens of microseconds, increasing the lock time of the PLLs. Thanks to the proposed REI technique, the convergence time of the calibration is shorter and independent of the fractional part of the frequency control word (FCW). The REI technique breaks the period pattern of the DTC control which normally depends on the fractional part and amplifies the DTC gain error which leads to a faster convergence time of the calibration loop. Furthermore, the REI technique enables the DTC gain calibration to converge with a wider range of the DTC gain error. Without the REI technique, the initial setting of the DTC gain cannot be more than 20% off from the correct setting.

Fig. 7 shows the sequence of calibrations during the locking procedure. During the 'PLL only' phase, the gain of the

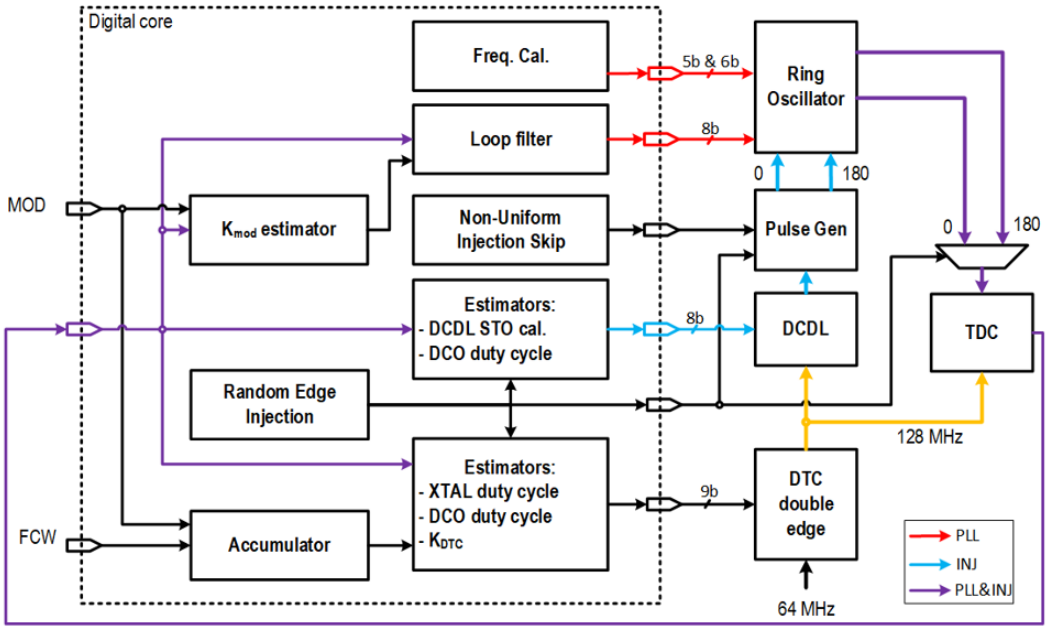

Fig. 8. Detailed block diagram of the proposed IL-DPLL.

DTC and the duty cycle error of the XO and oscillator can be calibrated based on the output of the phase detector, which is the TDC in this work. The TDC output indicates different duty cycle errors, depending on which edges (either rising or falling) of the XO and the DCO are selected. After a timeout counter is finished, the IL-DPLL moves to the 'injection-locked only' phase. The STO calibration and the XO duty cycle calibration are activated as DCO duty cycle calibration and the DTC gain calibration has been settled. After this, the imperfections in the PLL have been calibrated. Finally, the finite state machine (FSM) turns on the PLL again while the calibrations keep running simultaneously. Note that only one TDC is adopted for phase detection and calibrations to minimize the power and area overhead, and the FSM properly schedules the calibrations to avoid any racing conditions. For example, the TDC output contains the duty cycle error of the XO if positive edge of the RF signal and negative edge of the XO are selected, or contains the duty cycle error of the RF signal if the negative edge of the RF and positive edge of the XO are selected. The detailed block diagram of the proposed IL-DPLL including the calibration loops is shown in Fig. 8. In order to further improve the spur performance, non-uniform injection skip has been implemented. Instead of skipping the injection for PLL with every fixed number of reference cycles [14], the numbers of the injection skip change during the operation. In the DTC and the DCDL, the tunable delay is implemented by an RC-based structure with switched capacitors [25]. The resolution of the TDC is around 15 ps and the linearity is not critical as the TDC output only toggles one or two steps with the help of the DTC.

III. Frequency Tuning of RO with PSRR Improvement

Fig. 9 shows the implementation of the RO core and the output of the current banks is connected to four delay units in

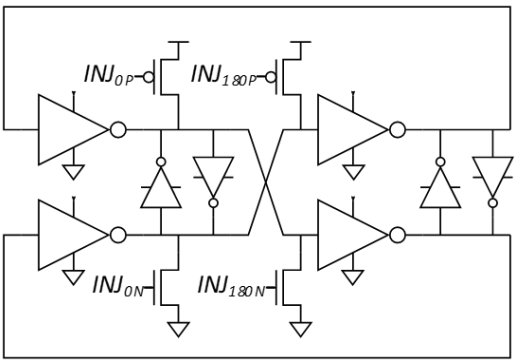

Fig. 9. Schematic of RO core.

the core. Based on the phase of injection, the pulse generator injects a pair of differential pulses to the core. The frequency of the RO is controlled by tuning the sinking current of a current-DAC which is shown in Fig. 10. It consists of a low-dropout regulator (LDO) and a current-DAC that splits into coarse, medium and fine banks. The LDO generates a reference voltage for the current-DAC. This reference voltage is converted to a current inside the coarse bank defining the LSB current of the coarse bank. The coarse bank sources a static bias current to the RO to set the minimum operating frequency of the RO. In addition to the static bias current, a 5-bit bank is used for coarse tuning the RO. A single LSB cell of the coarse bank is used as a reference for the medium bank. To increase the settling behavior of the RO, the medium (6-bit) and fine bank (8-bit) are implemented as current-sinking banks subtracting current from the bias current sources by the coarse bank. The frequency steps of the coarse, medium and fine banks are 44.5 MHz, 1.76 MHz and 28 kHz. Please note that, there is a digital module monitoring the control of the fine bank. When the control approaches the boundary, the

medium bank will change one step to avoid the tracking bank saturating.

An LDO is implemented to make the RO less susceptible to supply variation [26]. The reference voltage, V_{LDO}, is forced over a fixed resistor converting it to a current reference defining the LSB current step in the coarse bank. To keep a fixed ratio between coarse, medium and fine frequency step, the reference current generated by the LDO is passed from a coarse bank to a medium bank with a fixed division ratio. The phase noise of the RO with different supply noise is shown in Fig. 11.

To avoid the quantization noise of the frequency step of the RO in the fine bank, the current step of the fine bank needs to be small enough. However, the RO will have a long settling time when the control of the fine bank changes. To improve the settling behavior, the current sources of the medium and fine banks are implemented as current sources that subtract the current from the coarse bank current. The inactive current sources are switched to a dummy branch, which can avoid charging or discharging the internal nodes of the current unit. Thanks to the dummy branches, the DCO settles in 40 ns with a frequency accuracy of 1%.

IV. Measurement Results

The proposed IL-DPLL is implemented in 40-nm CMOS technology and it occupies an active area of 0.09 mm^2, which is shown in Fig. 12. This work consumes 2.76 mW and the power breakdown is shown in Fig. 13. The power consumption of the digital can be reduced by 40% if the background calibrations are frozen.

Fig. 14 shows the measured free-running RO frequency across different frequency control codes in different voltage supplies. The supply sensitivity is about 6%/V when the PVT code is at the middle, which shows a large improvement in supply rejection compared to normal ring oscillators where it is typically larger than 100%/V. The supply voltage of the RO is 1 V in the measurements.

Fig. 15(a) shows the calculated and measured phase noise of the DPLL output at 2.434 GHz and the integrated RMS jitter is 2.1 ps and from the phase noise profile, it can be observed that the noise suppression bandwidth is around 10 MHz, indicating that the injection strength is around 0.2. The measured in-band phase noise is higher than the calculated profile based on Eq. (3) and Eq. (4), and we believe it is caused by the degraded injection strength. In Fig. 15(b), the integrated jitter across 40 BLE channels is shown and the same results over integer and fractional mode, which demonstrates the effectiveness of the background calibrations. Fig. 16 and Fig. 17(a) show the fractional spur at 2.434 GHz, where the fractional part is 2 MHz (closest to integer channels in the BLE channelization). The fractional and reference spurs of the proposed DPLL are -44 dBc and -50 dBc, which are measured at 2434 MHz respectively. The fractional spur level reduces by 10 dB when the REI technique is enabled. Fig. 17(b) shows that the phase noise does not increase and the in-band phase noise is lower when the REI is on. Fig. 17(c) shows the level of the measured fractional spur across BLE channels and the worst measured spur lelve is -44 dBc.

The settling behavior of this DPLL is shown in Fig. 18 and this DPLL settles within 22 μs from a cold start. It can be observed that the calibrations for the DTC gain, the duty cycle error of the XO and the RO, and the STO are quickly converged during Phase 1 (P1) and Phase 2 (P2). Fig. 19(a) shows the FSK error with and without the proposed REI technique by applying BLE compliant 1 MB/s GFSK modulation and the adjacent channel power ratio (ACPR) is shown in Fig. 19(b). In Fig. 19(c), the FSK error across all BLE channels is within a range between 2.4% and 3.3% when the supply of the PLL changes from 1.05 V to 1.15 V, showing the proposed IL-DPLL with background calibrations ensures it operates in optimal conditions regardless of the fractional- or integer-N modes. In order to show the effectiveness of the calibrations, the spur levels measured at 2440 MHz under different conditions are shown in Fig. 20 and the worst reference spur is -47 dBc.

The comparison with state-of-the-art RO-based PLLs is listed in Table I and the presented work achieves FoM of -245 dB by normalizing the reference frequency. Thanks to the calibration loops, this work meets the BLE specifications without requiring high-frequency XO. To the best of our knowledge, it is the first IL-DPLL supporting BLE frequency modulation with excellent modulation quality, while having low spur level to meet spectral regulations (e.g., FCC).

V. Conclusion

This paper presents an RO-based fractional-N IL-DPLL which supports BLE frequency modulation. A spur reduction approach based on random edge injection is proposed and it improves FSK error during the frequency modulation. The background calibrations are employed to ensure stable and robust performance across integer- and fractional-N channels.

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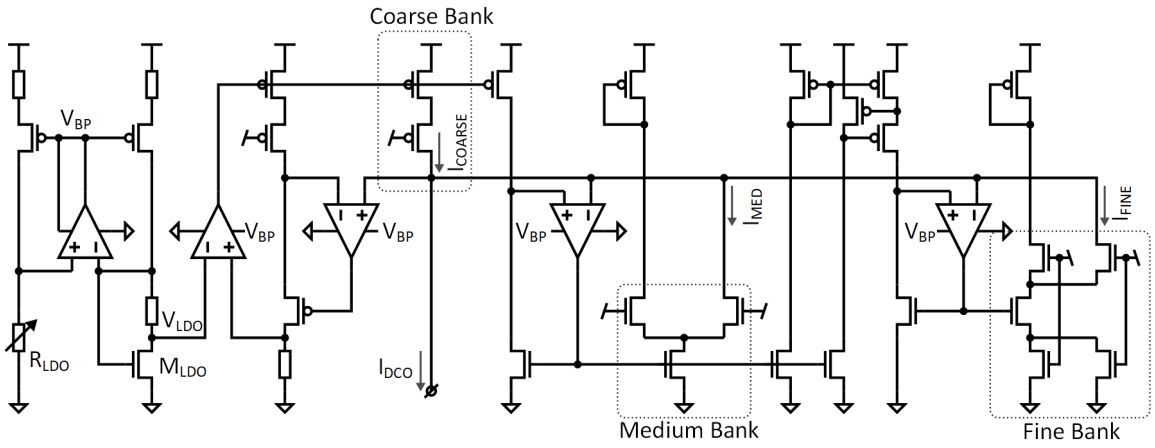

Fig. 10. Schematic of frequency tuning of RO with PSRR improvement.

TABLE I
COMPARISON WITH RING-OSCILLATOR-BASED FRACTIONAL-N DESIGNS

	This work	S. Levantino JSSC'15 [23]	J. Gong RFIC'18 [12]	A. Santiccioli JSSC'19 [28]	B. Liu CICC'19 [6]	T.Seong ISSCC'20 [29]	B. Liu SSC-L'20 [30]		S. Kundu JSSC'21 [13]	B. Liu TCAS-I'21 [5]	H. Park ISSCC'21 [31]
Oscillator Type	Ring	Ring	Ring	Ring	Ring	Ring	Ring		Ring	Ring	Ring
Type	IL	MDLL	IL	MDLL	IL	PLL	IL		MDLL	MDLL	PLL
Frac-N	Yes	Yes	Yes	Yes	Yes	Yes	Yes		Yes	Yes	Yes
Ref. Freq. (MHz)	64	50	64	100	40	100	40	100	80	100	100
Freq. Range (GHz)	1.8-2.7	1.6-1.9	1.8-2.7	1.3-3.0	0.9	4.5-6	0.4-1.5		1.2-3.8	0.6-1.6	5.2-6
Mult. Factor (N)	38	32	38	16	23	55	25	10	45	10	53
Frac. Spur (dBc)	-44	-47	-45.8	-51.5	NA	-58	-43.8	-44.3	-50	-61.9~-59.6	-63
Ref. Spur (dBc)	-47	-55.4	-43.6	-50	NA	NA	-37.1	-30.9	-56	-64.5	-77
Ref. Spur Cal	Background	Background	Foreground	No	Background	No	Background		Background	Background	No
Int. RMS Jitter (ps)	2.1	1.4	1.6	0.397	3.9	0.648	2.99	1.9	2.74	0.7	0.365
Int. BW	[10k-10M]	[30k-30M]	[10k-10M]	[30k to 30M]	[NA]	[1k to 30M]	[10k-10M]		[10k-100M]	[10k-40M]	[10k-30M]
Power (mW)	2.76	3	1.33	2.5	1.8	9.88	0.62	0.95	3.19	1.85	9.27
FOM* (dB)	-229.1	-232.3	-234.7	-244.0	-225.6	-233.8	-232.6	-234.6	-226.2	-240.4	-239.1
FoM_{REF}** (dB)	-244.9	-247.4	-250.5	-256.1	-239.2	-251.2	-246.5	-244.6	-242.7	-250.4	-256.3
Area (mm2)	0.09	0.4	0.13	0.0275	2.1***	0.108	0.0036		0.0052	0.126	0.146
Technology (nm)	40	65	40	65	65	65	5		22	65	65
Mod. Profile	GFSK	No	No	No	GM/FSK	No	Triangle/Sawtooth		No	No	No

*FOM=20*log10(Jitter/1s) + 10*log10(Power/1mW)
**Normalized to N, FoM_{REF}=10*log10[(jitter/1s)^2*(Power/1mW)/N][22]
*** Including TRx

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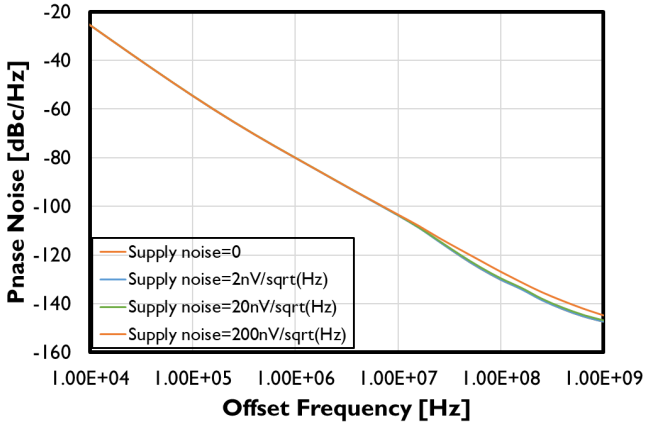


Fig. 11. Simulated RO phase noise with different supply noise.

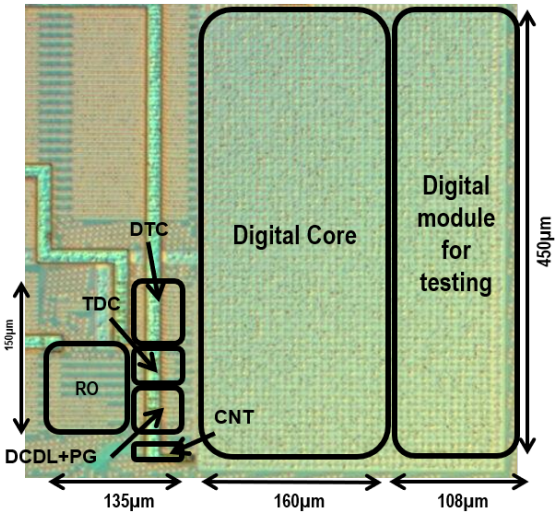


Fig. 12. Photograph of the prototype chip.

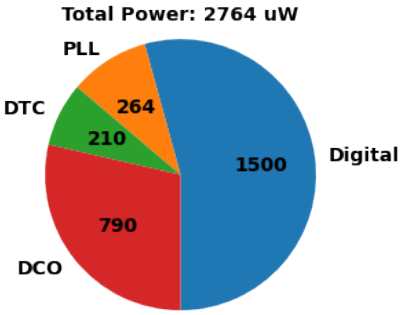


Fig. 13. Measured power breakdown.

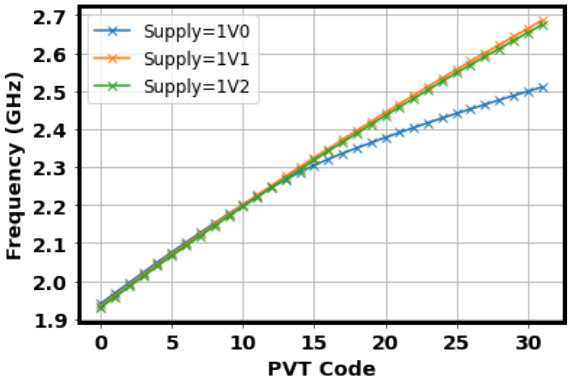
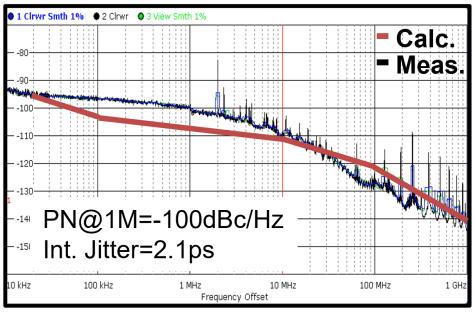
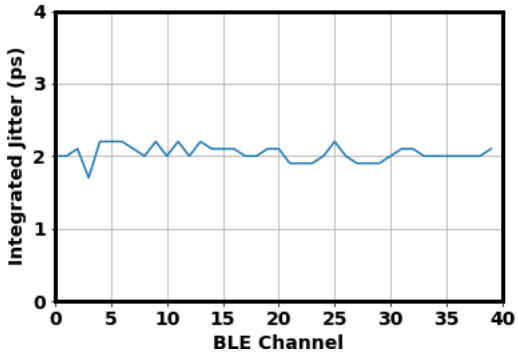


Fig. 14. Measured RO frequency in different supply conditions



(a)



(b)

Fig. 15. (a) Calculated and measured phase noise profile at 2434MHz. (b) Measured RMS jitter across BLE channels.

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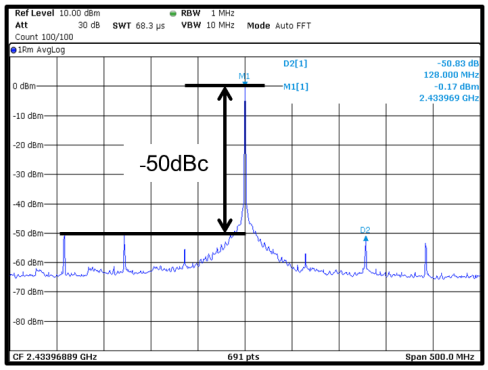

Fig. 16. Measured reference spur.

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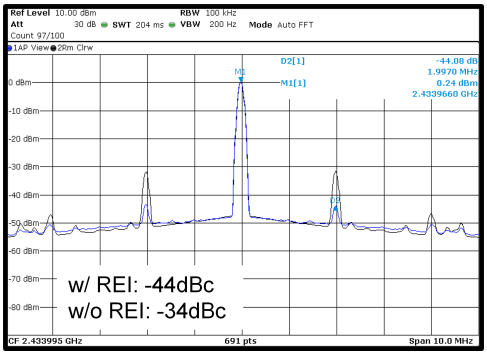
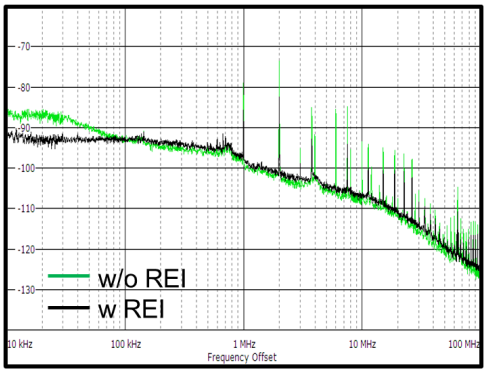
Yuming He received the B.S. degree in Optical Information and Technology from South China University, China, in 2012 and the M.S. degree in electronics engineering from Delft University of Technology, the Netherlands, in 2014.

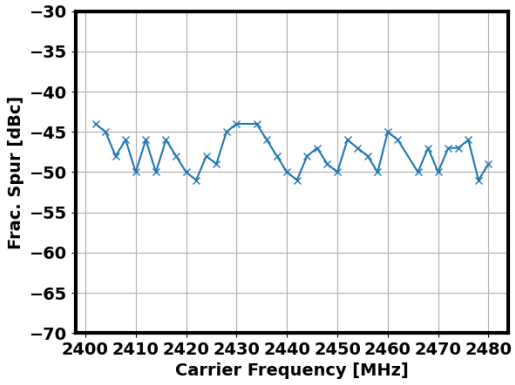
Since 2015, he joined Imec, the Netherlands, as a researcher. He is currently interested in energy- and area-efficient sensing systems for implantable neural interfaces.



(a)



(b)



(c)

Fig. 17. (a) Measured fractional spur when the REI is on and off. (b) Measured phase noise profile with and without REI. (c) Measured worst fractional spur across BLE channels.

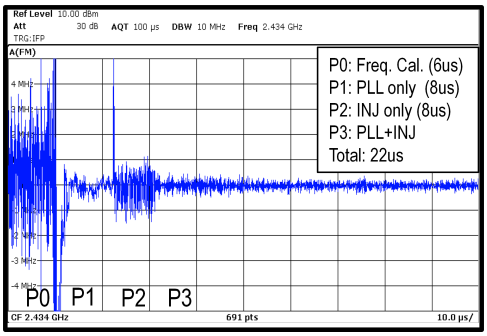
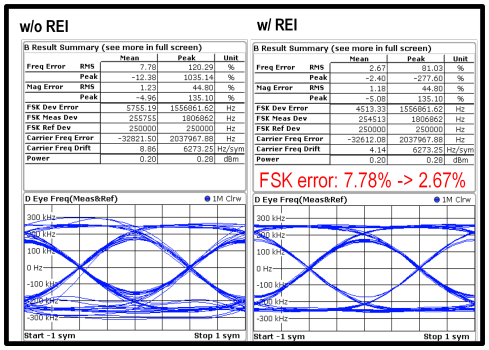
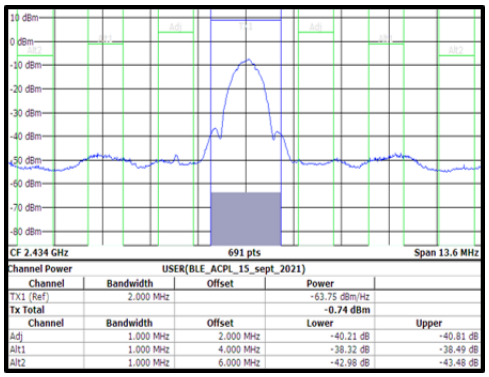


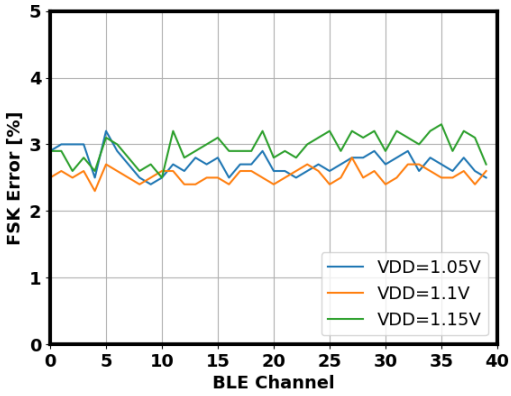
Fig. 18. Measured settling behavior from cold start.



(a)



(b)

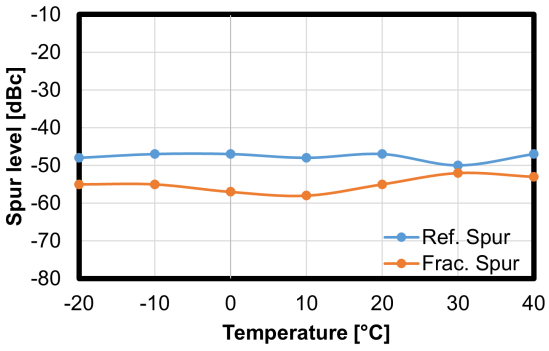


(c)

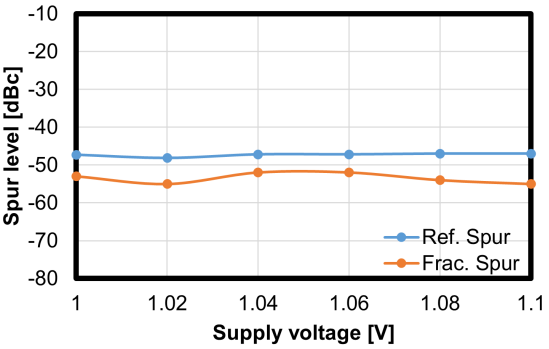
Fig. 19. (a) Measured eye diagram and FSK error. (b) Measured ACPR. (c) Measured FSK error across BLE channels in different voltage supply conditions.

Johan van den Heuvel was born on Febuary 5th 1981 in Oss, the Netherlands.

He received his M.Sc., and PhD degree in Electrical Engineering, from the Eindhoven University of Technology, the Netherlands, in 2006 and 2012 respectively. For his PhD thesis he was awarded the "Veder Prijs 2012". Currently, he works at imec-nl as principal member of the technical staff. His current research interests include all digital phase locked loops, low-power and high-speed mixed signal circuits and architectures, multiple antenna systems, ultra-wideband communication, channel measurements, and digital baseband algorithms.



(a)



(b)

Fig. 20. Measured spur level across different conditions.

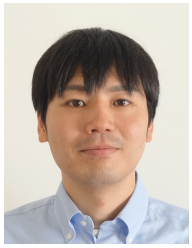
Paul Mateman received his Bachelor degree in Computer Technology from the Poly Technical school in Eindhoven (The Netherlands) in 1988 and his M.S. degree in Electrical Engineering from the Delft University of Technology (The Netherlands) in 1993. He has worked for Philips Research, Rockwell, NXP, ST Ericsson and nVidia, and joined Holst Centre/IMEC in 2014, where he works on Mixed Signal RF blocks (e.g. ADPLL)

Erwin Allebes joined IMEC in 2019 as an RF researcher where he is now involved in UWB radios and injection-locked frequency synthesizers. His research interests include ultra-low-power circuit design for IoT applications, digital PAs and frequency synthesizers/clock generators.

Stefano Traferro received the M.S. degree (cum laude) in electronics engineering from the Universita' degli Studi di Ancona (now Universita' Politecnica delle Marche), Ancona, Italy, in 1998. From June 2000 to June 2015, he worked at STMicroelectronics, Milan, Italy, as Digital Designer and the Project/Group Leader.

Since July 2015, he has been a Research and Development Engineer at Imec Netherlands, Eindhoven, The Netherlands. His main interests include low-power digital design and implementation, optimization techniques, and signal processing. He is an author of a couple of articles on the IEEE TRANSACTIONS ON OPTIMIZATION TECHNIQUES and a coauthor of a number of articles in various IEEE publications for his works in low-power digital designs.

Johan Dijkhuis received the M.S. degree in electrical engineering from the University of Twente in 1998. From 1998 he has worked as RF and analog design engineer for Philips Semiconductor, NXP, ST-Ericsson and NVIDIA. Since 2014 he works at Holst Centre / imec-NL. His research interests are ultra low power RF circuit design and power management circuits for ultra low power radios.



Keigo Bunsen received the B.E. and M.E. degrees in physical electronics from the Tokyo Institute of Technology, Tokyo, Japan, in 2009 and 2011, respectively. He joined Sony Corporation, Tokyo, in 2011, and Sony Semiconductor Solutions Corporation, Atsugi, Japan, in 2016, where he was involved in the research and development of analog/RF circuits and frequency synthesizers for wireless applications, including millimeter-wave communications, radar, and wireless power transfer systems. His current research interests include digital PLLs and analog-to-digital converters.

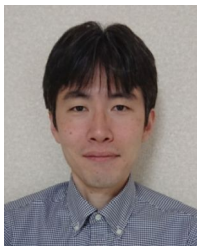
Peter Vis received the B. Eng. degree in electrical engineering from the AVANS University of Applied Sciences, 's-Hertogenbosch, The Netherlands, in 2005.

He worked for NXP semiconductors in and later for Synopsys on the development of interface IP. He joined imec in 2018 as an RD engineer. His current research interests include the design of ultra-low-power analog mixed signal ASICs for biomedical and IoT applications.

Arjan Breeschoten received his degree in computer technology in 1994. Until 2008 he worked within the semiconductor industry involved in research and development for ASICs in the Security, WiFi, WiMax and DECT application domains. In 2009, he joined Holst Centre/imec, Eindhoven, The Netherlands, where he focuses on system integration and project management for ultra low power wireless communications solutions.

Yao-Hong Liu is currently Scientific Director in imec. He is a recipient of a European Research Council (ERC) Consolidator grant and is the principal investigator of "Intranet of Neurons." His current research focuses on energy-efficient wireless and sensing technologies for implantable neural interfaces.

Dr. Liu received his Ph.D. degree from National Taiwan University, Taiwan, in 2009. He was with Terax, Via Telecom (now Intel), and Mobile Devices, Taiwan, from 2002 to 2010, developing Bluetooth, WiFi and cellular wireless SoC products. Since 2010, he joined imec, the Netherlands, and is leading the research of the ultra-low power wireless ASIC design for IoT and implantable applications. He served as a technical program committee of IEEE ISSCC, and currently serves in IEE RFIC symposium. He was a recipient of ISSCC 2020 Best System Demonstration Award.



Tomohiro Matsumoto joined Sony Corporation, Japan, in 2004. He has been engaged in research and development of analog and mixed-signal circuits for various applications.

Christian Bachmann obtained his Ph.D. in Electrical Engineering in 2011 at Graz University of Technology in Graz, Austria in a collaboration with Infineon Technologies. He joined imec in 2011, working on ultra-low-power DSP and wireless communication systems, digital baseband (DBB) processing, and hardware/software co-design. He is currently program director of imec's UWB and Bluetooth Secure Proximity programs, addressing RD challenges for high-accuracy, secure wireless localization with Bluetooth as well as Ultra-Wideband (UWB) and for advanced ultra-low power (ULP) RF wireless transceiver circuits enabling next-gen automotive, medical, and IoT applications.