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Direct bonding of low temperature heterogeneous dielectrics

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***Abstract*—Nowadays, the direct bonding process is embedded in a BEOL manufacturing process where the maximum temperature is $400°C$. For certain applications there is the need to lower such thermal budget. One of the first process steps which will be modified will be the bonding layer deposition step as well as the densification step. It is known that by lowering the deposition temperature the quality of the dielectric will be decreased as well. This change will have a direct consequence on the bonding process which relies on the quality of the dielectric.**

It is found that if we use a post bond anneal temperature which exceeds the densification temperature voids originate at the bonding interface. By means of FTIR studies and ERD analysis the origin of the voids is tentatively ascribed to H or H related species. These findings provide a basic understanding on how to tune the deposition condition to select a proper low temperature dielectric which will enable us to obtain a good bonding uniformity and a good bond strength for the described application.

***Keywords*-Direct wafer to wafer bonding; Low thermal budget; Voids formation; SiCN**

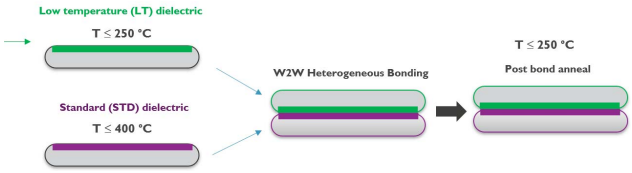

Figure 1. Process flow describing the experiments performed.

I. Introduction

Three-dimensional integrated circuits (3D-ICs) offer the possibility to solve delay and power problems in the conventional planar 2D-ICs. Different stacking options can be used to enable the use of the third dimension. One attractive option which allows the device stacking at room temperature and the possibility to reach high alignment accuracy is direct wafer to wafer bonding. Typically a post bond anneal step characterized by a temperature lower than or equal to $400°C$ is used to strengthen the adhesion between the bonded stack.

Memory applications are driving towards the reduction of process temperature [1], [2] meaning that an upper limit on the allowable temperature is imposed during deposition, densification and post bond anneal step.

In this work we run a first feasibility test to bond a standard (STD) SiCN dielectric deposited at $370°C$ to a dielectric deposited at temperatures lower than or equal to $200°C$. When we speak about STD dielectric for bonding applications within imec we refer to a SiCN material deposited at $370°C$. The so called "standard process steps" prior to bonding and the bonding process itself have been optimized for this material to obtain outstanding bonding results.

Two different kind of oxides have been selected; two nitrides and two silicon carbon-nitrides. For all the bonding experiments we use as device wafer a wafer where we deposit a low temperature dielectric and as carrier wafer a wafer where we deposit a standard SiCN dielectric. Afterwards the wafers are subjected to a densification step at a temperature lower than or equal to $250°C$. In a following step the wafers are planarized by using the same CMP process. Finally, the wafers are bonded by using the best-known method bonding sequence which includes a cleaning step and a N_2 plasma treatment prior to bonding. In order to complete the bonding process an annealing step is used to enhance the bond strength between the two bonded dielectrics.

Reducing deposition, densification and post bond anneal temperatures tends to go at the expense of the interface quality between the bonded dielectrics [3], [4]. Thus such changes in the process flow must be monitored by means of several characterization techniques enabling the selection of proper materials and integration flow, which can lead to defect-free and high enough bonding energy, ensuring final device reliability.

In this paper a simplified process flow is used to mimic the possible degradation of the interface quality which may occur when process temperatures are reduced to values lower than or equal to $250°C$. Different dielectrics as well as retuned and existing deposition, annealing and bonding processes have been fully characterized and explored by means of several characterization techniques being scanning acoustic microscopy (SAM), Fourier transform infrared derivative spectroscopy (FTIR), ellipsometry, electron recoil detection (ERD), transmission electron microscopy (TEM), energy-dispersive X-ray spectroscopy (EDS). Optimized processes and materials which enable a void free bonding with a

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relative high bond strength have been successfully demonstrated. Void formation mechanisms for the tested materials are proposed.

II. Experimental

For all the experiments a STD SiCN, deposited by PECVD at $375°C$, has been used as a bonding dielectric for the device wafer while as a bonding dielectric for the carrier wafer different dielectrics deposited at temperatures lower than or equal to $200°C$ were used, as described in Fig. 1.

Dielectric films were deposited by PECVD in three tools (A, B and C). We selected two kind of oxides (SiO_2A and SiO_2B), two nitrides (SiNA and SiNB) and two silicon carbon-nitrides (SiCNA and SiCNC) for 300 mm W2W bonding experiments.

For both SiCN materials NH_3 and $SiH_x(CH)_y$ have been selected as precursors. The remaining SiO_2 and SiN film types were deposited by using different precursors as summarized in Table I. The layers have been characterized by means of ERD analysis revealing atomic composition. In all the cases dielectric thickness was 150 nm with a total thickness variation $< 5\%$ to ensure a good co-planarity for bonding [5].

Table I
Main precursors used for SiO_2 and SiN film types

	SiO_2A	**SiO_2B**	**SiNA**	**SiNB**
Precursors	SiH_4	TEOS	NH_3	without NH_3

After deposition, the so-called densification step corresponds to a 2-hour annealing step which is used to remove outgas from the dielectrics. Such annealing process is done in pure N_2 atmosphere. In the case of STD SiCN, the temperature used is $350°C$ while for the low temperature (LT) dielectrics two different annealing temperatures $200°C$ and $250°C$ have been tested for this step. Chemical mechanical polishing (CMP) has been used to planarize the surface. AFM, with a scanning area of 4 μm^2, has been used to determine the surface roughness of each dielectric. FTIR has been employed after each process step to monitor the properties of the dielectrics and their evolution. The entire bonding sequence is realized in the EVG GEMINI cluster and it consists of the following steps: plasma activation in N_2 ambient, jet nozzle DI-water rinse, mechanical alignment and bonding at room temperature [6]. The quality of the bonding interface has been evaluated by means of SAM to identify void formation while the bond strength, established between the different combinations of dielectrics, has been evaluated by means of Maszara razor blade test. In some cases, in order to get more information regarding chemical bonding of interfacial layers, TEM together with EDS techniques have been employed.

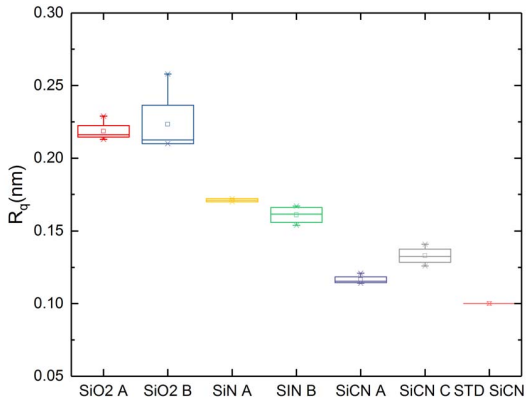

Figure 2. AFM results after CMP. Roughest materials are the SiO_2 ones while the smoothest are the SiCN ones.

III. Results and Discussion

A critical parameter to be monitored prio to direct bonding is the surface smoothness of the dielectric. R_q values expressed in nm are shown in Fig. 2 for all the dielectrics screened. As it is visible from the graph SiCN films exhibits the lowest roughness while the rougher films are the SiO_2 ones. Nevertheless the maximum R_q value measured for the various films is below 0.5 nm which is identified in many research reports as a maximum required surface roughness enabling optimum hydrophilic low temperature wafer direct bonding [7].

As explained previously the experiments were performed by tuning process temperatures of densification and post bond anneal steps. It has been observed that when deposition, densification and post bond anneal temperatures are kept below or equal to $200°C$, then we obtain good bonding uniformity for all the wafer pairs. However, bond strength results, reported in Fig. 3, point to a weak bonding which might be not fully compatible with subsequent thinning down techniques. On the same graph the bond strength achievable by bonding STD SiCN to STD SiCN, with post bond anneal equal to $200°C$, is reported, highlighting the significant difference in bond strength achievable when we use LT dielectrics.

With the aim of verifying whether we are able to improve these bond strength values, we increase the post bond anneal temperature to $250°C$, which is considered as an optimum post bond anneal temperature value in the standard process [8]. As a result, bonding voids with different shapes and patterns are appearing in the SAM images, presented in Fig. 4, depending on the bonded materials. In particular it has been noticed that when comparing the same kind of materials the ones deposited in tool A were worse compared

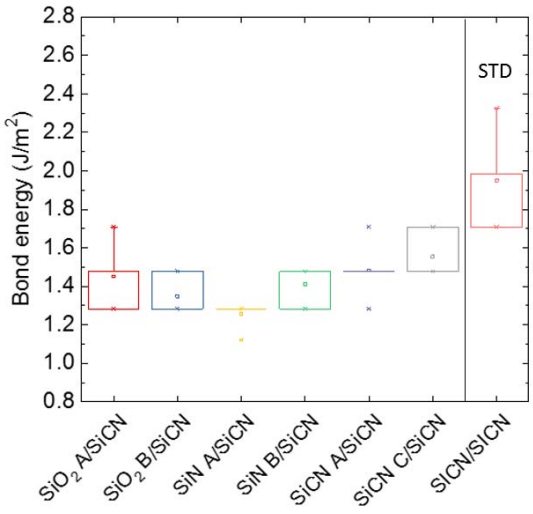

Figure 3. Bond strength results obtained for the different materials tested when densification and post bond anneal temperature are equal to $200°C$

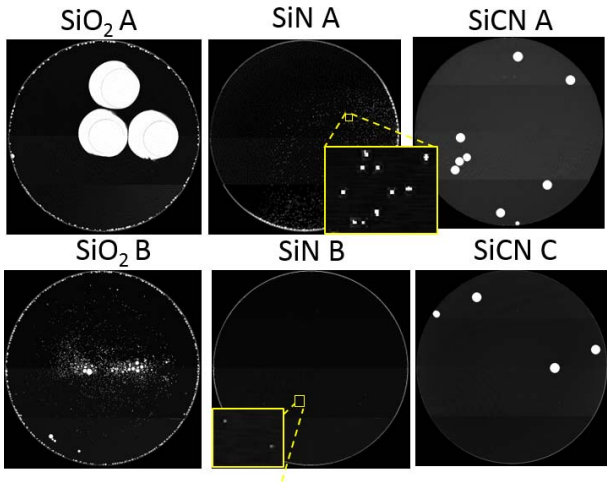

Figure 4. SAM images obtained after bonding and annealing step for the various combinations of films tested. For these experiments densification temperature was $200°C$ and post bond annealing was set to $250°C$. Voids with a variety of shapes are arising after annealing related to out-gassing. If we consider the same kind of material (SiO_2, SiN and SiCN) it appears that films deposited in tool A are worse compared to films deposited in tool B or C.

to the ones deposited in tool B or C. Reasons behind void formation have been analyzed by means of several characterization techniques. The fact that we are not observing any void directly after bonding is excluding particles as possible origin. Whereas one of the most probable root causes can be identified into out-gassing of by-products as it will be discussed later in detail.

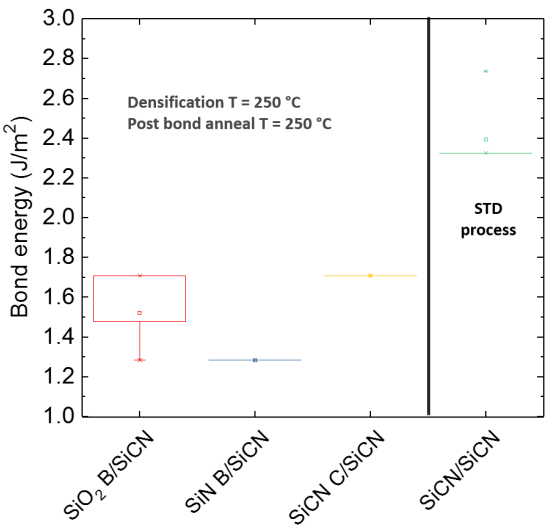

Figure 5. Bond strength results obtained for the different combination of films tested when densification and post bond anneal temperature are equal to $250°C$

If we believe that the possible reason for void formation is out-gassing then a logic choice would be to increase not only the post bond anneal temperature but also the densification temperature to $250°C$ enabling outgassing of the by-products produced at such temperature before the bonding process. By doing so we are able to suppress bonding voids creation and bond strength achieved are shown in Fig. 5. It should be mentioned here that for this test we only used materials which exhibited better void performances meaning SiO_2B , SiNB and SiCNC.

Therefore it appears that, when the post bond anneal temperature exceed the densification temperature, bonding voids are generated at the interface. To validate this observation, we subjected the bonded pairs with wafers densified at $250°C$ to a post bond anneal temperature of $300°C$. Once again, voids were created.

Between all the materials tested SiCNC appears to be the most robust material for void formation and the one which allow us to get the highest bond strength meaning 1.7 J/m^2 when bonded to STD SiCN with a process temperature $\leq$ $250°C$. In spite of that, the bond strength we are able to achieve when bonding STD SiCN to STD SiCN by using the same post bond anneal temperature is significantly higher (2.5 J/m^2) and a possible explanation will be given in the following. However, the mechanical stability of STD SiCN bonded to SiCNC was successfully verified by grinding (see Fig. 6) and dicing test. Therefore we can consider SiCNC as a potential material usable for the application described

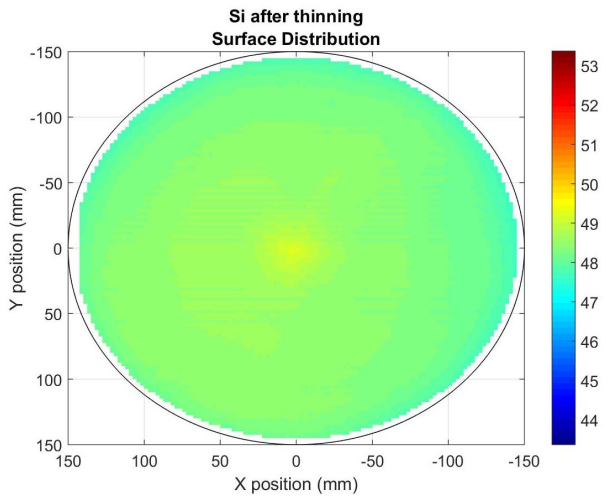

Figure 6. SiCNC/SiCN top wafer surface distribution after grinding to 50 μm

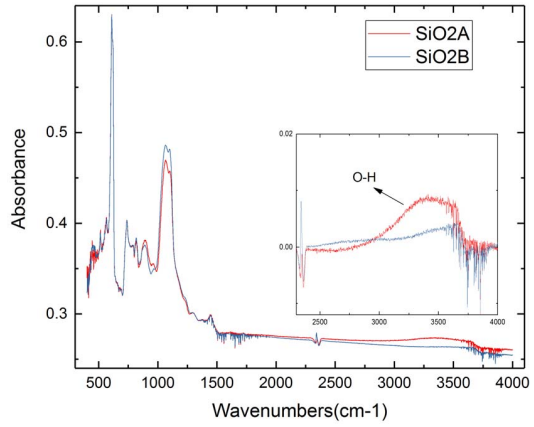

Figure 7. Comparison of FTIR spectra measured for SiO_2A (red line) and SiO_2B (blue line) films. The inset highlight the difference in O-H absorption band (3200-3700 cm $^{-1}$) between the two materials [9].

in the introduction.

A. *Void formation mechanisms*

In order to understand the failing mechanisms for materials A and in general reasons behind void formation between the various materials, films have been inspected by FTIR directly after deposition.

In Fig. 7 the comparison between FTIR spectra belonging to SiO_2A and SiO_2B is presented. The inset shows that in the case of SiO_2A the O-H stretching absorption band 3200-3700 cm^{-1} is more pronounced than for SiO_2B. Such observation is pointing in the direction of voids generated by physiosorbed water. In order to validate such hypothesis we subjected SiO_2A to an annealing of $250°C$ to simulate

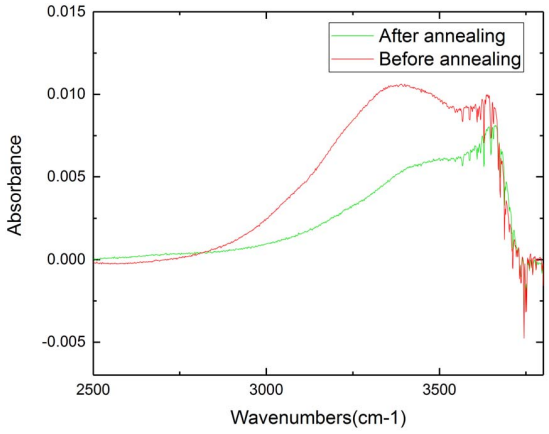

Figure 8. Comparison between spectra belonging to SiO_2 A before and after a 2-hour annealing at $250°C$ centered in the O-H stretching absorption band 3200-3700 cm^{-1}. The broad band can be seen as composed of two regions: molecular water 3225–3400 cm $^{-1}$ and hydroxyl groups 3500–3700 cm $^{-1}$ [9]. It is possible to observe a decrease mainly in the peak corresponding to molecular water.

the post bond anneal step. The comparison between spectra before and after annealing is shown in Fig. 8. It is possible to observe that after annealing the peak corresponding to molecular water (3225-3400 cm $^{-1}$) is decreasing, which make us conclude that one of the reason for void formation is the excessive water in the layer.

Additional characterization analysis has been carried out on SiO_2A. A portion of what it appeared a well bonded area of the wafer pair was submitted to TEM and EDS analysis. Results are shown in Fig. 9. In previous works it was shown that when bonding materials different from SiO_2, the bonding interface was easily located due to the presence of an accumulation of oxygen [8]. For the current case, as it appears from the EDS map, it is difficult to locate what represents the interface region since the difference in oxygen content due to the bonding step cannot be detected.

Interesting features to observe are appearing in the HAADF STEM picture. As highlighted in the yellow circle several darker spots with a diameter of ∼5-10 nm appear equally distributed, probably along the region which can be identified as the interface, close to the SiO_2 layer. Such spots can be associated to nanovoids. Similar nanovoids were previously observed by Ventosa et al. [10]. According to Ventosa these are located at the bonded interface and can be ascribed to unbonded zones created to store water during the sealing mechanism.

Remarkably are the small voids at the edge observed whenever we use SiO_2 materials (Fig. 4). Even SiO_2 films deposited at higher temperatures exhibited such edge voids [11], unveiling the inherent weakness of SiO_2 in

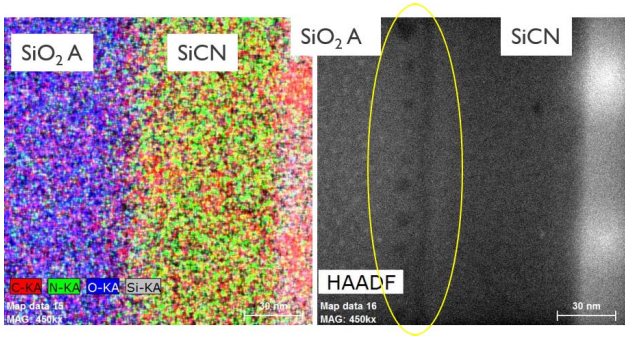

Figure 9. EDS and angular dark field (HAADF) STEM images for SiO_2 A. In the HAADF image are highlighted, in the yellow circle, darker spots assigned to nanovoids and appearing at the interface of SiO_2/SiCN. It is suggested that these nanovoids are filled with water generated during the sealing mechanism of the two wafers.

general for wafer bonding applications. This phenomenon was previously investigated by studying the dynamics of the bonding wave propagation. The voids were ascribed to water droplet nucleation [12]. The fact that in our experiments we are observing this phenomenon exclusively for SiO_2 is confirming our interpretation of water related voids in case of SiO_2.

In the case of nitride type materials we are not able to observe any peak in the region of the O-H absorption band but we can recognize some differences for the peaks around 2100 and 3300 cm^{-1} which represent Si-H and N-H bonds, respectively. In particular, SiNA contains more N-H compared to Si-H bonds, as it appears in Fig. 10. Previous reports are suggesting that this characteristic can potentially identify the layer as N-rich [13], [14]. In the current work we confirmed the N-rich nature of SiN A by means of ERD as shown in Table II.

Table II
ERD COMPOSITION ANALYSIS OF SINA AND SINB

	SiNA	**SiNB**
H	11.7 %	10.5 %
N	50 %	48.1 %
Si	38.3 %	41.4 %

The fact that SiNA can be identified as a N-rich layer is an indication that the hydrogen content is higher compared to SiN B [14]. In Fig. 11 ERD results for the hydrogen concentration are presented. It is possible to notice that H concentration is decreasing after annealing for SiNA and the concentration of H in SiNB is comparable to the one of SiNA after annealing. Taking into account these results we can consider as a possible origin for voids the molecular hydrogen in the bulk or loosely bonded H [15].

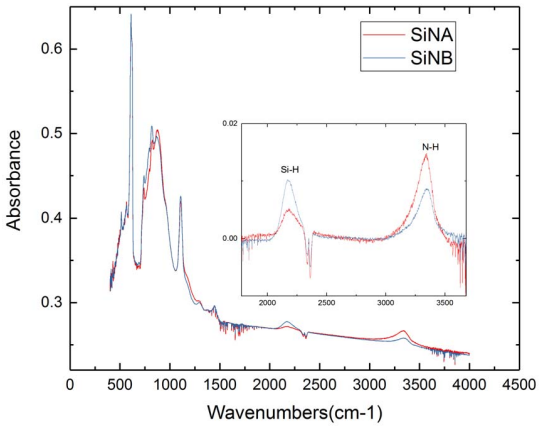

Figure 10. Comparison between SiNA and SiNB FTIR spectra. The inset zooms in the Si-H ∼2200 cm^{-1}, and the N-H peak at ∼3300 cm^{-1}. For SiNA N-H peak is higher than Si-H.

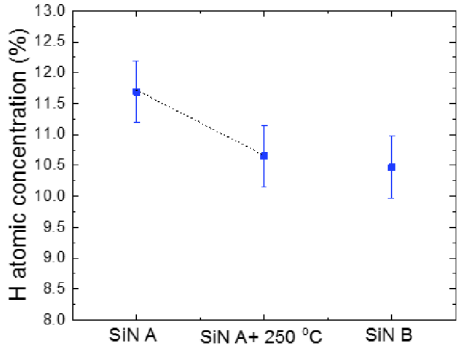

Figure 11. Hydrogen content measured by ERD for as-deposited SiNA, SiNA subjected to 250°C anneal and SiNB. It appears that the H% for SiNB is similar to the one of SiNA after annealing.

B. Lower bond strength of LT materials

As it was stated before, bond strength results achievable when bonding STD SiCN to STD SiCN (STD SiCN/ STD SiCN) are higher compared to the ones for LT materials/ STD SiCN. In order to understand the reason behind the superiority of STD SiCN in terms of W2W bond strength we compare STD SiCN with the SiCN film types.

FTIR spectra of SiCNA and SiCNC did not show any major difference. Contrarily differences can be observed when we compare SiCN STD and SiCNC. As it is shown in Fig. 12, the absorption spectra exhibited peaks at 1260 cm^{-1}, identified as CH_3 symmetric bending in Si-(CH_3), and at 3000 cm^{-1}, attributed to to CH_x stretching vibrations [16]. Such peaks are higher in SiCNC compared to STD

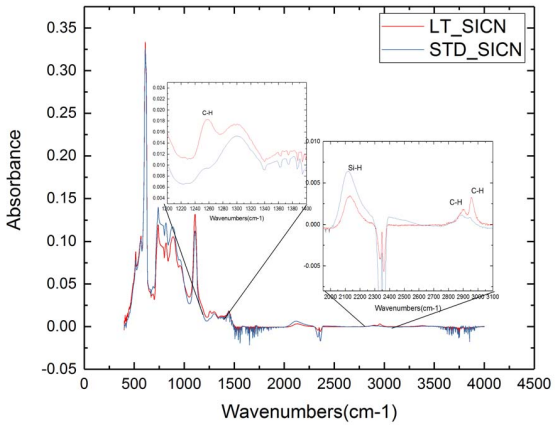

Figure 12. Comparison between SiCNC (LT SiCN) and STD SiCN. The first inset zooms at the C-H stretching band $\sim$ 1260 cm $^{-1}$, assigned to CH_3 symmetric bending mode in Si-$(CH_3)_x$. The second one is zooming at the Si-H $\sim$ 2150 cm $^{-1}$ and CH_x stretching modes. Is it visible that SiCNC is characterized by the presence of an higher C-H concentration compared to STD SiCN. [16]

SiCN suggesting a larger concentration of C-H bonds in SiCNC.

Figure 13 presents ERD results of SiCNC and STD SiCN. In SiCNC a high amount of oxygen is detected even in the bulk identifying the material as SiCNO and not purely SiCN. Density measurement shows that the density of the SiCNC is equal to 1.32 g/cm^3 while the one of STD SiCN is 1.78 g/cm^3. Such low density could point out to a facilitated moisture absorption mechanism which might be the cause of Oxygen presence in the layer.

Also, if we look at the graphs we can see that at the surface we do have a lower Si and C concentration for SiCNC compared to STD SiCN. If considering that SiCNC is characterized by a lower density compared to STD SiCN then we have to expect an even lower amount of Si and C atoms. In the past we have shown some evidence for the importance of Si an C atoms as key elements to increase the W2W bond strength [17]. Then one could ascribe the lower bond strength result that we are able to achieve when bonding SiCNC/STD SiCN compared to STD SiCN/STD SiCN to a decrease amount of of Si and C atoms at the surface.

IV. Conclusions

A material grown at low temperature ($\leq 200°C$) which guarantees void free interface and a bond strength of 1.7 J/m^2, when bonded to STD SiCN with a process temperature $\leq 250°C$, has been selected. It has been demonstrated that the bond strength is high enough to withstand the wafer thinning and dicing processes.

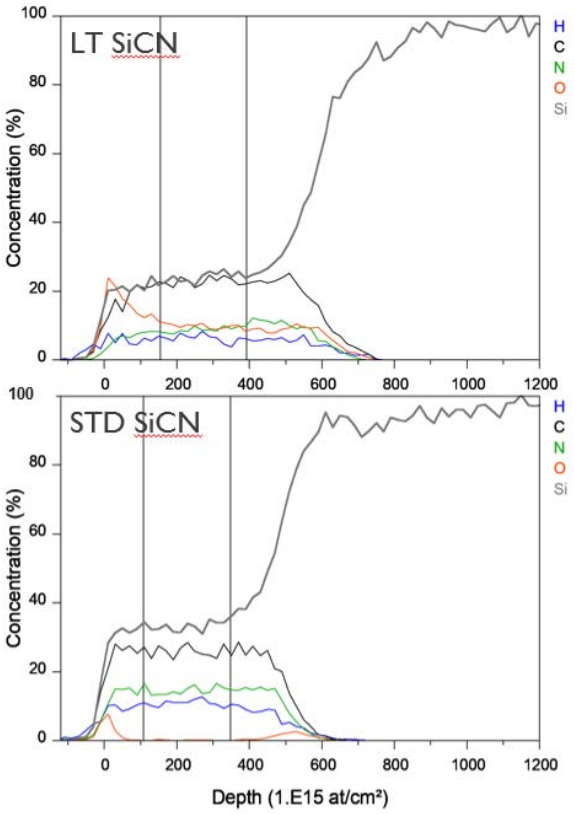

Figure 13. ERD results for STD SiCN and SiCNC (LT SiCN). Oxygen profile is different from both samples as function of depth. In STD SiCN Oxygen is mainly present at the surface as a result of room temperature oxidation mechanism while for SiCNC oxygen it is distributed in the entire bulk.

The lower bond strength of the best LT SiCN material is tentatively attributed to a lower concentration of Si and C at the bond surface when compared to STD SiCN.

It is found that post bond anneal temperature should not exceed densification temperature in order to avoid bonding voids formation.

A study on void formation mechanism has been carried out. The main source of interface voids can be identified as H_2O in the case of SiO_2 and H, present in the in the molecular form or loosely bonded, for SiN.

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