PPAC of sheet-based CFET configurations for 4 track design with 16nm metal pitch

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Abstract: We evaluate Power-Performance-Area & Cost (PPAC) for nanosheet (NS), forksheet (FS), monolithic & sequential Complementary FET (CFET) at 5 & 4 track (T) designs with tight gate pitch (CPP) & metal pitch (MP). While NS & FS prove unsuitable for 4T designs, CFETs provide a performant & cost-effective 4T solution.

Keywords: PPAC, CFET, forksheet, scaling, SAGM, HOT

Introduction: Continuous area scaling has driven CPP & MP down to present patterning limits [1]. Further area reduction is accomplished by reducing the number of available intracell routing tracks (T). Fin depopulation results in drive strength loss in finFETs, for which NS is introduced at 5T for active area recovery [2]. Here, FS [3] & N-on-P CFET [4] are explored for further sheet-based scaling at tighter MP.

Device architectures: We study sheet-based devices (NS, FS & CFET) in 5T & 4T designs at A14 (42nm CPP, 18nm MP) & A7 (39nm CPP, 16nm MP) (**Fig. 1**). Reference is A14 5T NS with 4 sheets of 12nm (4x12). FS has better area efficiency (3x21.5), but at 4T becomes too narrow (11nm FS) [5]. CFET allows 25nm sheets, hence promising for A7 4T scaling [6]. Both monolithic (mono,m) & sequential (seq,s) CFET are evaluated. Basic seqCFET(v1) is wider & taller than monoCFET. SeqCFET(v2) & (v3) try to counter those issues.

CFET process considerations: CFET processing requires more steps than regular non-CFET devices. Mono has an inherent top-bottom self-alignment, but requires many high aspect ratio (AR) processes & does not support split-gate designs [7]. Front-end-of-line (FEOL) processing for seqCFET is similar to non-CFET devices, but needs layer transfer (from bulk Si, SOI wafer or by low temp. Smart Cut™) & thinning of the bonding dielectric (20nm) between the tiers. SeqCFET allows for independent gate connections (simplifying intracell routing) (**Fig. 2, 3 & 4**) [8]. It also has the advantage of independent optimization of channel material, crystal orientation & strain engineering [9]. Here, same S/D-epi-induced stress values were assumed for mono- & seqCFET.

TCAD, CM & PEX: Monte-Carlo (MC) TCAD [10] uses doping & contact resistivity values, which result from fitting IdVg curves to finFET measurement data (**Fig. 5** left)[11][12]. Applying A14/7 dimensions, BSIM-CMG compact models (CM) were fitted to new MC TCAD IdVg data (incl. S/D extension, epi & contact resistance), for varying #sheets (**Fig. 5** right). Parasitic extraction environments (PEX) model the resistance network between the individual sheets [13], mimicking the vertical IR-drop as observed in [12].

Power-Performance analysis: A 15-stage inverter (INVD1), triple fan-out (FO) ring oscillator (RO) is simulated without back-end-of-line (BEOL) wire load, at a total leakage current of 2nA & across varying #sheets. The average current (Ieff) delivered by the Vdd buried power rail (BPR) [14] is plotted against the effective capacitance (Ceff) deduced from the observed INVD1 delay, both normalized to A14 5T NS (4x12). At iso-Vdd, power comparison is based on the normalized Ieff, while performance (freq) benchmarks on the Ieff/Ceff slope (**Fig. 6**). Going to A14 5T FS (3x21.5) & A7 5T FS (4x18.5) reduces Ceff by ~4% & Ieff by ~1.5%, resulting in a freq boost of 3%, setting the reference for all other A7 devices. Reducing cell height from 5T to 4T, FS needs 6 sheets to maintain Ieff, but at 21% higher Ceff, giving 16% lower freq (**Fig. 7**). Thus, FS is not suitable for A7 4T designs. MonoCFET (3x25) is 5.6% ahead of the A7 ref. SeqCFET(v1) suffers a 7% Ceff rise (**Fig. 8**), due to the extended gate connection mask & the bottom gate capping layer (**Fig. 1**). Self-Aligned Gate Merge (SAGM,v2), reusing the active hard mask for the top-bottom gate connection patterning, only reduces Ceff by 1.5% (**Fig. 4**). Removing the bottom gate capping layer (v3) is troublesome & still sees 2.3% Ceff overhead w.r.t. monoCFET. Thus, our best strategy to recover seqCFET is to boost SAGM (v2) drive strength by optimizing the Si crystal orientations independently through use of Hybrid Orientation Technology (HOT) (Ieff +7%). This puts the trajectory of seqCFET(v2) on par with that of monoCFET. The direction of strongest mobility response to stress is <100> for NMOS & <110> for PMOS; thus with stress, standard (STD) <channel>/(wafer) orientation of <110>/(001) is nearly optimal for PMOS, while <100> strongly benefits NMOS (**Table 1**). Without stress, the strongest quasi-ballistic velocity overshoot is for both N- & PMOS in <100>. For PMOS, the favorable (110) surface provides additional benefit. **Fig. 9** shows the impact of stress & orientation on INVD1 performance, which is 5x more sensitive to stress loss in PMOS (w.r.t. NMOS), being the main argument for N-on-P CFET. NMOS stress loss degrades freq by ~4% for all CFET. 4T CFET provides 16% library area scaling vs 5T FS (**Fig. 10**).

Wafer & Die cost: Compared to A14 5T NS, wafer cost for A7 4T FS increases by 11%, due to additional metal layers (**Fig. 11**)[15]. For CFET, more processing steps increase wafer cost (mono+16%, seq+29%). Due to area scaling, die cost is reduced by 15-21%, despite CFET's higher wafer cost.

Conclusions: FS is not a suitable device for 4T designs at tight CPP (39nm) & MP (16nm). STD 4T monoCFET outperforms 5T FS by 5.6%, while offering 16% lib area scaling. SeqCFET suffers a Ceff penalty & requires combined SAGM & HOT to match the performance of monoCFET. Even with non-stressed NMOS, CFET can maintain a performance advantage. Independent strain engineering could give seqCFET an extra benefit over monoCFET, while using fewer high AR processes. CFET scaling manages to reduce die cost by 15-21%.

References: [1] Y. Sherazi *et al.*, SPIE, 1096202 (2019), [2] J. Ryckaert *et al.*, IEDM, p.685 (2019), [3] P. Weckx *et al.*, IEDM, p.871 (2019), [4] P. Schuddinck *et al.*, VLSI, p. 204 (2019), [5] B. Chehab *et al.*, IITC, S9-4 (2021), [6] L. Liebmann *et al.*, IEDM, p.51 (2021), [7] S. Subramanian *et al.*, VLSI, TH3.1 (2020), [8] Semulator3D, Coventor, [9] A. Vandooren *et al.*, VLSI, TH3.2 (2020), [10] SDEVICE MC S-2021.06, Synopsys, [11] S.-Y. Wu *et al.*, VLSI, p.92 (2016), [12] F. M. Bufler *et al.*, TED 67 (11), 4701 (2020), [13] QuickCap R-2020.09-SP4, Synopsys, [14] A. Gupta *et al.*, IEDM, p.502 (2021), [15] G. Mirabelli *et al.*, submitted to VLSI Symp. 2022.

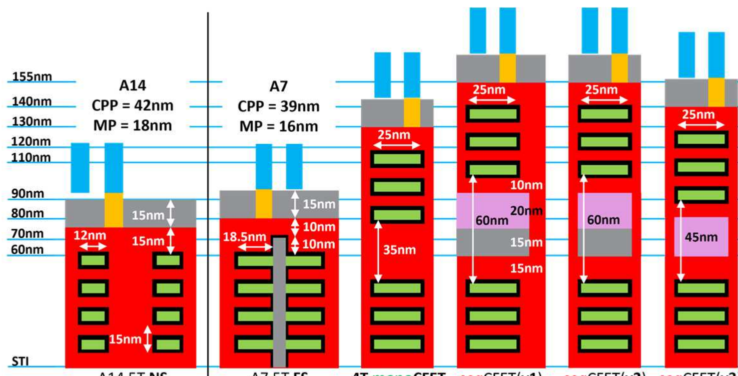

Fig. 1: Gate cross sections for nanosheet (NS), forksheet (FS) & CFET (monolithic & sequential). Basic seqCFET (v1) is wider & taller than mono. Self-aligned gate merge (SAGM,v2) & no gate cap (v3) approach monoCFET.

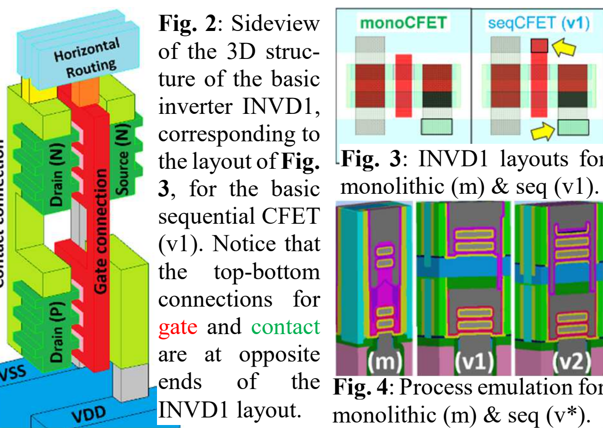

Fig. 2: Sideview of the 3D structure of the basic inverter INVD1, corresponding to the layout of **Fig. 3**, for the basic sequential CFET (v1). Notice that the top-bottom connections for gate and contact are at opposite ends of the INVD1 layout.

Fig. 3: INVD1 layouts for monolithic (m) & seq (v1).

Fig. 4: Process emulation for monolithic (m) & seq (v*).

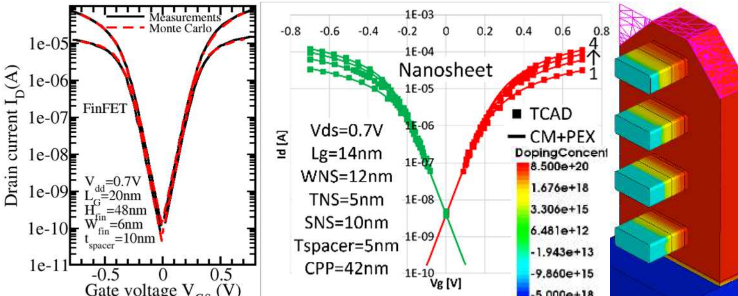

Fig. 5: (left) IdVg at V_{DS}=0.7V & 0.05V according to FinFET measurements [11] and doping & contact resistivity calibrated MC simulations [12] (©2020 IEEE). (right) IdVg at V_{DS}=0.7V for A14 5T NS: MC TCAD and fitted CM.

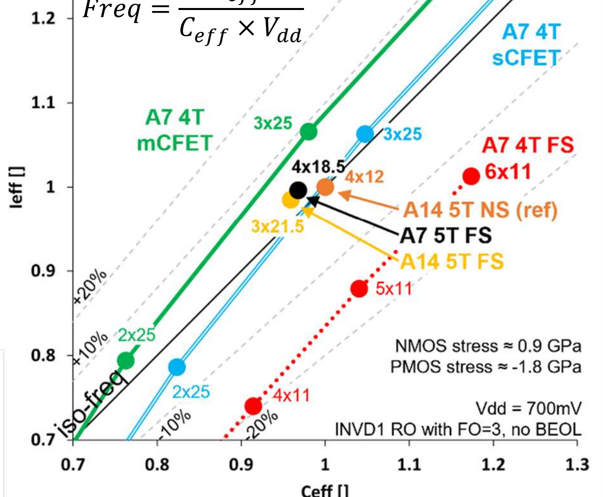

Fig. 6: Ring Oscillator (RO) based evaluation of INVD1 power and performance for varying number of stacked sheets. Effective current (Ieff) and capacitance (Ceff) are normalized to A14 5T NS with 4 sheets of 12nm (4x12). A7 5T FS (4x18.5) benefits from 3% reduction in Ceff. The 4T CFET configurations are evaluated w.r.t. this A7 reference point.

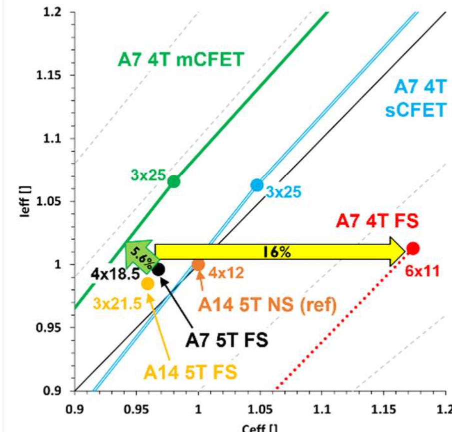

Fig. 7: Zoom of **Fig. 6**. FS is not suitable for 4T designs (16% lower performance). 4T CFET is viable with 5.6% higher freq for monoCFET.

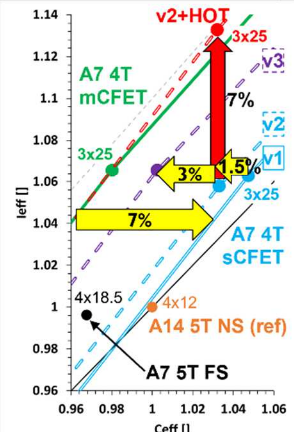

Fig. 8: Improving seqCFET (v1) by SAGM (v2), no gate cap (v3) & optimized HOT.

ION per Weff [µA/µm]	WITH stress		WITHOUT stress	
	STD+	Optimal+	STD-	Optimal-
N-type NS	<110>/(001)	<100>/(001)	<110>/(001)	<100>/(001)
<channel>/(wafer)	799	945 (+18%)	758	810 (+7%)
P-type NS	<110>/(001)	<110>/(110)	<110>/(001)	<100>/(110)
<channel>/(wafer)	917	955 (+4%)	590	674 (+14%)

Table 1: NS ON current normalized by effective width (Weff) for standard (STD) & optimal (HOT) crystal orientations, with (+) & without (-) stress. Notice that the optimal channel orientation is different for PMOS with & without stress.

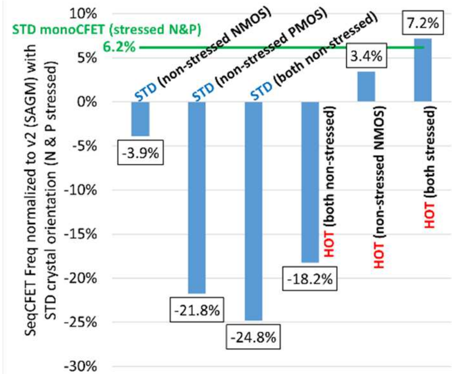

Fig. 9: INVD1 performance impact of stress & crystal orientation. Performance is 5x more sensitive to stress loss in PMOS. Switching from standard orientation (STD) to optimal Hybrid Orientation (HOT) boosts frequency by 7%.

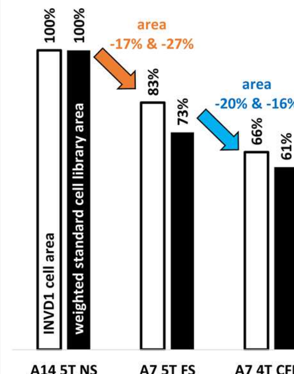

Fig. 10: Area scaling from A14 5T down to A7 4T CFET, at cell & library level (~Arm 64bit core PnR). FS lib is compacter than NS due to extra gate cut masks.

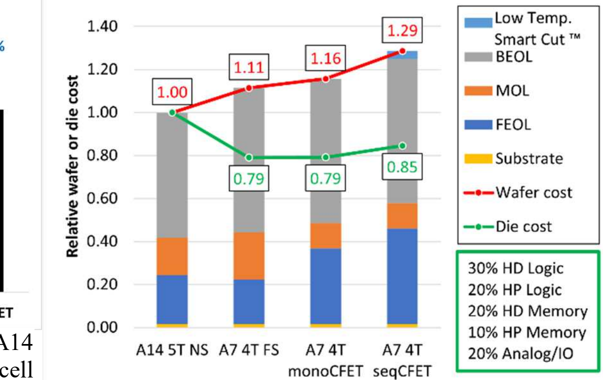

Fig. 11: Wafer & Die cost of A7 4T technologies w.r.t. A14 5T NS. Wafer cost increases due to additional routing layers & process steps. Die cost decreases due to scaling.