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# Perspective of 2D Integrated Electronic Circuits: Scientific Pipe Dream or Disruptive Technology?

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**Within the last decade, considerable efforts have been devoted to fabricating transistors utilizing 2D semiconductors. Also, small circuits consisting of a few transistors have been demonstrated, including inverters, ring oscillators, and static random access memory cells. However, for industrial applications, both time-zero and time-dependent variability in the performance of the transistors appear critical. While time-zero variability is primarily related to immature processing, time-dependent drifts are dominated by charge trapping at defects located at the channel/insulator interface and in the insulator itself, which can substantially degrade the stability of circuits. At the current state of the art, 2D transistors typically exhibit a few orders of magnitude higher trap densities than silicon devices, which considerably increases their time-dependent variability, resulting in stability and yield issues. Here, the stability of currently available 2D electronics is carefully evaluated using circuit simulations to determine the impact of transistor-related issues on the overall circuit performance. The results suggest that while the performance parameters of transistors based on certain material combinations are already getting close to being competitive with Si technologies, a reduction in variability and defect densities is required. Overall, the criteria for parameter variability serve as guidance for evaluating the future development of 2D technologies.**

## 1. Introduction

The last half-century in microelectronics was clearly dominated by silicon (Si) technology. Countless contenders with higher mobility than Si have been demonstrated, including Germanium and various III-V materials, but they have only been successfully applied and commercialized in a few niche markets at best. The reasons for the immense success of Si technology are manifold, including for instance the native oxide of Si ($SiO_2$), the extremely well established and finely tuned processing capabilities, as well as the existence of both n- and p-type metal-oxide semiconductor (MOS) transistors, which enable highly efficient complementary MOS (CMOS) logic. With further scaling, intense efforts have been exerted toward improving fabrication methods in order to enable a steady increase in the performance of Si field-effect transistors (FETs). At the current state of the art the technology node for Si transistors is in the sub 10 nm regime. However, in such small devices short channel effects (SCEs), increased variability and reliability issues,[1] but also reduced channel carrier mobility for sub-3 nm channels[2] pose serious challenges for continued use of Si technology. To overcome the drawbacks of ultra-thin devices made from Si, research in alternative material systems for transistor structures has intensified in the last decade. So-called 2D materials have shown to be particularly advantageous for post-silicon technologies and could potentially provide a solution to the aforementioned limitations of Si technology.[3,4]

2D semiconductors are thermodynamically stable as single atomic layers[5] and have a thickness of about half a nanometer. Ideally, the surfaces of these 2D layers are inert and free of dangling bonds and other defects, which would allow for the formation of nearly defect-free interfaces with other layered materials. Consequently, if the same holds true for the insulators employed, the charge carrier mobilities in 2D semiconductors can be expected to be very high, since scattering and trapping at surface defects is minimized.[6,7] In addition, transistor structures with channel thicknesses below 1 nm have been realized, which suppress the aforementioned SCE.[8] Thus, FETs fabricated employing 2D semiconductors are expected to exhibit large carrier mobility, nearly ideal sub-threshold slopes, and high on/off current ratios which opens the door for ultra-scaled post-silicon technologies.

While tremendous efforts have been exerted into the fabrication of 2D transistor prototypes employing various material

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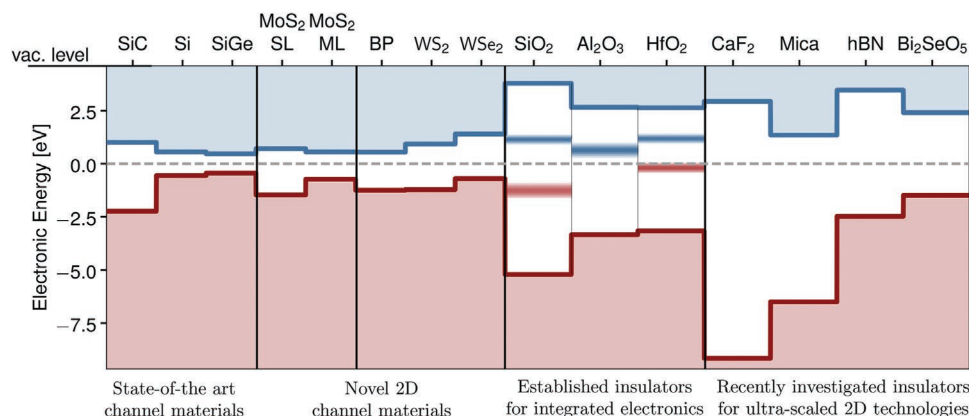


**Figure 1.** Various combinations of 2D materials for the channel and insulators have been investigated for novel 2D transistors structures. Next to the band-alignment, the energetic distributions of known trap bands[38,60,61] are also given. When searching for the ideal material system for 2D electronics, one aim is to achieve the highest robustness of the device against charge trapping at insulator traps. Toward this aim, the energetic distance between the relevant band edges of the channel material and the trap bands should be maximized.[41,62]

combinations,[9–12] the research into 2D electronic applications is still in its infancy. So far, small digital circuits such as inverters,[13–19] logic gates,[20,21] ring oscillators (RO),[22] static random access memory cells (SRAM),[22] but also an operational amplifier,[23] and a simple microprocessor[24] have demonstrated stable operation when made from 2D materials. The stable operation of the circuits strongly relies on the fabrication of transistors with well-defined properties, that is, process-controllable threshold voltage, large sub-threshold slope, and on/off current ratio, but also small time-dependent parameter drifts to ensure a long lifetime. However, as evidenced from experimental studies, 2D transistors can still exhibit large variability, that is, in the threshold voltage with $\sigma_{\mathrm{Vth}} \approx 1\mathrm{V}$,[25–27] which is a serious issue for industrial applications. Furthermore, from studies on silicon technologies it is already well known that in scaled devices the impact of individual defects on the current flow is more pronounced than in large-area devices,[28–32] ultimately leading to a higher time-dependent variability for small area FETs.[33,34] Since a central advantage of 2D FETs is their superior scalability toward ultra-small dimensions,[3,4] charge trapping at single defects may entail a considerable performance limitation for these technologies when they are scaled down further. Therefore, it is worthwhile to explore the impact of both time-zero and time-dependent variability on the stability of electronic circuits at an early stage of the development process of a new technology.

For the design of integrated circuits typically ideal transistors are assumed. To some extent, time-zero variations of the characteristics of the employed components can be compensated by guard bands in the design, for example, by increasing $V_{\mathrm{DD}}$ to ensure higher gate-overdrive bias to compensate for large $\sigma_{\mathrm{Vth}}$.[35,36] Unfortunately, these guard bands come at a cost, for example, reduced performance or increased area requirements.[35,37] Also, the determination of these guard bands is much more difficult for time-dependent variations, which can then lead to severe reliability issues in electronic applications. This is particularly true for scaled nodes in which variations of, for example, $\Delta V_{\mathrm{th}}(t)$ are known to increase.

In this work both time-zero and time-dependent variations in the characteristics of 2D FETs are investigated and their impact on the performance of electronic circuits is discussed. Our evaluation considers the variation of the static transfer characteristics of a transistor whose physical causes will be likewise discussed. Regarding time-dependent effects, we will focus on charge trapping, which appears to be dominant in 2D devices.[38–41] Other time-dependent aging effects such as hot carrier degradation[42] and the breakdown of the insulator[43–45] are known; however, they will not be considered in our study as no well established models currently exist. Thus, our results will provide a lower bound to the time-dependent variability. Subsequently, based on models calibrated to the best performing 2D transistors published, the suitability of 2D technologies for integrated electronic circuits will be studied. For this purpose, three key digital benchmark circuits, namely the inverter, the ring oscillator, and the 6T-SRAM cell, are analyzed in considerable detail. In this context, the influence of processing tolerances and time-dependent variations in the characteristics of 2D FETs on the behavior of circuits is investigated. Based on our results, benchmark values are defined enabling an efficient evaluation of the competitiveness of newly developed structures.

## 2. Material Systems for 2D FETs

A promising class of 2D semiconductors are transition metal dichalcogenides (TMDs)[46,47] (for example $MoS_2$,[9,20] $WS_2$,[10,48] $MoSe_2$,[11,49] $WSe_2$[12,50] etc.) or the class of Xenes,[51] which are single-elemental 2D semiconductors like black phosphorus (BP)[52,53] and silicene.[54,55] The metal-insulator-semiconductor layer which is the central element of FETs are formed in combination with gate insulators such as hBN,[7,56] $SiO_2$,[11,20] $HfO_2$,[57,58] $Al_2O_3$.[8,59] An overview of some electronic properties of selected materials for 2D electronic applications is provided in **Figure 1**.

For the fabrication of single and multi-layer films, several methods are being considered, including mechanical exfoliation,[5,63] chemical vapor deposition (CVD),[64,65] metal organic CVD,[66,67] and atomic layer deposition (ALD).[68,69] The evaluation of the performance of a technology is thereafter carried out on the basis of the most important properties of the transistors, which are collected in **Figure 2**. It is the deviation of


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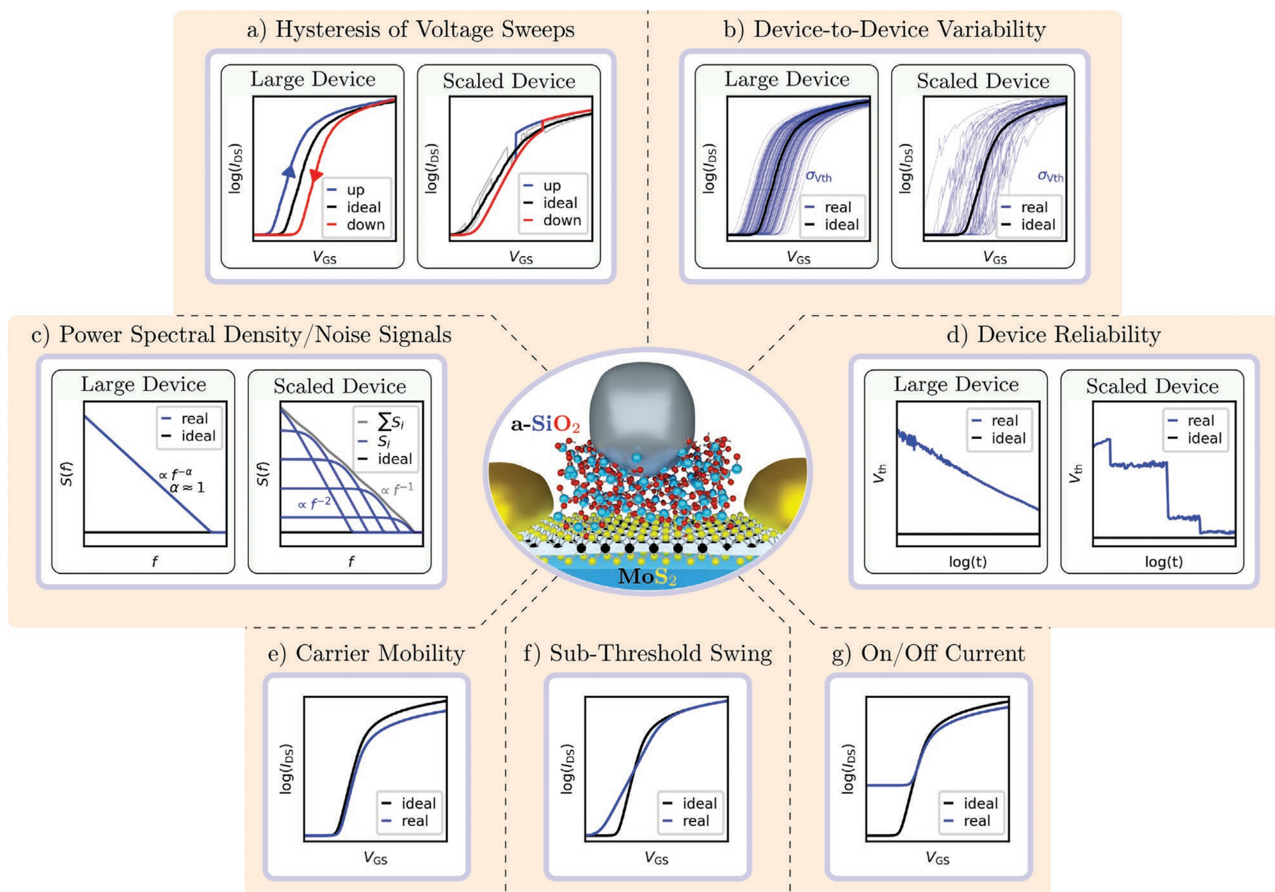


**Figure 2.** Nonideality issues in individual FETs directly impact the circuit level performance. The most important such effects are related to dynamic trapping and de-trapping of charge carriers, which results in several modifications of the transistor characteristics which must be taken into account for the design of robust circuits. The most prominent challenges shown here are a) hysteresis of voltage sweeps,[76–78] b) time-zero combined with time-dependent device-to-device variability in the threshold voltage of nominally identical devices,[79] c) significant noise signals,[80,81] d) time-dependent variability, typically referred to as device stability and reliability,[77,82,83] e) channel carrier mobilities which are often considerably lower than theoretical values,[79] f) limited sub-threshold swing,[58] and g) reduced on/off current ratios.[84] Particularly noteworthy is that for scaled devices (a–d), that is, charge transitions of single defects become visible as discrete steps in the characteristics.

the real transistor characteristic curves from the ideal behavior of a transistor which is particularly important here. The dominant reason for these deviations is the presence of non-idealities in the structure, that is, mostly defects which occur at the interface between the conductive channel and the insulator or directly inside the insulator. These defects can change their charge state during operation or measurement and thus lead to a distortion of the ideal transistor characteristics. Continuous improvement of the manufacturing processes can considerably reduce the number of electrically active defects, but understanding their influence on both transistors and circuits is not trivial. In addition, it should be noted that some defects are intrinsic properties of the material system and bonding nature of the insulator to the semiconductor interface and therefore cannot be avoided. For example, the surface of amorphous insulators is characterized by an inherently high defect concentration leading to a deterioration of the device performance.[62] The replication of non-ideal device behavior through theoretical models, in addition to the description of the static and dynamic device characteristics, is therefore an important prerequisite for the evaluation of the robustness of integrated electronic circuits.

## 3. Performance Evaluation and Compact Modeling of Transistors

To evaluate the functionality of electronic applications, circuit simulations are usually performed during the development process,[70,71] with SPICE being the de facto standard. For this, compact models, for example, the BSIM model,[72] or the models implemented in HSPICE, are typically used to represent the behavior of the transistors. Initially the models have been developed for Si technology, but recent enhancements to explain peculiarities seen in 2D transistors have been proposed: For instance, analytical formulas and Verilog-A models to replicate the characteristics of $MoS_2$ transistors have been proposed.[71,73,74] Other approaches for simulating the drain current in 2D transistors employ the drift-diffusion model,[75] but also a combination of TCAD simulations, that account for other


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physical effects, with look-up tables implemented in Verilog-A have shown promising results.[25] The proposed models have been mostly verified employing experimental DC characteristics of 2D transistors. However, the response to AC signals, as well as nonideality effects arising from time-zero and time-dependent variability sources, are not considered in current approaches. In order for circuits to be as robust as possible against deviations from the ideal behavior, that is, process-related or operation-related variations, the impact of these deviations must be evaluated at the circuit level. Before evaluating the circuit performance the most important sources for transistor reliability are discussed as these form the basics for understanding circuit aging.

### 3.1. Main Sources of Nonideality Effects in FETs

The most important nonideality effects which impact the behavior of digital electronic circuits are summarized in Figure 2.The most obvious dynamic effect is the hysteresis of the transfer characteristics (Figure 2a) which has been extensively studied in the 2D transistor literature.[76–78,85–88] This observed hysteresis is caused by defects which are charged during the up-sweep of the gate voltage but which do not have enough time to discharge before the end of the down-sweep, thereby resulting in a shift of the threshold voltage compared to the up-sweep. The hysteresis depends strongly on the insulator/2D semiconductor combination, the device design, and on the applied gate sweep range and the sweep rate.[77,78,86,89] Compared to Si technology, the normalized hysteresis width of state-of-the-art 2D devices is about 50–100 times larger for comparable device geometry and oxide thickness,[89] which is a clear indicator of the massive number of defects present in 2D devices.[4] While in large-area devices the hysteresis is the response of thousands of defects, only a small number of defects can contribute in scaled technologies since this number of defects per device typically scales with gate area. At the same time, the impact of a defect on the device behavior becomes more pronounced in scaled transistors. Consequently, discrete charge capture and charge emission processes at the defects appear in the measurement signal.[90,91] From Si technology it is well know that the impact of single defects on the drift of the threshold voltage $\Delta V_{\mathrm{th}}$ is widely distributed and approximately follows an exponential distribution. In addition, their capture and emission times vary from the picosecond regime up to several years[90,92] and show an exponential bias and temperature dependence.[93] As a consequence, these defects can lead to considerable dynamic device-to-device variability (Figure 2b) during operation. This can be particularly unfortunate for integrated circuits where the functionality requires the seamless interaction of billions of transistors. Hence, for circuits, the reproducibility and stability of the transistor characteristics is essential. This becomes even more critical in scaled transistors since, while the total number defects decreases with device area, the impact of a single defect on the device characteristics increases with decreasing gate area.[33,94] As a consequence, while the area scaling cancels in the mean of $\Delta V_{\mathrm{th}}$, the variance increases with $\sigma_{V\mathrm{th}}$ perA.[33] Thus ultra-scaled nodes exhibit a larger variability than their large-area counterparts. The same effect can also be observed in the noise signals (Figure 2c): While for large-area MOSFETs the power spectral denstiy (PSD) approximately follows an $1/f$ behavior, which results from the superposition of the individual Lorentzian spectra obtained from a single defect,[95,96] in scaled devices, the individual Lorentzian contributions become clearly visible.

Another important reliability criterion for transistors is the slower drift of the threshold voltage $\Delta V_{\mathrm{th}}$ which can be observed in the time domain and is typically referred to as the bias temperature instability (BTI)[97,98] (Figure 2d). Again, while the change of $V_{\mathrm{th}}$ is continuous for large-area devices, discrete steps dominate the $\Delta V_{\mathrm{th}}$ behavior of scaled transistors. Each of the observed steps is the result of a charge capture or charge emission event, respectively, depending on the sign of the step height, or due to the creation/annihilation of defects. Such signals have already been studied in detail for Si technology.[90,99,100] Note that single defects are also regularly investigated at constant applied biases, that is under equilibrium conditions. In this case defects that exhibit similar charge capture and emission times, that is $\tau_c \approx \tau_e$, give rise to random telegraph noise (RTN). From RTN signals the charge transition times can be extracted directly.[101–104]

The charge trapping kinetics form the basis for the development of theoretical defect models which are essential for an accurate calculation of $\Delta V_{\mathrm{th}}$ trends as a response to arbitrary voltage and temperature signals.[60,104,105] These simulations enable the estimation of the device lifetime but also to predict the robustness of circuits under various operating conditions. Further nonideality effects include the carrier mobility (Figure 2e) which should be as large as possible and the sub-threshold swing (SS) (Figure 2f) which should be as small as possible (theoretical limit 60 mV dec$^{-1}$ at room temperature) to allow switching of the transistor at a minimum $\Delta V_G$, and thus enable a low $V_{DD}$. Also important is a large on/off current ratio (Figure 2g) and a small gate leakage current to minimize the static power consumption of transistors and circuits.

### 3.2. Modeling the Impact of Defects on Transistors

To describe the impact of the defects on transistors and circuits a combination of time-zero and time-dependent distributions of transistor parameters must be employed,[106] see **Figure 3**. The time-zero variability of parameters such as $V_{\mathrm{th}}$ or SS in circuit simulations is relatively straight forward to consider via Monte Carlo simulations .[110] However, the intricate charge trapping kinetics of defects in transistors must be considered when time-dependent effects are being investigated. For Si technologies various models have been proposed to explain the charge-trapping induced drift in the $V_{\mathrm{th}}$ of n-type and p-type transistors, mostly employing empirical formulas. Over the last decade, detailed physics-based models have been developed[60,90] and proven to provide an accurate explanation of charge trapping in large- and small-area devices alike. Furthermore, circuit simulations have been carried out employing a simplified version of the model.[60,111] Before the impact of time-zero and time-dependent variability on 2D electronic circuits is described in detail, the models used for the evaluation are discussed briefly.


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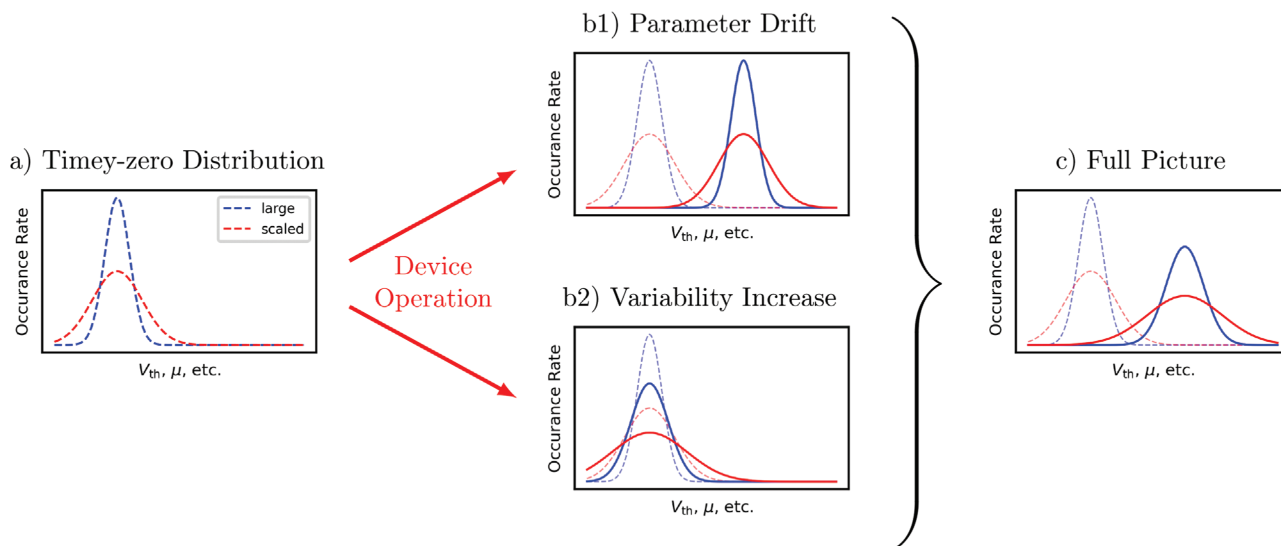


**Figure 3.** To ensure the robust operation of electronic applications, a high resilience against deviations from their ideal operational characteristics of transistors is important. Thus, time-zero and time-dependent effects have to be considered in simulations. a) The time-zero distributions include device-to-device variations as a consequence of the fabrication process and can be described statistically using measured distributions, which must properly consider the various cross-correlations.[107–109] Time-dependent variability emerges on the one hand as b1) drift of characteristic parameters during operation and on the other hand b2) lead to an increase of the variance of the parameter distributions. The explanation of time-dependent effects on the device performance requires sophisticated physical models since their impact and dynamics strongly depend on the operating conditions. c) For the evaluation of a circuit, the superposition of both effects must be considered at the highest accuracy, which is a complex endeavor. To account for time-dependent variability effects, worst-case simulations are often performed employing the envelope of certain distributions. However, an overestimation of device performance degradation may lead to the incorporation of a significant overhead in the circuitry.

The origin of time-zero parameter variation is typically assumed to result from process variations. For 2D transistors, initially most studies only analyzed few selected devices and did not touch upon the question of device variability. Recently, however, initial studies on the variability in 2D FETs have been performed, mostly on the chip-scale[79,112,113] and in a few instances on the wafer-scale.[114–116] In these studies, growth defects in 2D semiconductors,[114] bilayer islands,[116] and adsorbed impurities at the semiconductor to insulator interface[113] were identified as the most important sources of variability in 2D technologies.[4]

The time-dependent changes, on the other hand, are largely determined by charging and discharging processes of insulator and interface defects.[94,106,108,117–120] In initial studies on single defects in scaled $MoS_2/SiO_2$ transistors, distinct charge trapping events were observed using RTN measurements, see **Figure 4**a,b.[40,91] RTN signals as shown in Figure 4a are characterized by discrete transitions between two disjunctive current levels which are recorded at constant applied gate and drain voltages. These current levels correspond to charge states of an individual defect, which switches between its states at statistically distributed times. Note that the effect of a defect on the change in current $\Delta I_D$ varies dramatically from defect to defect. It is particularly noteworthy that, for the investigated $MoS_2/SiO_2$ transistors, defects with an impact on the drain current of up to $\Delta I_D \approx 70\,\text{nA}$, that is 50% of the measured current, can be observed (see Figure 4b). Such giant steps can significantly influence the yield of a technology, and cannot be described with existing physical models. To examine the probability of the occurrence of such a “killer-defect”,[121] RTN and measure-stress-measure experiments (MSM)[90,122] are performed on a few dozen transistors of the same technology and the distribution of step heights is analyzed, see Figure 4c. The flat branch (tail) of the complementary cumulative distribution functions (CCDFs) originates from defects with exceptionally large step heights, which might potentially have a strong effect on the behavior of transistors and circuits. Thus, such large step heights are a decisive factor in determining the quality of a technology and its suitability for integrated electronic applications. Furthermore, it has to be noted that the average step heights $\eta_1$ and $\eta_2$ decrease with increasing active gate area. In order to describe the probability with which one can anticipate steps of a given height $\Delta I_D$, the CCDF of $\Delta I_D$ is calculated for a certain technology. For $MoS_2$ devices, the CCDF shows bi-modal exponential characteristics, similar to those observed for Si technologies. However, the second branch in the bi-modal exponential distributions of the steps in $MoS_2$ transistors is flatter in comparison to Si. This results in an increased probability of giant steps (see Figure 4b). This leads, in combination with an enhanced trap density when compared to Si, to a considerably larger variability for current 2D devices. While the CCDF describes the distribution of the impact of the defects on $I_D$, the number of defects per transistor has been found to follow a Poisson distribution.[123,124]

In addition to the step heights, the charge trapping kinetics of the defects must be reproduced by simulations. For 2D transistors the charge trapping kinetics of a small set of defects has been extracted recently from RTN signals and reproduced using a two-state defect model, see **Figure 5**a.The extracted trap parameters, that is, energetic trap levels, depth, and relaxation energy, are similar to parameters known from Si technology,[40,127] where this model has been established to explain both the continuous $\Delta V_{th}$ shifts in large-area devices[93,128–130]

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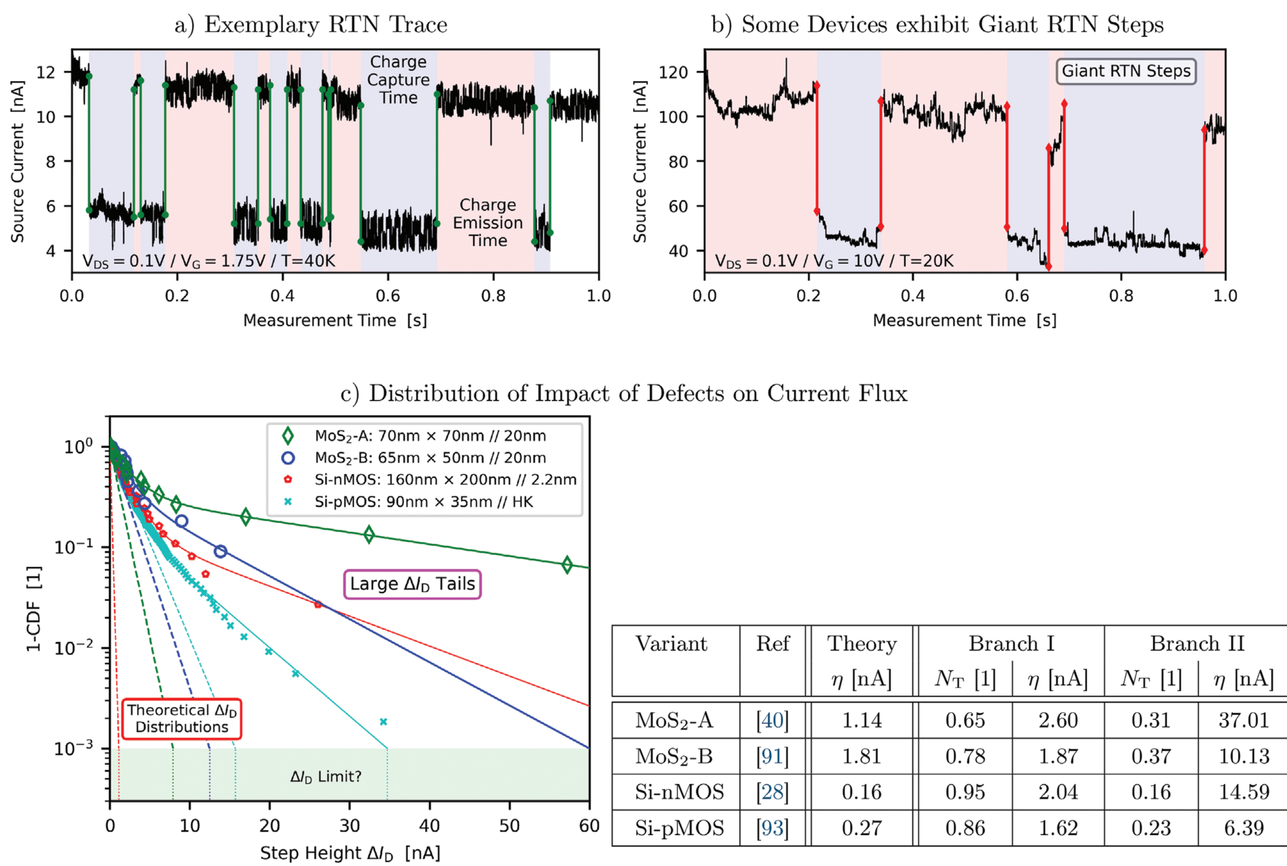


| Variant | Ref | Theory | Branch I | | Branch II | |
|---|---|---|---|---|---|---|
| | | $\eta$ [nA] | $N_T$ [1] | $\eta$ [nA] | $N_T$ [1] | $\eta$ [nA] |
| $MoS_2$-A | [40] | 1.14 | 0.65 | 2.60 | 0.31 | 37.01 |
| $MoS_2$-B | [91] | 1.81 | 0.78 | 1.87 | 0.37 | 10.13 |
| Si-nMOS | [28] | 0.16 | 0.95 | 2.04 | 0.16 | 14.59 |
| Si-pMOS | [93] | 0.27 | 0.86 | 1.62 | 0.23 | 6.39 |

**Figure 4.** a) Exemplary RTN trace. The individual stable current levels of the measurement signal can be assigned to a charge state of defects, that is, charged versus neutral. b) Quite remarkably, enormously large step heights have been observed, for example, for $MoS_2/SiO_2$ transistors. c) From RTN and BTI measurements the complementary cumulative distribution function (CCDF) of discrete current changes $\Delta I_D$ can be recorded, which is an indicator for the influence of defects on the transistor characteristics. Obviously, the frequency with which defects with large step heights, that is flat branch (tail) of the CCDFs, occur ("killer-defects"[121]) is a decisive factor in determining the quality of a technology and its suitability for integrated electronic applications. Note that, theoretical values which are typically calculated using the charge sheet approximation considerably underestimate the experimentally observed $\Delta I_D$, thereby giving rise to circuit failure. The physical explanation for the upper boundary of $\Delta I_D$ still remains an open issue and requires further attention for both Si and 2D transistor technologies.

and the intricate features of the charge trapping behavior of single defects observed in scaled nodes.[131–133] This allows to employ the trap bands from Si for the theoretical analysis of 2D electronic applications.

Another important aspect in this analysis is the number of defects which are able to contribute to charge trapping, limiting the device performance. In literature, trap densities have been extracted using different experimental methods, for example, hysteresis, RTN, BTI, or CV measurements, to name a few; however, only a certain fraction of defects contribute to the measurement signals of each of these methods. Thus, different experimental techniques cover different experimental windows, see Figure 5b. It is noteworthy that the typical operating ranges of circuits are outside of the measurement window which is accessible with available tools and methods. Therefore, the physical accuracy of available models is an essential factor for the precise extrapolation of the behavior of defects and devices at the circuit level. To ensure the accuracy of the model parameters the calibration is based on measurements performed at different temperatures and stress conditions to analyze devices and circuits operating under various operating conditions.

### 3.3. Time-Dependent Variability in 2D FETs

In general, the requirements for integrated circuits are summarized in the international roadmap for devices and systems (IRDS). According to the IRDS, a $V_{DD} = 0.65$ V for electrical circuits is targeted for 2028.[134] This requires that transistors can be switched from accumulation to inversion in the gate voltage range $V_G \in [GND : V_{DD}]$, even when parameters such as $V_{th}$ change due to parasitic effects. State-of-the-art $MoS_2$ transistors have defect densities of up to $N_T = 10^{13}\,cm^{-2}$,[38,135,136] which is considerably larger than values known from Si technology. For the technology from **Figure 6**a with an equivalent oxide thickness EOT = 20 nm, this means that for areas $W \times L < 10^{-2} \mu m^2$, scaling of the gate insulator thickness down to EOT = 1.8 nm will likely not be sufficient to enable an operation at $V_{DD} = 0.65$ V. Instead, without a drastic simultaneous reduction of the defect density, an operation of this technology at a small $V_{DD}$ would result in an unacceptably low yield and thus would not be economical.In fact, a comparison with state-of-the-art technologies in Figure 6a shows that the variability of $V_{th}$ between individual transistors of the same


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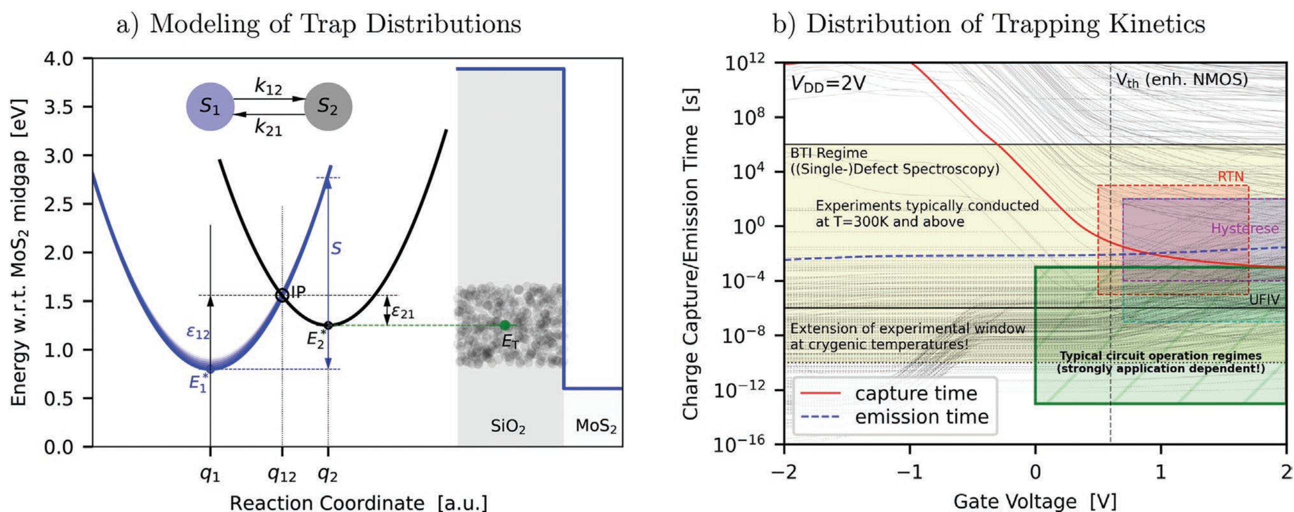


**Figure 5.** In our study, the calculation of the charge trapping kinetics of defects for 2D FETs is based on a two-state defect model implemented into SPICE.[60,111,125] a) In the simulations, the trap band considered for the following analysis is energetically aligned slightly above the conduction band edge of the $MoS_2$ channel, inline with results know from Si[60] and 2D.[126] b) The combination of trap level, trap depth, and the curvature of the parabolas leads to widely distributed charge capture and emission times, consistent with experimental observations. It is also observed that the trapping kinetics depend on the applied gate bias and temperature (not explicitly shown here). The gate bias and timing range of traps which can be extracted from measurements strongly depend on the technique applied. In particular, the experimental windows for BTI, RTN, hysteresis, and ultra-fast *I- V* measurements (UFIV) can be vastly different. However, the timing, that is, operational frequencies, of digital circuits is typically considerably faster than what can be accessed by experiments. Thus, the charge trapping kinetics of the defects have to be extrapolated to this regime accordingly.

technology needs to be improved by about tenfold to enable operation at low supply voltages. It should be noted that the impact of defects on $V_{\mathrm{th}}$ is typically approximated in theoretical models using the charge sheet approximation (CSA).[146] For the CSA it is assumed that the oxide charge is uniformly distributed over a fictious sheet in the insulator and thus the impact of a single defect on the device threshold voltage can be described by

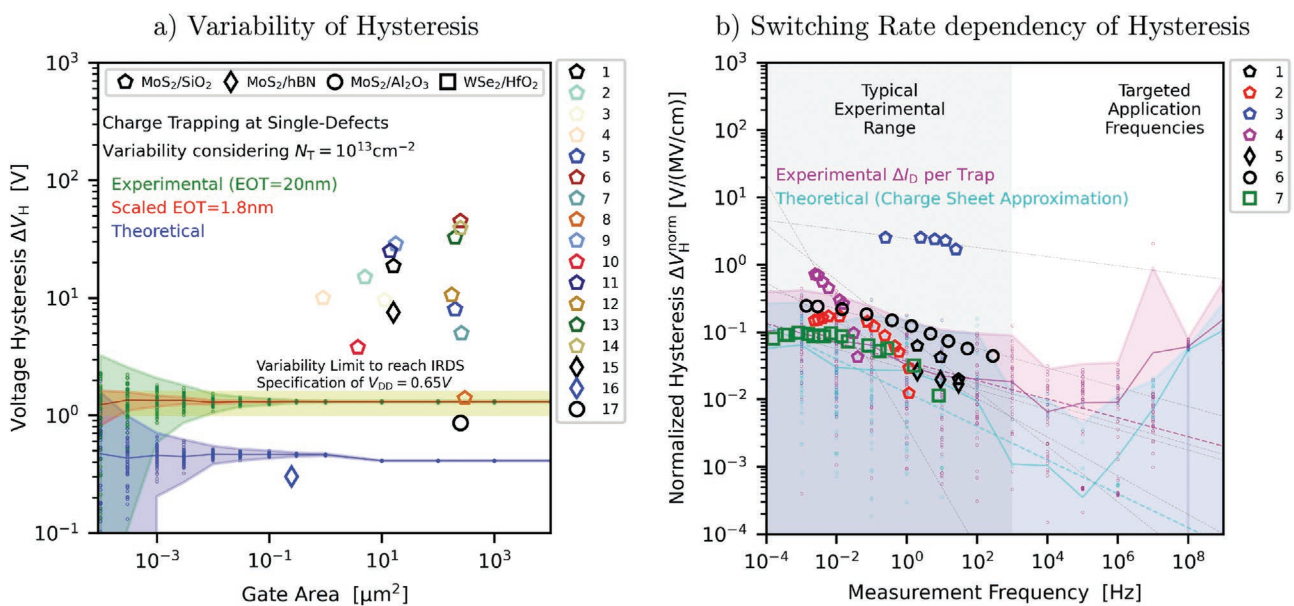


**Figure 6.** In a) the broad distribution of $\Delta V_{\mathrm{H}}$ is shown over a wide gate area range. Additionally, the limit in the variability of $\Delta V_{\mathrm{H}}$ which ensures proper operation of digital circuits at $V_{\mathrm{DD}} = 0.65$ V is marked. One can see that the current quality of 2D devices (symbols) is often not sufficient to meet the stringent hysteresis requirements. Next to the variability b) several experiments have demonstrated that $\Delta V_{\mathrm{H}}$ reduces at higher operating frequencies,[87] consistent with our simulation results. The primary reason that $\Delta V_{\mathrm{H}}$ becomes smaller at higher frequencies is because a significant fraction of the defects is no longer able to respond to the AC signal, and thus their charge state takes on an average value. Based on the current understanding of charge trapping, there is no correlation between the $\Delta I_{\mathrm{D}}$ of a defect and its trapping kinetics. Thus, defects which contribute to the large-$\Delta I_{\mathrm{D}}$ tail of the PDF could be able to interact at high frequencies, leading to failure of devices and circuits. (References: a) 1,[137] 2,[76] 3,[138] 4,[52] 5,[139] 6,[25] 7,[140] 8,[141] 9,[85] 10,[87] 11,[142] 12,[26] 13,[139] 14,[143] 15,[137] 16,[86] 17[25]); b) 1,[137] 2,[77] 3,[144] 4,[77] 5,[137] 6,[39] 7[145]).


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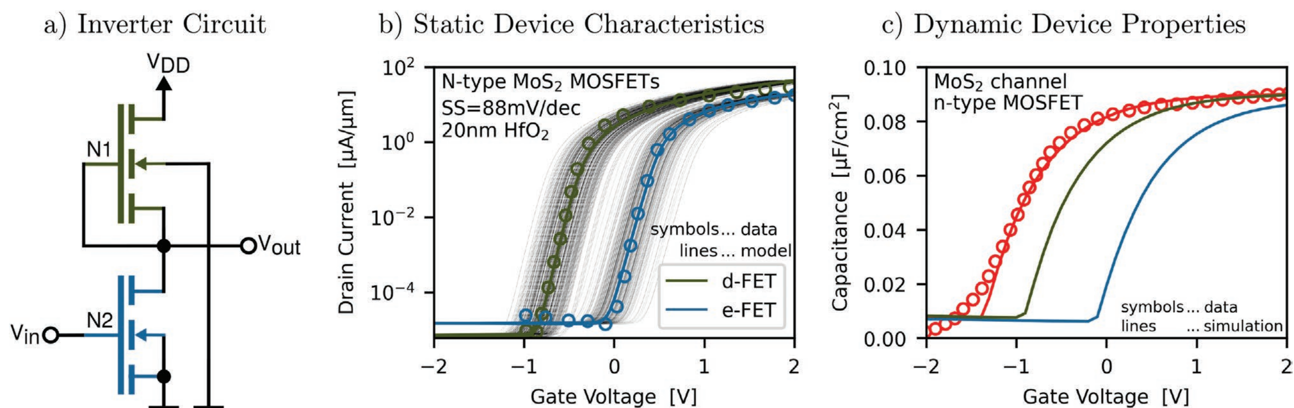


**Figure 7.** The inverter is one of the most fundamental building blocks of integrated electronic circuits. a) The schematic of a pseudo-D inverter, complementary transistors (n- and p-type) are currently not readily available for 2D technologies. The main requirement of this circuit is the combination of a depletion mode FET transistor (d-FET) $N_1$ and an enhancement mode transistor (e-FET) $N_2$ . b) The static device behavior of the FETs is described by their transfer characteristics, data taken from refs. [22,24]. c) To describe the dynamic circuit behavior parasitic capacitances have to be considered in the models, which can be extracted from CV data. However, CV data is only rarely available for 2D technologies in literature, as mostly back-gated 2D FETs are fabricated where the contribution of the capacitance of contact pads does not allow for proper CV analysis. Thus, the CV data shown in the graph is based on ref. [149] and has been transferred to $SiO_2$ oxide using the permittivity values from ref. [150]. The shown CV characteristics are consistent with other experimental studies,[135] and the model can replicate the curve. To reproduce the data set a simulation model has been used (lines).

$$\Delta V_{th} = -\frac{q}{\varepsilon_0 \varepsilon_r WL} t_{ox} \left(1 - \frac{x_T}{t_{ox}}\right) \tag{1}$$

with dielectric constants $\varepsilon_0$ and $\varepsilon_r$, the elementary charge $q$, the spatial trap position $x_T$ and the oxide thickness $t_{ox}$. It is evident from Figure 6a that the predicted variability based on the CSA (shown in blue) is much smaller than those observed in experiments, which is due to the fact that the influence of defects on $\Delta I_D$ is underestimated.[31] Several theoretical studies considering a wide range of variability sources, like random discrete dopants, have been performed for Si transistors to close this knowledge gap.[107,147] Another possible explanation is that defects can carry multiple charges and therefore should be considered as multiples of the CSA in simulations.[148] In addition to the replication of $\Delta I_D$, the correct description of the dynamic behavior of the defects through modeling is important. For this purpose, the dependence of the width of the hysteresis on the sweep rate (SR) is compared in Figure 6b to the employed model. From the measurement data on 2D transistors, a decrease of $\Delta V_H$ with SR can be clearly seen. The observed $\Delta V_H$ decreases, as fewer defects are able to follow the faster voltage ramp signals, a behavior accurately captured by the simulations. Since the proposed models correctly describe both $\Delta I_D$ and charge trapping dynamics, these models can be used to investigate the static and dynamic operating modes of circuits using 2D transistors. In addition, important evaluation criteria can be formulated to benchmark transistors made from 2D materials and to test whether 2D FETs are competitive for integrated electronics.

## 4. Challenges for Robust Electronic Circuits

The design of integrated circuits is typically based on the assumption of ideal transistors and ignores the non-idealities discussed in Section 3, which result in a reduction of performance and yield. After a brief introduction of the pseudo-D inverter, the impact of the key stability issues of transistors on the robustness of an inverter and a chain of inverters, which results in a ring oscillator, is discussed.

### 4.1. Basic Considerations for 2D Inverter Circuits

One of the basic logic circuits is the inverter. In CMOS technology, the inverter consists of a p-type FET transistor connected in series with an n-type FET. To enable CMOS circuits for 2D technologies the threshold voltage $V_{th}$ of the single transistors must be adjustable. One way to combine 2D p- and n-type transistors is to use different channel materials, for example, $MoS_2$ (n-type) and $WSe_2$ (p-type),[14,15] but the combination of various channel materials makes the on-chip integration highly complex. Alternatively, the $V_{th}$ of 2D transistors can be adjusted by intentionally doping the channel layers,[13] by adding back-gate contacts and employing the body-effect[17,151] but also by deliberately selecting different contact materials for n- and p-type transistors and exploiting the work-function difference of materials to opt for either the injection of holes or electrons.[18] In this way, CMOS inverters based on bi-layer $WSe_2$ have been demonstrated.[18] However, an alternative approach is the implementation of pseudo CMOS circuits consisting only of n-type transistors.[23,24] An nMOS inverter can be formed by connecting a depletion mode FET transistor in series with an enhancement FET transistor, see **Figure 7**a. The static and dynamic performance of the inverter is defined by the transfer characteristics (see Figure 7b) and capacitance-voltage (CV) characteristics (see Figure 7c) of the FETs used. To investigate the static and transient behavior of the inverter, theoretical models are calibrated to reproduce the transfer characteristics and the CV curves. As emphasized in Figure 2, a variety of physical mechanism exist that can cause variations of the ideal transistor characteristics and consequently affect


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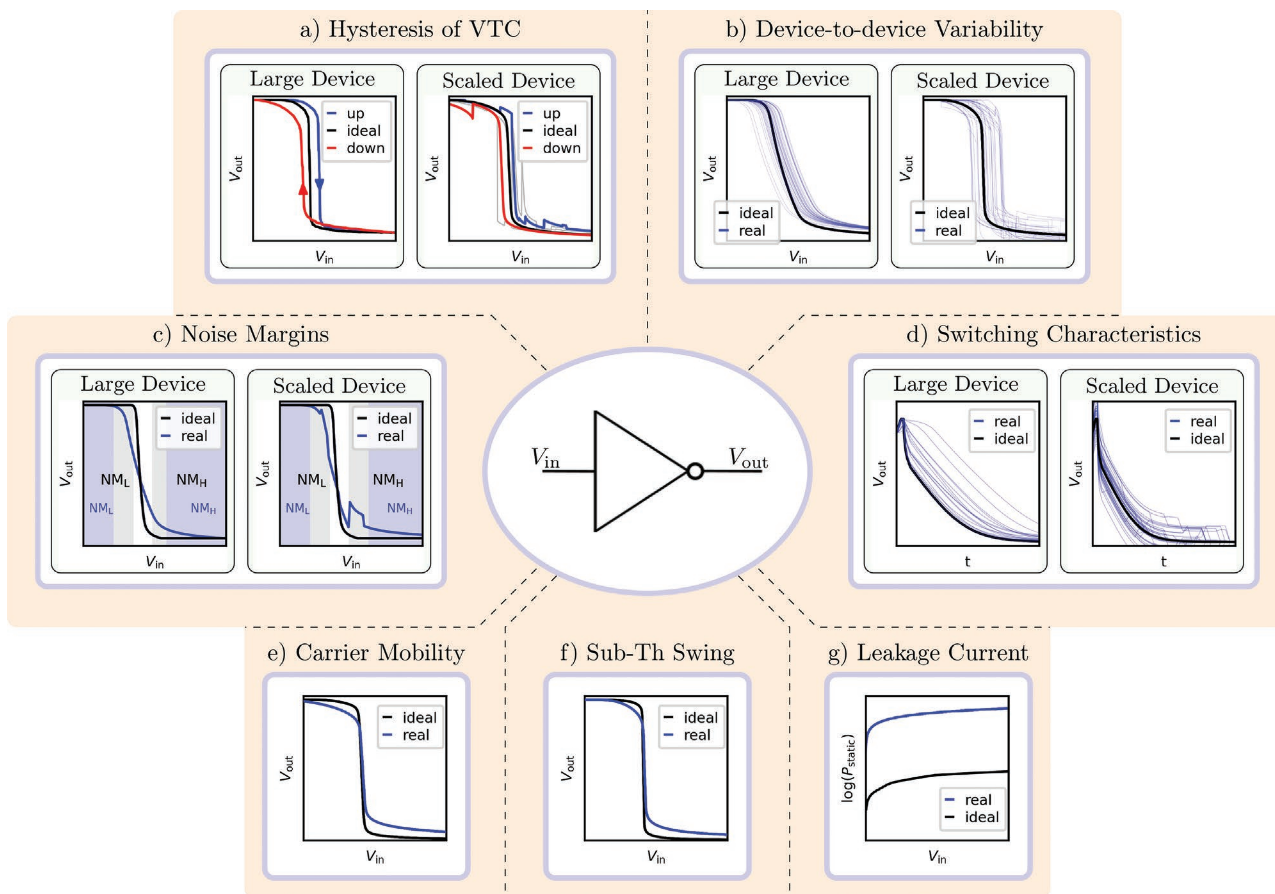


**Figure 8.** The behavior of the inverter follows directly from the static voltage transfer characteristics (VTC) and the dynamic switch-on and switch-off times. In turn, the VTC and the dynamic behavior strongly depend on the properties of the employed FETs. For example, hysteresis in the transfer characteristic of the transistors leads to a) hysteresis in the VTC of the inverter. Similarly, b) device-to-device variability issues of the FETs will also affect the switching point between the two logic levels of the inverter output. Further deviations from the ideal transistor behavior give rise to c) the widening of the noise margin and d) deviations in the dynamic behavior, for example, switching times. The slope of the VTC is further affected by e) changes in the carrier mobility as well as by f) the sub-threshold slopes. Another critical parameter is the power consumption of the circuits, which is determined by g) off- and leakage currents. Also, the impact of the individual defects in scaled transistors can be directly translated to the inverter, as indicated by the discrete steps in the behavior shown for scaled nodes in (a–d).

the behavior of the inverter. In order to evaluate the quality of 2D technologies, a comparison with benchmark criteria for circuits is essential. For 2D technologies, these have not yet been addressed in the literature. However, the knowledge of thresholds for transistor parameters like for example the maximum allowed variability of the threshold voltage, the maximum allowed sub-threshold swing or the maximum acceptable defect density are essential guidelines to characterize the achievable yield of a technology.

In the case of an inverter, non-idealities in transistors give rise to a change in the static voltage transfer characteristics (VTC) and the transient switching behavior. The consideration of both time-zero and time-dependent effects, as summarized in **Figure 8**, poses a formidable challenge to circuit designers who have to ensure immunity for the desired operating behavior against prevalent parameter changes.For instance, in the case of an inverter, deviations in the $V_{th}$ of transistors $N_1$ and $N_2$ (see Figure 7a) from its nominal value can cause asymmetrical input voltage ranges which are interpreted by the inverter as logical $1_L$ or logical $0_L$ and narrow the respective noise margins, see Figure 8c. Consequently, logic states might be misinterpreted if the output level of the previous stage deviates significantly from ground (GND) or $V_{DD}$. Furthermore, the voltage levels of the output voltage of an inverter rely on the $V_{th}$ of the used transistors as well. Therefore, for example, a drift of $V_{th,\,N2}$ can increase $V_{out}$, which can lead to falsely detected logic states in subsequent circuits. In addition to the VTC, defects in the transistors also have a significant effect on the transient behavior during switching operations and can cause substantial delays or increases in switching times, see Figure 8d.

### 4.2. Quality of Inverters Based on 2D Materials

The static behavior of the inverter from Figure 7a can be described by its voltage transfer characteristics (VTC) shown in **Figure 9**a. From the VTC the bias margins can be extracted, which describe where the inverter operates in a well-defined state. These bias margins, in turn, determine the margins of the input voltages $V_{in} \leq V_{IL}$ and $V_{in} \geq V_{IH}$, since the input signal


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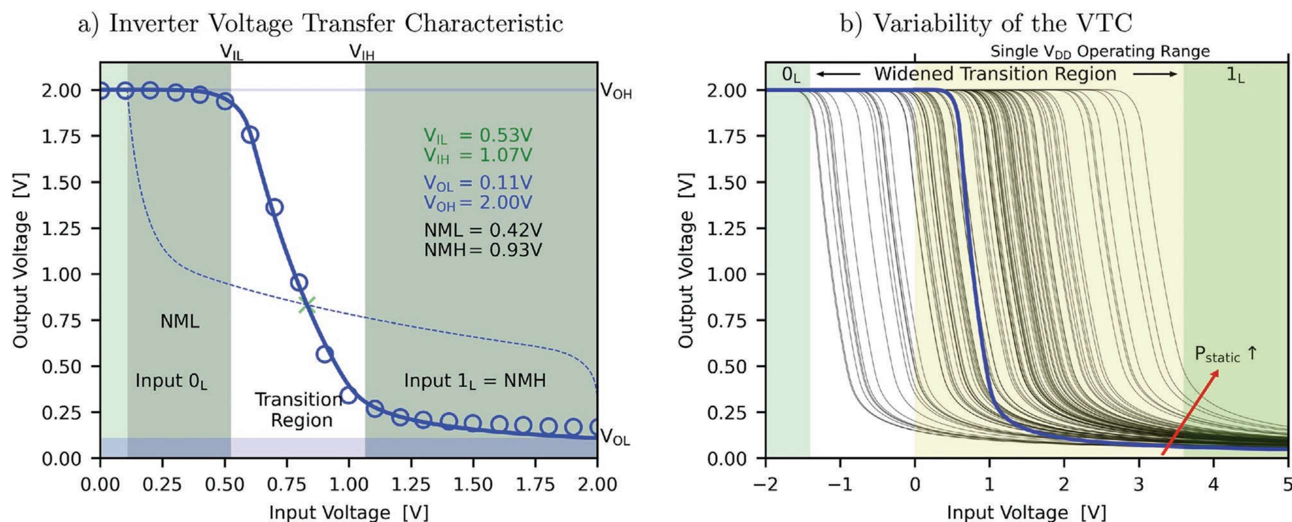


**Figure 9.** The following parameters can be extracted from the a) voltage transfer characteristics of an inverter circuit: bias levels which are interpreted as a logic low/high when $V_{IL}/V_{IH}$ are applied at the input, the output voltages representing the logic low/high state $V_{OL}/V_{OH}$, and the noise margin for logic low/high inputs NML/NMH. b) Evidently, altering the characteristics of the FETs used in the circuit changes the noise margins. Note that reduced noise margins can make a sub-circuit sensitive to noise at the input node as too high noise levels can unintentionally change the output state of a component, leading to erroneous operating behavior. In addition, the output voltage levels can also increase and thus affect the proper detection of a logic state in one of the subsequent inputs of a device.

is interpreted by the inverter as logical $0_L$ or $1_L$. Additionally, the output bias levels for the respective states are then given as $V_{OL}$ and $V_{OH}$. Note that in the case of a pseudo nFET inverter $V_{OL}$ always equals $V_{DD}$. The region with the large slope $dV_{out}/dV_{in}$ is the transition region. For this input bias range a small change in $V_{in}$ causes a large change in $V_{out}$, making the inverter unstable. The difference between the maximum $V_{in}$ which is interpreted as $0_L/1_L$, and the output voltage $V_{out}$ which is connected to the input of the next inverter, the high/low noise margins, NMH and NML can be defined, respectively. The higher NML and NMH are, the more robust the inverter is against noise from other circuit elements or external distortions, for example, radiation. A change in $V_{th}$ of either transistor $N_1$ or $N_2$ directly reduces NML and NMH, see Figure 9b, and also increases the static power consumption. The latter is especially critical for technologies which are intended for battery-powered applications.

One means to improve the energy efficiency of integrated electronic circuits is to reduce $V_{DD}$. However, this also directly affects the margins for NML/NMH and reduces the maximum permitted drift of $V_{th}$ to ensure stable operation of inverters while maintaining a high yield. In this context, in order to ensure proper operation of inverters based on equally balanced FETs, the maximum permitted variability is $\sigma_{Vth} < 30\,\text{mV}$, as shown in **Figure 10**a.

For this a maximum allowed NMH and NML of $0.1 \times V_{DD}$ is assumed for the extraction of the $\sigma_{Vth}$ boundaries.[163] A comparison with different 2D technologies shows that the $WS_2/HfO_2$ transistors discussed in ref. [152] are already very close to meeting targets for low-voltage 2D inverters, while the majority of published technologies requires further optimization to comply with the IRDS 2028 targets. In Figure 10a another tremendous challenge of nanoelectronics becomes apparent: for small $\sigma_{Vth} < 10$ mV the SS of the transistor $N_2$ becomes the limiting factor for a further reduction of $V_{DD}$. In contrast to a full CMOS inverter, $N_1$ of the pseudo-nFET inverter is always in inversion, independent of the input bias. Consequently, the SS of $N_2$ determines the slope of the VTC, see also Figure 10b. It can be observed that to reach the $V_{DD} = 0.65$ V target, a maximum SS ≈ 90 mVdec$^{-1}$ for $N_2$ is permissible. Although the results shown in literature are widely scattered depending on the fabrication process or material system used, the requirements in term of SS have already been achieved with $WS_2$ and $MoS_2$ based transistors.[22,152]

While the static VTC describes the bias levels at steady state conditions, the high-to-low and low-to-high transition times are the parameters which determine the dynamic behavior of inverter circuits, see **Figure 11**a. As can be seen from Figure 11b, the dynamic parameters can be seriously impacted by charge trapping which increases the delay times during the operation of the inverter. Furthermore, with increasing trap density the obtained variability increases which results in a jitter in the clock signals of digital circuits. In addition, large drifts of $V_{th}$ can increase the device failure rate and thus decrease the yield which becomes particularly critical for defect densities $N_T > 10^{12}\,\text{cm}^{-2}$. It should be noted that for scaled devices the variability increases (compare Figure 6a) and lower $N_T$ margins are thus necessary for an acceptable yield. Note that additional parasitic capacitances and inductances related to interconnects and vias are not considered in the presented analysis; however, these parasitic effects will lead to even more stringent criteria for $\sigma_{Vth}$ and $N_T$, in particular for devices operating at high frequencies of several GHz and above.

### 4.3. Performance of Scaled 2D Ring Oscillators

Ring oscillators (ROs) are widely used in integrated circuits for a variety of applications: for example, ROs are applied as


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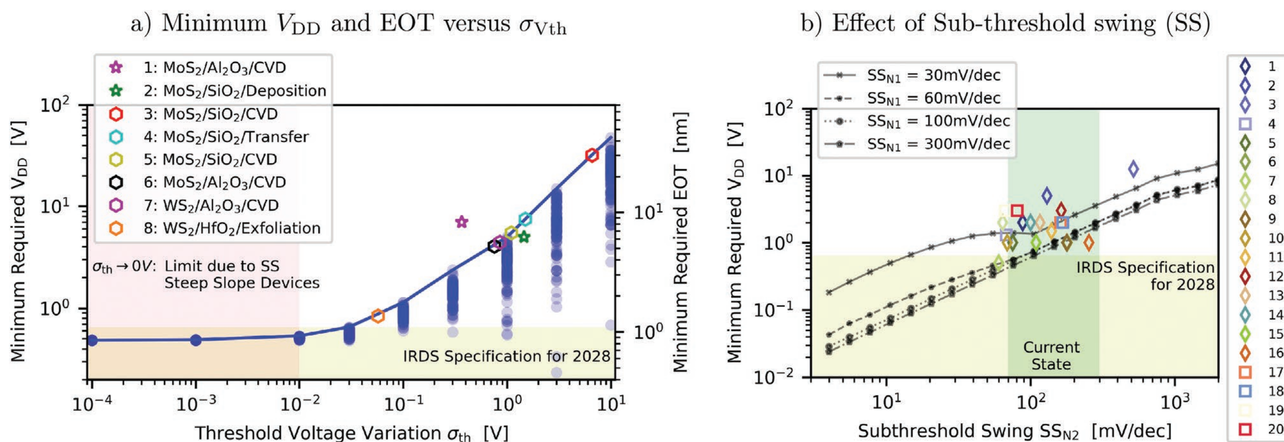


**Figure 10.** Demands on 2D transistor technologies to enable circuits operating at conditions targeted by the specification of the IRDS for 2028.[134] a) The left graph illustrates how the variation of $V_{th}$ of $N_1$ and $N_2$ of the inverter affects the minimum required $V_{DD}$ to achieve noise margins NML and NMH of at least $0.1 \times V_{DD}$. As can be seen, the SS of transistor $N_2$ from the inverter circuit becomes the limiting factor for achieving this goal if the distribution of $V_{th}$ approaches $\sigma_{Vth} < 10$mV. Among the large number of material systems discussed in the literature on 2D transistors, we found only one technology, namely exfoliated $WS_2$ with $HfO_2$ as an insulator, which appears to fulfill this requirement at least for the time-zero $V_{th}$ distribution.[152] b) The SS of $N_1$ and $N_2$ also affects the behavior of the pseudo-D inverter and are an important factor toward minimum achievable $V_{DD}$. Since $N_1$ is continuously operated in the on-state because $V_{in} > 0$V, the switching behavior is determined by the slope of $N_2$. It can be seen that for a SS of $N_2$ below 80 mV dec$^{-1}$ the desired $V_{DD} = 0.65$ V can be achieved. (References: a) 1,[23] 2,[16] 3-4,[27] 5,[79] 6-7,[113] 8;[152] right b) 1,[22] 2,[21] 3,[153] 4,[152] 5,[154] 6,[155] 7,[58] 8,[156] 9,[157] 10,[86] 11,[112] 12,[158] 13,[159] 14,[160] 15-16;[161] 17-18;[162] 19-20;[19] targeted $V_{DD}$= 0.65 V according to IRDS[134])

test structures for measuring the signal propagation time of inverters,[164] for determining die-to-die and across-wafer variability,[165] for measuring the chip temperature,[166] or directly as voltage-controlled-oscillators (VCOs) in phase-locked loops (PLLs).[167] ROs are constructed by connecting an odd number of inverters in series, with the output of the last inverter fed back to the input of the first one, see **Figure 12**a. Consequently, the oscillation frequency of the RO depends on the input capacitance of the input stages of the inverters. As discussed in Figure 11a, a variation of the $V_{th}$ of the transistors employed in the inverter stages leads to a change of the signal amplitude of the RO, thereby causing a considerable variation of the oscillation frequency $f_{osc}$, see Figure 12b. In the case of an RO built from equally balanced inverter stages, a maximum

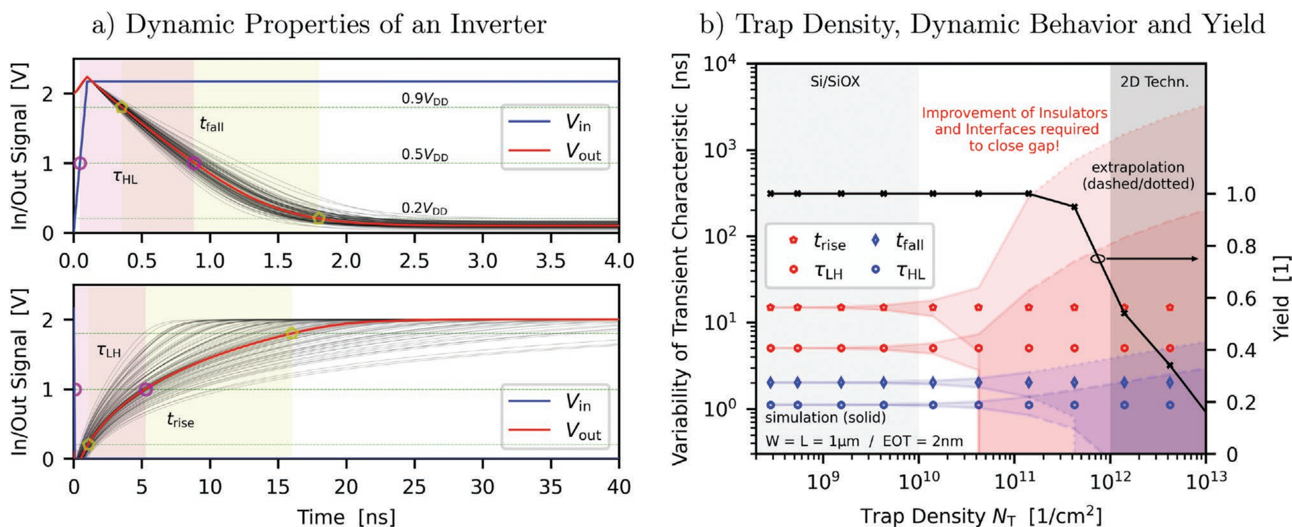


**Figure 11.** To evaluate the impact of trap distributions on the dynamic behavior of an inverter we inspect the a) high-to-low and low-to-high transition times $\tau_{HL}$ and $\tau_{LH}$ when the output of the inverter is connected to an input transistor of a subsequent block (the symbols mark the intersection points which are considered to extract the timing parameters). b) Considering the impact of a trap according to the PDF from Figure 4c and the trap bands from Figure 5 the variability of the transient inverter characteristics is extracted. For a trap density exceeding $N_T > 10^{11}$ cm$^{-2}$ a significant variation of the timing characteristics can be observed. Note that the variability deteriorates at scaled nodes. In addition, if a large number of traps is present, this can lead to the malfunction of circuits, which becomes evident as a drop in the yield when $N_T$ approaches $10^{12}$ cm$^{-2}$. Considering the properties of the 2D transistors discussed in literature there is still an improvement of two orders of magnitude of $N_T$ required for this novel technology to be suitable for digital electronic applications.


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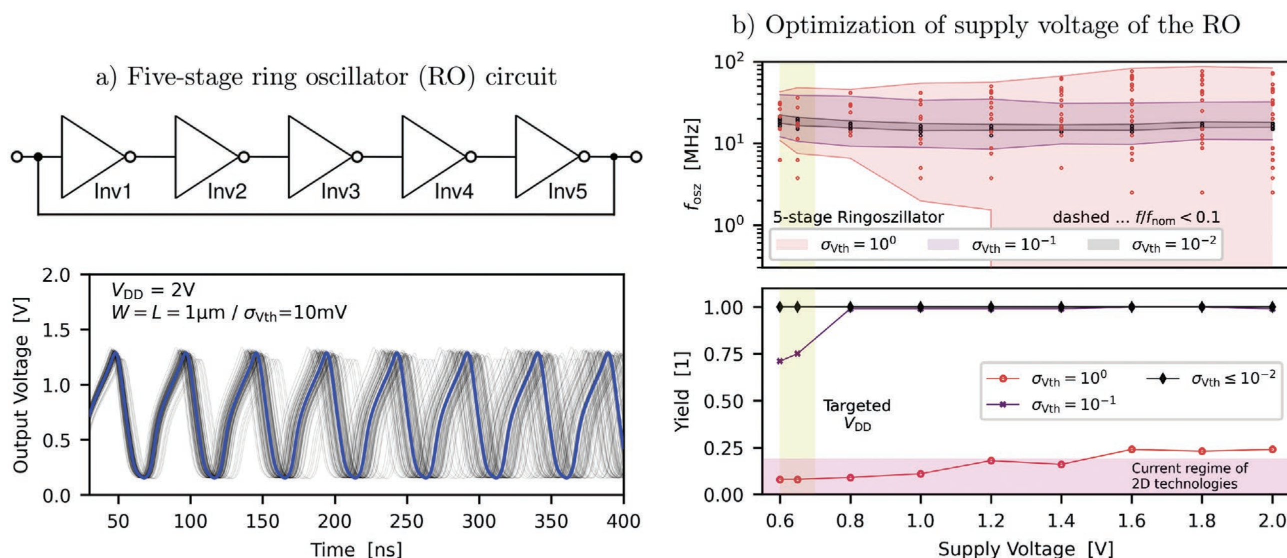


**Figure 12.** a) It can be seen that a change in the threshold voltage of the transistors leads to a shift in the oscillation frequency of the original signal in a five-state RO. Also, the amplitude of the voltage signal can be reduced, making the circuit more vulnerable to external noise sources. b) In this context, we have investigated the influence of reducing the supply voltage and the threshold voltage variation as required by the IRDS. In order to guarantee a minimum deviation of the oscillation frequency from its nominal value, the threshold voltage must not deviate by more than 30 mV ($3\sigma_{Vth}$) from the target value. Here, the sum of time-zero variability and parameter change during operation is considered. Furthermore, it is shown that only a poor yield is obtained for current 2D technologies ($\sigma_{Vth} \approx$ 1V), in addition to the observed enormous variation of the oscillation frequency.

variability of $\sigma_{Vth}$ < 30mV has to be ensured to guarantee a maximum reduction of the oscillation frequency by 10%. Furthermore, an optimization of $V_{DD}$ toward the target value of the IRDS[134] drastically reduces the yield for technologies which exhibit a significant $\sigma_{Vth}$. The technologies discussed in the literature are currently in the range of $\sigma_{Vth} \approx$ 1 V, as summarized in Figure 10a. For these values, a yield of about 25% would be obtained, rendering these technologies uneconomical. Note that for the lifetime evaluation for Si transistors a maximum allowed drift of the threshold voltage of $\Delta V_{th}$= 30 mV is often used as a criterion for Si technology[168–171] and circuits.[172,173] However, the criterion for $\sigma_{Vth}$ cannot be considered independently from the SS of the transistors employed. In fact, a steep slope of the transfer characteristics can compensate for a slightly larger $\sigma_{Vth}$, while a narrow $\sigma_{Vth}$ is mandatory for technologies which exhibit larger values of SS.

In addition to the static variability of $V_{th}$, charge trapping also affects the dynamic behavior of ROs. Charge capture and emission events can cause substantial noise spikes in the voltage signals of scaled ROs, see **Figure 13**a. Furthermore, during operation, a defect can be activated[174] which generates an RTN signal which cyclically switches the RO on and off. Along similar lines as for transistors, the influence of charge trapping at defects gives rise to a considerable variation in the behavior of the ROs. This variation becomes substantially more pronounced for transistors with scaled device dimensions Figure 13b. A comparison with Si technology shows that, while in Si a lowering of the resonance frequency stays below 2% of the nominal frequency, for current 2D technologies a drop of more than 30% is to be expected. It should be noted that the variation of $f_{osc}/f_{nom}$ strongly depends on the PDF of the step heights of the defects. This means that, in addition to the optimization of $N_T$, the impact of individual defects $\Delta I_D$ must be minimized as well for future 2D technologies.

## 5. Suitability of 2D Technologies for Memory Applications

Conventional memory banks employed in integrated electronic applications are based on static random access memory (SRAM) or dynamic RAM (DRAM) cells. However, as SCEs and reliability issues in sub-10 nm nodes become increasingly dominant, alternatives to traditional memory concepts have been investigated. For instance, magnetic RAM, resistive RAM, phase-change RAM, and ferroelectric RAM have been developed recently.[175] Following the introduction of 2D transistors, the feasibility of memory cells based on this novel material system has been investigated as well. Meanwhile, prototypes of various kinds of memory have been successfully produced. A CMOS-like SRAM cell, for instance, has been fabricated employing $WSe_2$ as the channel material[151] as well as an nFET-only SRAM cell using $MoS_2$ for the channel.[22] Besides the challenges arising during the complex fabrication processes, the stable operation of memory cells relies on the reliability of the employed transistors. Both time-zero and time-dependent variations of $V_{th}$ due to charge trapping at the interface and insulator defects give rise to variability in noise margins of the circuits. Because especially the characteristics of 2D transistors significantly vary between devices of the same lot, an in-depth evaluation of the key requirements to maximize noise margins and minimize variability is an essential quality criterion for a new technology. As SRAM cells are widely used in electronic applications due to their on-chip implementation, enabling the fastest access times to individual memory cells, 2D-based SRAM cells are analyzed in the following.

The most prominent example of SRAM cells is the 6T-SRAM which consists of two inverter stages, formed by $N_2/N_3$ and $N_4/N_6$, where the output of one inverter is connected to the input of the other inverter, see **Figure 14**a. During operation,

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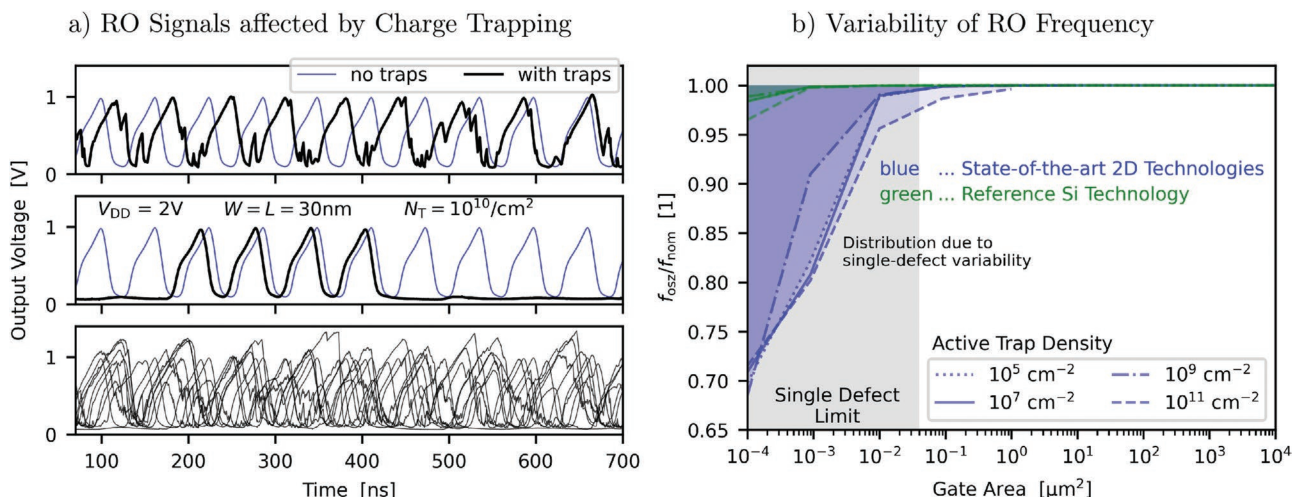


**Figure 13.** For scaled technologies, the analysis of the influence of single defects on the behavior of circuits is essential. a) Simulations demonstrate that the charge transitions of single oxide defects directly impact RO signals, see (a) top. Interestingly, a single RTN defect can switch the ring oscillator on or off, see (a) center. At the bottom, various possible time signals are shown, demonstrating that defects are responsible for a considerable variation in the behavior of the RO. b) For current 2D technologies, one can expect a deviation of the oscillation frequency of up to 30%, compared to deviations smaller than 5% for Si technologies. Particularly interesting is that these are independent of the active defect density. This is due to the fact that the variance of $f_{osc}$ is determined by the distribution of step heights of defects from Figure 4c. A lower defect density boosts the yield of ROs operating within the specific frequency. To make 2D transistors competitive, however, the influence of the traps on the behavior must be reduced in addition to the trap densities.

this means that the outputs $V_Q$ and $V_{\bar{Q}}$ of the inverters each store the inverted states of each other. One performance parameter of the SRAM is the hold static noise margin (HSNM) which describes the amount of noise required to change the state of the SRAM cell and to consequently cause data loss. The HSNM can be extracted from the butterfly curve of the SRAM cell, as created from the VTCs of the two inverter stages, see Figure 14b. Therefore, the HSNM depends on the performance parameters of the transistors used, that is, threshold voltages and carrier mobilities. When designing SRAM cells, typically matched transistor pairs are assumed, that is $V_{th,\ N2} = V_{th,\ N4}$ and $V_{th,\ N3} = V_{th,\ N5}$. Any deviation from this perfect matching will lead to a change in the performance of the SRAM cell and to a reduction of the HSNM. In general, an important advantage of the SRAM cell is that it is available in all dimensions due to its CMOS compatibility. However, since transistors variability effects are more pronounced in scaled nodes, the variability of scaled SRAM cells is also higher.[176–178] In fact, charge transitions of single defects will have an impact on the butterfly curve of scaled SRAM cells. In a first order

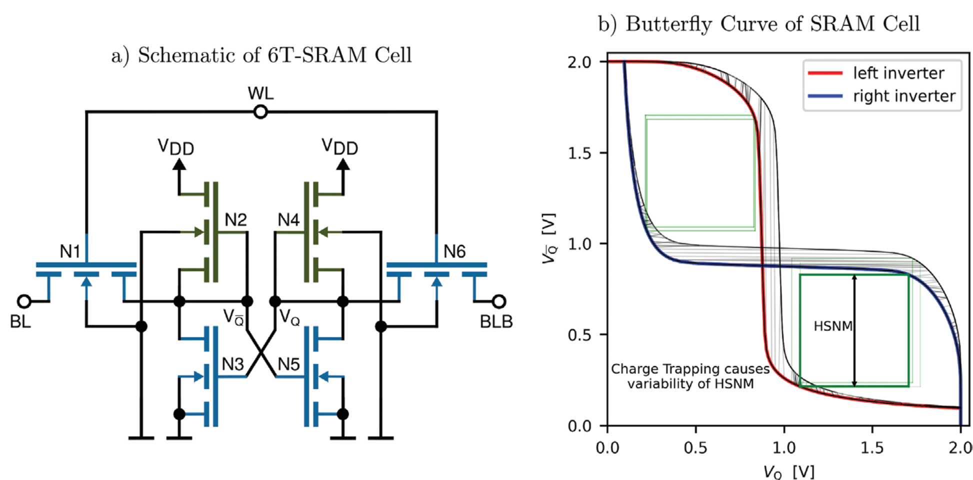


**Figure 14.** a) A very prominent circuit used in electronics is a the 6T-SRAM cell. It consists of two inverter circuits formed by the transistor pairs ($N_2$, $N_3$) and ($N_4$, $N_5$), where the output of each sub-inverter is connected to the input of the other inverter. The two transistors $N_1$ and $N_6$ serve as access transistors and are turned on during write or read operations. b) The static operating characteristics of the SRAM cell represented by its so-called butterfly curve. The width of the eye indicates the hold static noise margin (HSNM) of the cell and depends, amongst other parameters, on the device threshold voltage. As can be seen, charge capture and emission events at defects in the transistors result in discrete steps in the SRAM characteristics. This leads to a lowering of the HSNM of the cell.


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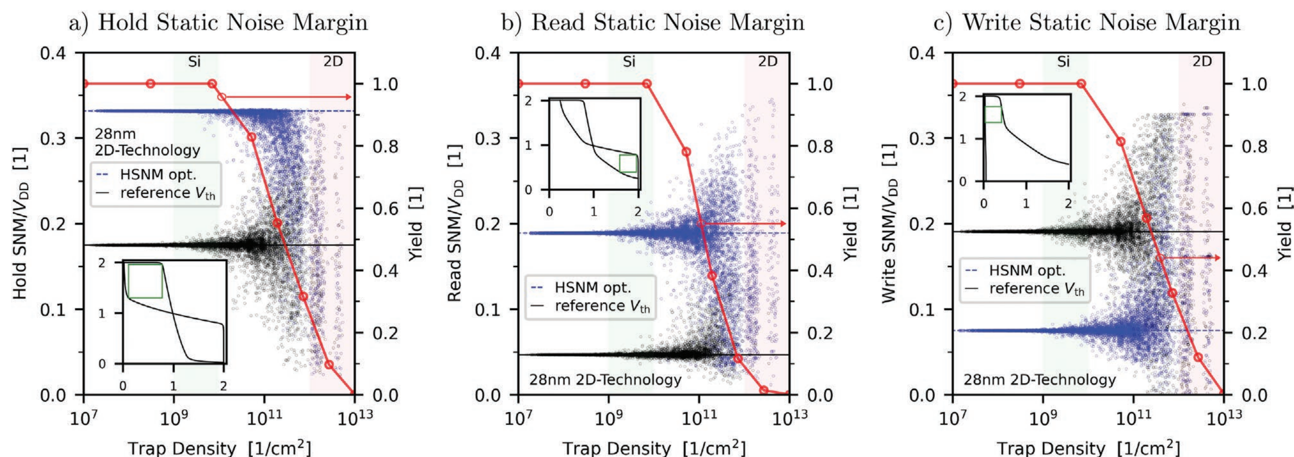


**Figure 15.** The a) hold SNM, b) read SNM, and c) write SNM are the basic parameters determining the quality of the 6T-SRAM cell. We compare two theoretical 28 nm 2D technologies. First, one where the transfer and CV characteristics for the depletion and enhancement FETs have been matched to Figure 7 (black), that is, $V_{th,\ e\text{-}FET} = -0.15$ V and $V_{th,\ d\text{-}FET} = -0.95$ V, and second, one the $V_{th}$ has been optimized to achieve maximum hold SNM (blue), that is, $V_{th,\ e\text{-}FET} = 0.5$ V and $V_{th,\ d\text{-}FET} = -0.73$ V. In the case of an ideal (but impossible) sharp transition between $1_L$ and $0_L$ the maximum value of SNM/VDD = 0.5 would be achieved. However, even with ideal SS values, possible values for SNM/VDD are considerably lower. In addition, at a trap density above $N_T > 10^{10}$ a large variability in the SNM can be observed in all three cases. This is a consequence of the distribution of the impact of the defects on the device characteristics. Note that the yield also considerably reduces when $N_T$ increase which means that the majority of SRAM cells at larger $N_T$ do not operate properly, and only a few "lucky" circuits can be used. Furthermore, note that to optimize the HSNM for this particular technology a $V_{th}$>0 V is required while $V_{th}$<0 V is demanded for the other FET type. Thus, a precise control of $V_{th}$ is a mandatory feature to ensure to success of 2D electronic applications.

approximation, defects causing RTN when GND or $V_{DD}$ is applied at the gate mainly influence the plateaus of the butterfly curve, as here the applied gate voltages are nearly constant. At the same time, BTI related defects affect the SRAM cell performance during state switching processes. These defects have a considerable impact not only on the hold state, but also on the performance during read and write operations, as evaluated in **Figure 15**.

In order to read or write the state of the SRAM cell, the outputs are connected via the enhancement mode access transistors $N_1$ and $N_6$ to the bit lines (BL). In turn, the bit lines link a large number of SRAM cells in the form of a matrix array. In such an array, the state of the access transistors $N_1$/$N_6$ is controlled by the write line (WL). Potential instabilities of the SRAM cell occur mainly during read and write accesses when the inputs of the inverter stages are connected to the control electronics via the access transistors. During the read process the two bit-lines, BL and BLB, are pre-charged to logic $1_L$. Thus, at the beginning of the read process the drain nodes of the drive transistors, that is, $N_3$ and $N_5$, are pulled from the logic $0_L$ state toward $V_{DD}$ via the voltage divider formed with the access transistor. If due to charge trapping the drain potential at the entry point rises above $V_{th}$ of the driver transistor of the second stage (either $N_3$ or $N_5$), the stored state of the cell switches. In turn, wrong data would be read out. This situation is described by the read SNM (RSNM). The RSNM defines the maximum noise level up to which the data can be read correctly, see inset of Figure 15b. In contrast, the write margin provides a measure for the programming of the SRAM cell to a defined state. If noise levels at BL or BLB are larger than the write SNM (WSNM), erroneous write operations may occur. In all three cases, a reduced margin indicates poor robustness of the SRAM cell which leads to undesired behavior.

An evaluation of the SNM for a 6T-SRAM cell considering a 28 nm 2D transistors technology is summarized in Figure 15. Our results are based on the reference transistors from Figure 7 and are contrasted with a technology optimized for maximum HSNM. In all three cases, one can see a pronounced variability of the SNMs, which increases dramatically for $N_T > 10^{10}$cm$^{-2}$. It should be noted that in the plot the density of data points is an indicator for the yield. This means that, when considering the defect density currently achieved for 2D transistors, only a few lucky circuits will function after fabrication. Therefore, in order to render memory chips based on 2D transistors competitive for industrial applications, the defect density needs to be reduced by 2-3 orders of magnitude.

In addition to the robustness against noise, the ability to write and read data at high rates is among the most important performance metrics of the SRAM. These access times of the SRAM cell are determined by the gate capacitances of the driver transistors $N_3$ and $N_5$ and of the inverter stages, that is, $N_3$ and $N_5$, as well as the current through both the access and driver transistors. However, charge trapping induced drift of $V_{th}$, in turn leads to a reduction of the on-current, which consequently reduces the write and read times. Thus, the variability of the access times strongly depends on the number of defects in the transistors. Consequently, the aforementioned required reduction of $N_T$ is expected to positively affect the timing. Furthermore, a lower trap density will effectively increase the carrier mobilities in the channel. In turn, this will improve the inversion current provided by the access transistors, resulting in a reduction of the access times. Another key parameter for SRAMs is the data retention time, which depends on off-state drain currents and gate leakage currents across the insulator. In order to obtain minimum off-state currents, $V_{th}$ and SS need to be optimized, among other things. For an improved


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SS, transistors can be switched off effectively even at reduced $V_{DD}$. With respect to the off-current, charge trapping can lead to a time-dependent decrease of the $V_{th}$, thereby shifting the *I-V* characteristic of the FETs toward lower voltages, and thus increased off-currents can emerge during operation. In terms of gate leakage currents, research efforts have been devoted to identifying high-quality insulators for 2D material based FETs recently.[62,179] Ideally, these insulators should form an almost defect free van der Waals interface with 2D materials, can be deposited in atomically thin crystalline layers, and exhibit almost negligible gate leakage currents. In recent investigations $CaF_2$[89] or $Bi_2SeO_5$,[144] have shown promise for being used as gate insulators for 2D FETs which, in turn, could potentially open up the path for 2D memory applications.

## 6. Perspective of 2D Electronic Applications

For over a decade, the fabrication of novel transistors based on 2D materials, such as BP, $MoS_2$, $WS_2$, and $WSe_2$, has been discussed in numerous publications. These ongoing research efforts target an optimization of performance parameters such as the SS, the channel carrier mobility, and the on/off current ratio. At the same time, suitable methods for threshold voltage adjustments have been investigated including, for example, different gate materials or chemical and electrical doping strategies. In fact, a precise control of these parameters will be required for a successful integration of 2D transistors in advanced electronic circuitry. Recently, first prototypes of inverters,[17] logic gates,[24] as well memory cells based on 2D semiconductors[151] have been fabricated. However, at the moment these prototypes suffer from large process-related parameter variations as well as considerable aging during operation. Note that a control of aging is essential for failure-safe and long-term operation with sustained device performance, which will be decisive for the introduction of 2D circuits at the industrial scale. In general, the margins for key parameters to ensure stable transistor operation must be considered individually for each application scenario. As an overarching trend, two important criteria for robust circuits are the number of electrically active defects per transistor as well as the average influence of a defect on the transistor behavior. Frequently, a low absolute number of defects is considered to be a measure of the quality of a technology. Note that the number of defects which contribute to observed changes of a device characteristics depends on the measurement technique used. Thus, the defects which can follow the voltage signals during operation lead to a dynamic change of the *I- V* characteristics and affect the stability of applications.[41] From this, it can be concluded that the electrically active number of traps and their step heights $\Delta I_D$ are the important measures for evaluating 2D electronic circuits. An overview of the requirements is shown for Si and 2D technologies in **Figure 16**. The margins for maximum yield, thus ensuring a minimum failure rate during operation, are extracted from the previously discussed analysis (see Figures 11, 12, and 15) and are also shown. Currently, the number of active defects is still considerably higher than that of Si technology. The impact of a single defect is reflected by the height of the boxes, which is observed to be slightly above the values observed in Si technology. Note that this effect is important for device quality evaluation, but has so far not been considered in literature. Such defects are assumed to be located close to or directly at the channel/insulator interface of 2D transistors.[40,91,184] The width of the boxes represents the gate area and a scaled EOT = 1 nm has been considered as operation at low $V_{DD}$ is targeted. As a results, scaled 2D transistors for applications at high frequencies in the range of several MHz to GHz already show very promising characteristics. Especially the material combination of $hBN/MoS_2/hBN$ shows the smallest defect numbers among studied 2D materials as well as the smallest influence of individual defects on the current flow. Unfortunately, the large leakage currents in scaled hBN layers, which are not considered in this study, will likely endanger successful operation of this material system.[44] We also remark that the charge trapping and giant RTN steps as observed in Figure 4b can be beneficial for certain applications, for example, in random number generators where a variation of $f_{osc}$ of a RO is induced by the statistically distributed charge transitions of the single defects. A more pronounced impact of a defect is, in this case, advantageous, since they can lead to easily detectable $\Delta f_{osc}$.

A further application for 2D material based FETs to augment and enhance the functionality of Si CMOS chips is via back-end-of-line integration, that is, 3D monolithic integration. As 2D materials can be grown on a variety of substrates and transferred to any arbitrary surface, either additional layers of logic circuitry or memory cells as well as gas sensors, optical receivers, or image sensors,[185,186] can be seamlessly integrated with current Si CMOS technologies. In addition, multiple layers of 2D FETs could be stacked on top of each other to enhance the current drive while maintaining low off-state currents.[187]

The use of 2D materials to build memristive cells and neuromorphic circuits is another emerging application.[188–190] Here, conventional digital logic circuits based on 2D materials can be directly integrated with memristive crossbar arrays for neuromorphic computing.[191] Also, due to the large surface to volume ratio, 2D materials are excellent candidates for sensors[192–194] in combination with Si-based or 2D-based control electronics. As 2D materials form few atoms thin layers the resulting sheets are also inherently flexible, opening up a market for flexible electronics.[195]

Overall, there is enormous potential of 2D materials in electronic applications; however, considerable improvements are still required in terms of time-independent variability, that is, reproducibility of devices to remain within well defined specifications, but also stability, that is, time-dependent effects. The limits for the key properties of transistors evaluated in this work provide guidance for further advancement of 2D material systems and will support the future development to bring 2D electronics closer toward being a valuable add-on or even a serious competitor to Si-based chips.

## 7. Conclusion

Due to the ongoing industry push for the miniaturization of Si-based transistors, an enormous increase in performance of electronic applications has been achieved in the past decades.


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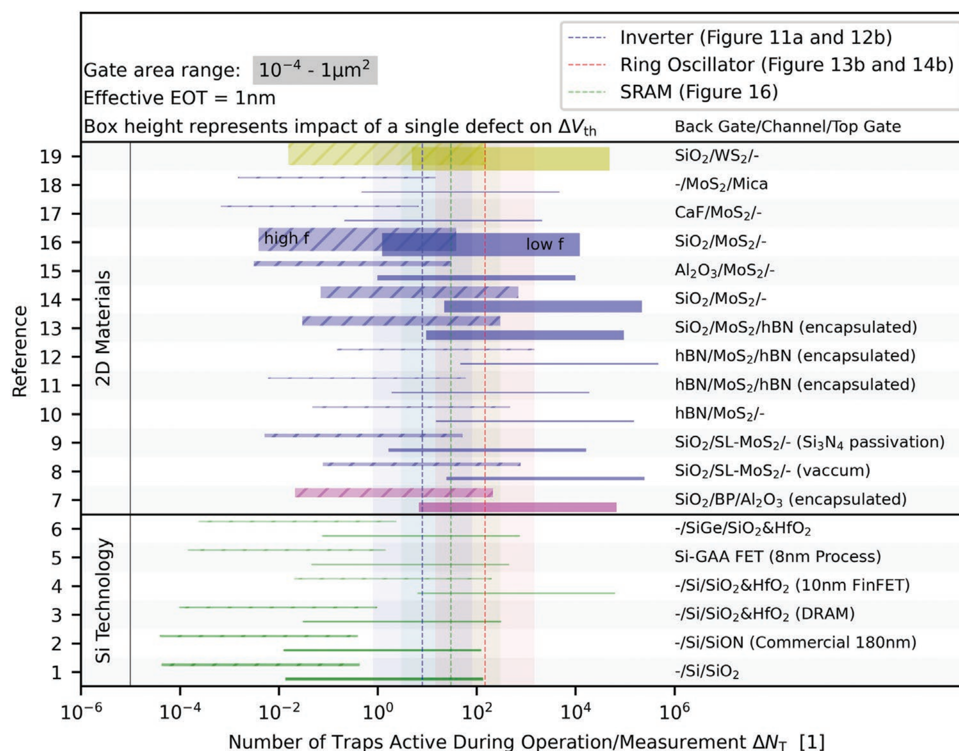


**Figure 16.** Based on evaluations of the performance of 2D technologies, we identify the major factors which are essential for ensuring robust operation. These factors are the number of electrically active traps and their charge trapping kinetics, as well as the variability of $V_{th}$. The combination of the number of defects per transistor and the influence of a single defect on $I_D$ (represented by the height of the boxes) reduces the stability during operation. A comparison of different Si technologies with state-of-the-art 2D transistors shows that, in addition to a high number of defects, the influence of the individual defects, that is $\Delta I_D$, is also more pronounced in 2D materials. It is noteworthy that operation at frequencies in the GHz range (hatched boxes) inherently reduces the number of active defects. As a result, some 2D technologies already meet the stringent criteria for failure-safe operation of inverter, RO, and SRAM circuits. In fact, a box which is entirely below the three vertical dashed lines could, in principle, be used to build fully functional inverters, ring oscillators, and SRAM cells. For 2D transistors, this is currently only achieved in a few examples (e.g., nr. 17) and only for high frequency operation. Therefore, in order to firmly establish 2D electronics, it is necessary to further optimize the quality of interfaces, which entails a reduction in the number of defects and their impact on the devices. In principle, both challenges are perfectly suited to the chemically inert surface of 2D layers. As soon as equally inert surfaces of good gate insulators are found, these technologies will be on-track to shape the future of electronic applications. (References: 1,[31] 2-3,[60] 4,[180] 5,[181] 6,[93] 7,[126] 8-9,[76] 10-11,[86] 12-13,[137] 14-15,[25] 16,[59] 17,[89] 18,[182] and 19[183]).

However, few nanometer sized Si transistors are plagued by severe SCEs which are observed as limited gate control and reduced charge carrier mobilities, for instance in 3 nm GAA technologies. Both effects pose serious challenges for the efficiency of future circuits. A further goal of the semiconductor industry is the functional integration of digital circuits with a large set of applications including sensors, RF circuits, and memory, leading to non-digital system-in-package and digital system-on-chip integration for a higher value system. However, with the discovery of 2D materials, which might be better suited for these functionalities, the limitations of silicon may be overcome.

2D materials could potentially overcome these limitations in scaling and functional integration, mainly because they can be fabricated as monoatomic sheets. At the current state-of-the-art, the operation of transistors and circuits designed using 2D materials has been demonstrated at the prototyping stage. However, the performance of 2D transistors suffers from defects present at the channel/insulator interface as well as in the insulator, which can considerably degrade the characteristics of the devices. While such defects are in principle well known from Si technologies, a higher defect density and a larger impact of individual defects on the current flux is observed in 2D transistors when compared to Si devices. This entails a pronounced variability in the device behavior. Therefore, the design of robust electronic circuits based on 2D semiconductors is very challenging at the current state of the art, as both time-independent and time-dependent effects must be taken into account.

It should also be noted that, for 2D materials in particular, defects which produce giant steps in the device current are observed. These defects contribute to the tail of the step height distribution function and are a decisive factor for the yield of a technology. It is demonstrated that such "killer-defects" increase circuit variability and decrease the yield. However, note that the conclusions made for small circuits do not easily translate to large microprocessors and require a careful individual evaluation.

To provide guidance for the optimization of this emerging technology, limits for changes in the threshold voltage, sub-threshold swing, and carrier mobility, which ensure proper functionality have been established here. It should be


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noted that the absolute number of defect-related fixed charges leads to a static change of the threshold voltage of a transistor, which can be compensated in the circuit design. However, the dynamic behavior of interface and insulator defects described by charge capture and charge emission times as well as their influence on the current is critical for the long-term stability of electronic applications. A comparison with Si technology shows that, for 2D transistors, an optimization of both the number of defects and their influence is necessary if this technology is to reach an industrial mass-production level. For this purpose, the interface between the channel and insulator layers plays a decisive role. Several 2D technologies, mostly based on the $MoS_2$/hBN material system, exhibit performance values close to those observed in Si devices. Unfortunately, hBN will likely lead to excessive leakage currents when scaled down to EOT = 1 nm. Overall, considerable improvements are still required in terms of the reproducibility of 2D devices in order for them to operate within well-defined specifications. Furthermore, 2D device stability, that is, time-dependent effects, must be improved before 2D circuits can become suitable for consumer electronics. To achieve this goal, the limits extracted in this work may serve as a guide for the evaluation of further optimization processes.

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## Conflict of Interest

The authors declare no conflict of interest.

## Keywords

2D materials, circuit performance, defects in semiconductors, device and circuit reliability, integrated electronic circuits, static random access memory, technology yield

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