Electrolithic Memory: A New Device for Ultra-High Density Data Storage

Senne Fransen, Kherim Willems, Harold Philipsen, Devin Verreck, Willem Van Roy, Olivier Y. F. Henry, Antonio Arreghini, Geert Van den bosch, Arnaud Furnémont, and Maarten Rosmeulen

***Abstract*—We propose a storage memory device that enables bit densities of >1 Tbit/mm² based on the electrodeposition and -dissolution of multilayered metal stacks in deep nanometer-sized wells. This device addresses the challenge of bit density scaling slowdown expected for 3D NAND flash beyond 2030. We describe in detail the operating principles and discuss the response time, bandwidth, retention, and cycling endurance requirements for the device to be viable. As a proof-of-principle, we provide a first demonstration of the write/read mechanism on millimeter- and micrometer-sized electrodes and show the device's potential for reaching very high bit densities. To evaluate how the response time scales for the envisioned nanometer-sized electrodes, we derive simple analytical expressions based on finite element simulations that relate the well depth, radius, and electrolyte composition to the deposition/dissolution rate.**

***Index Terms*—Non-volatile memory, High-density data storage, post-NAND technology.**

I. Introduction

NAND flash memory established itself over the past decades as the dominant, low cost-per-bit, large capacity semiconductor storage device. While NAND data access time cannot compete with active memory technologies (e.g., DRAM or SRAM), parallelization of flash memory control circuits allows for high bandwidths, making NAND flash well suited for data storage applications. Furthermore, the low energy consumption and compactness compared to hard disk drives, made it the preferred storage solution for mobile devices [1]. Today's products exploit the third dimension by stacking multiple cells on top of each other, making the NAND memory string run vertically, with tremendous benefits to bit density and a reduction of the cost-per-bit. Currently, the gross bit storage density of 3D NAND flash is reaching 10 Gbit/mm^2 and increases roughly by a factor 40 every 10 years [2]. At this rate it is projected that devices with bit storage densities of 1 Tbit/mm^2 will be in production before 2035. However, attaining such a high bit density would require an extremely challenging number of programming levels, memory cell stacking height, and vertical and horizontal pitch of the individual cells [3-6].

Inevitably, the question arises how the memory landscape will evolve after 3D NAND has saturated. A likely outcome is the emergence of different device classes. Some product types will prioritize random access latency [7], whereas others will emphasize the relentless efforts to reduce the cost-per-bit [8]. Despite degraded latencies, these high-density memories can maintain large data transfer bandwidths by use of parallel addressing and low-latency data buffers.

The critical features enabling high bit densities are already apparent from developments in 3D NAND: maximally using the vertical dimension and storing more than one bit per cell. Yet, this cannot be fully exploited by 3D NAND as each cell in the vertical stack must be individually accessed, which leads to word line scaling and stacking issues [9]. In addition, storing more than one bit per cell requires an exponentially growing number of program levels, making this strategy untenable in the long run [5, 7]. By dissociating the write/read (W/R) access device from a low cost, multi-bit storage location, higher bit densities become feasible.

We propose a memory concept that is based on electrodeposition [10-18] and -dissolution [19-21] of multilayered metal stacks. If an extremely precise control of the individual metal layer thickness can be achieved, these layered stacks can be used to encode information and achieve very high bit densities. As the resulting metal stacks are reminiscent of geological stone (*lithos*) strata, we coin the name: *Electrolithic memory*. Because electrodeposition and -dissolution is inherently slower than the electrical switching of a silicon transistor, it is important to realize that this memory concept is intended for application at the low-cost-per-bit end of the memory spectrum.

The primary focus of this paper is to describe the memory device and its operating principles (Section II), as well as to put forward the device's requirements (Section III). In support of the concept, we provide a preliminary experimental

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S. Fransen, K. Willems, H. Philipsen, D. Verreck, W. Van Roy, O. Y. F. Henry, A. Arreghini, G. Van den bosch, A. Furnémont, and M. Rosmeulen are with imec, Leuven, B-3001, Belgium (e-mail: Maarten.Rosmeulen@imec.be).

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demonstration of the elementary W/R principles on large (>1 mm^2) and micrometer-sized electrodes (Section IV). Lastly, calculations based on finite element simulations give an indication of the scalability of our experimental results towards the final concept (Section V).

II. Memory Concept

The conceptual device (Fig. 1a) consists of a liquid electrolyte in contact with a dense array of individually addressable *working electrodes* (WEs) and a single large *counter electrode* (CE). The electrolyte contains at least two metal ion types, denoted here as A^{n+} and B^{m+}, that can deposit onto (or dissolve from) the WEs as respectively metal A or B. The WEs are made out of an inert metal, such as Pt or Ru, and are found at the bottom of high-aspect-ratio wells patterned in an insulating material (see Fig. 1b). Whether A^{n+} or B^{m+} deposits onto (dissolves from) the WE depends on the WE vs. CE potential, which is controlled by a CMOS circuit access array (see Fig. 1c-e).

Information is encoded as thickness and composition modulations of metal stacks deposited onto the WE. For example, 1 nm of metal A can be used to encode a binary 0, while 2 nm thick layers encode a binary 1. Metal B layers with a thickness of 0.5 nm can be used to delimit subsequent layers of A. Wells with a depth of 1 µm would then be capable of storing up to 500 bits. This contrasts with the 60 bits stored in an equally deep triple-level 3D NAND memory string with a 50 nm Z pitch. Hence, the proposed device is theoretically able to reach very high bit densities (>1 Tbit/mm^2) for >3.3 µm deep wells arranged in a <40 nm pitch square array.

Writing and reading information is equivalent to the deposition and dissolution of modulated metal stacks. As the deposition (or dissolution) of metal ions corresponds to the reduction $A^{n+}(aq) + ne^- \rightarrow A(s)$ (or oxidation $A(s) \rightarrow A^{n+}(aq) + ne^-$), an electrical current proportional to the deposition (dissolution) rate flows through the WE. Therefore, each potential applied by the WE corresponds to a species-specific partial current. The current-potential (*I-V*) relationships for A^{n+} and B^{m+} then determine the procedure for writing and reading bits (Fig. 2a).

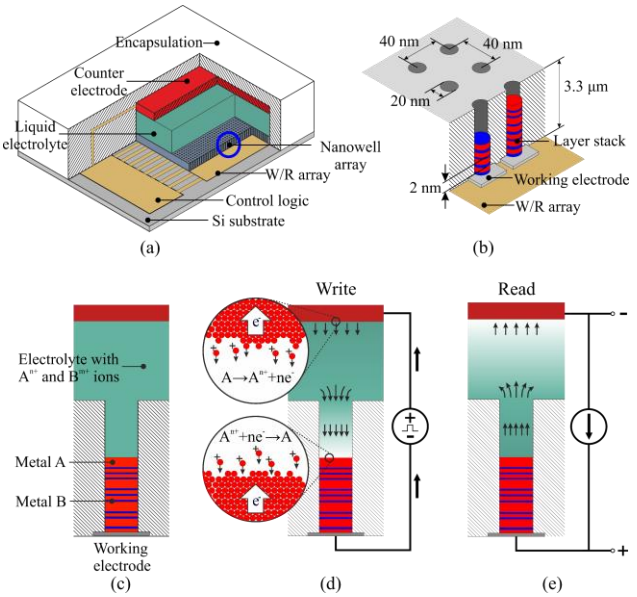

Fig. 1. The conceptual electrolithic memory device (a) as part of an integrated circuit where (b) an array of high aspect ratio nanowells stores a very large number of bits as (c) encoded by thickness modulations between metals A and B. The working electrode potential or current is controlled to selectively (d) deposit (write) or (e) dissolve (read) the metal stack.

Bits are written by polarizing the WE cathodically compared to the open-circuit potential (OCP). At a certain cathodic potential, A^{n+} will reduce and deposit onto the WE. In principle, the deposition rate increases exponentially for more cathodic potentials but stagnates once diffusion of A^{n+} towards the WE becomes the rate-limiting step. The metal ion B^{m+} behaves similarly, except that it has a different deposition onset potential (determined by its chemical nature) and diffusion-limited plateau (determined by its concentration). Thus, the desired stack is deposited by controlling the pulse amplitude and/or duration of the applied cell potential (see Fig. 2b). Note from the *I-V* characteristic that A layers are typically pure, as they

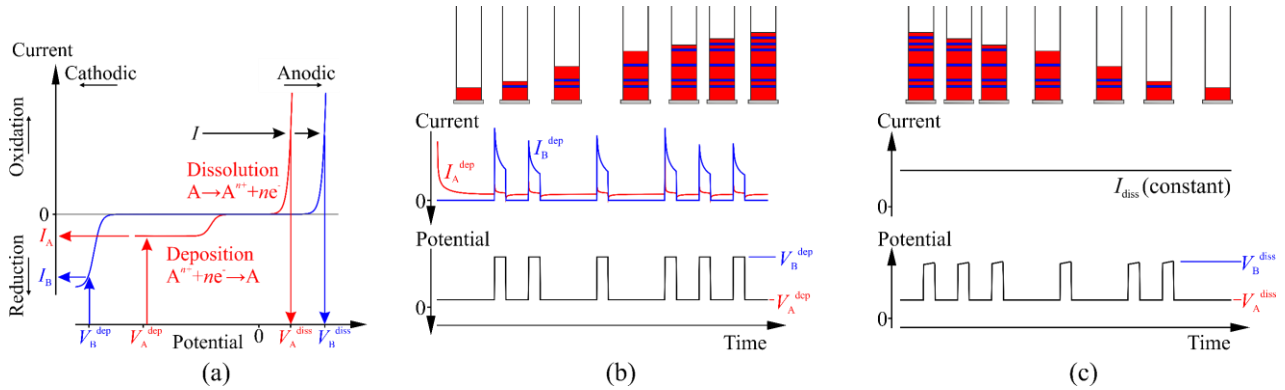

Fig. 2. Schematic of the operating principle with (a) the desired current-potential characteristics for metal A and B, (b) the write operation where layers A or B are deposited (deposition rates are respectively proportional to the partial currents I_A^{dep} and I_B^{dep}) by switching between the potential V_A^{dep} for metal A and V_B^{dep} for metal B, and (c) the read operation where the metal stack is dissolved by applying a fixed anodic current I_{diss}. During the dissolution process, the potential switches from V_A^{diss} to V_B^{diss} depending on the top layer's composition.

reduce below the deposition onset potential of B, whereas B layers tend to be alloyed with some amount of A.

The stored bits can be read by dissolving the metal layers at a fixed anodic current. As the dissolution rate increases exponentially for more anodic potentials and no diffusion limited regime occurs, mainly the dissolution onset potentials for metal A and B are relevant (Fig. 2a). Hence, by applying a constant anodic current, the stack will dissolve at a fixed rate and the corresponding dissolution potential is determined by the top metal layer's composition. As the dissolution of the metal stack progresses, the changing top layer composition of the modulated stack is detected through a changing dissolution potential (Fig. 2c). The deposited metal stack is, therefore, read destructively in a "last-in first-out" (LIFO) way.

The primary purpose of the CE is to close the electrical circuit and provide a concurrent oxidation (or reduction) reaction during deposition onto (or dissolution from) the WE. Preferably, the CE consists of an A–B alloy that dissolves when A or B is being deposited onto the WE (or vice versa). By matching the composition of this alloy with the expected (averaged) composition of the metal stacks, the electrolyte composition will remain unaffected: All the metal ions consumed at the WE are replenished by exactly the same number of ions dissolving from the CE and vice versa. For example, using 1 nm and 2 nm A layers with 0.5 nm B spacer layers, the counter electrode preferably consists of 75 at% A and 25 at% B. An inert metal, such as Pt or Ru, cannot be used as CE. The concurrent counter reaction would then be the oxygen (or hydrogen) evolution reaction, which introduces undesirable gas bubbles inside the closed electrolyte reservoir and changes the electrolyte's pH.

III. Device requirements

The primary advantage of electrolithic memory is its extremely high bit density (>1 Tbit/mm^2). However, in order to be viable, the technology must also have an acceptable response time, bandwidth, cycling endurance, and retention. Estimates for these device characteristics are provided here.

As electrolithic memory targets nearline workloads (i.e., large datasets that are less frequently accessed), achieving an acceptable bandwidth is prioritized over the response time. Based on projections for 3D NAND flash beyond 2030 [1], we aim for bandwidths of ~20 Gb/s for electrolithic memory. These high bandwidths are reached by addressing a large number of memory cells in parallel. Assuming a deposition/dissolution rate of 20 µm/s (see Section V) and ~2 nm/bit, each cell can be written or read at 100 µs/bit. On a per-bit basis, this is comparable to the write time and ten times slower than the read time of a NAND flash cell [1]. However, the bits in electrolithic memory are not randomly accessed but information is retrieved by full stack (~1650 bits) readout, which takes from 100 ms to 1 s. About 2 million cells need to be accessed simultaneously to reach a bandwidth of 20 Gb/s. For a more relaxed deposition/ dissolution rate of 2 µm/s (1 ms/bit), the number of cells addressed in parallel should be increased by tenfold. The destructive read also requires depositing a duplicate stack in another well. As this can be done simultaneously with readout, no impact on the device performance is expected.

The degree of parallelization is fundamentally limited by the energy needed for depositing/dissolving a single bit, which is equivalent to a certain thickness of the metal stack. Assuming typical transition metals are deposited in a Ø20 nm well with ~2 nm/bit on average, the charge to write or read a bit would be ~20 fC. This charge results in ~60 fJ/bit using a conservative ±3 V W/R potential. Although this is of the same order of magnitude as the ~10 fJ needed to write a bit in a 3D-NAND cell [22], an accurate comparison can only be made after specific aspects, such as the peripheral electrical circuitry, have been detailed. Nevertheless, the low power consumption for writing/reading bits raises no theoretical objections for achieving high bandwidths. For example, even for bandwidths of 100 Gb/s, the power consumption of the memory cells will at most be 6 mW. Moreover, as the peripheral circuit architecture likely will be comparable to contemporary 3D NAND flash, no inherently different challenges are expected with regards to parallelization.

An endurance of roughly 10^3 W/R cycles is required for typical data storage applications. Although challenging, cycling times of $>10^4$ have been reported for high-end electrolytic batteries [23] and supercapacitors [24], which operate on similar charge/discharge mechanisms. Typical degradation mechanisms would then include (i) incomplete dissolution of the stack due to partial passivation or metal oxide formation, (ii) plating bath stability, and (iii) cyclical degradation of plating bath additives that ensure a good deposit quality. For applications closer to cold data storage, however, the cycle endurance can be more relaxed.

Due to the very low mobility of atoms with respect to electrons, much longer retention times than 3D NAND can theoretically be achieved. Retention is most likely affected by corrosion of the deposited stacks. To prevent corrosion of the metal stacks by dissolved oxygen, it suffices to remove oxygen from the electrolyte prior to hermetically sealing the electrolyte reservoir, e.g., by sparging the electrolyte with N_2 or Ar, packaging in an N_2 blanketed environment, and using a packaging material with sufficiently low O_2 permeability. The temperature window will likely be limited by the electrolyte's boiling and freezing point, the solubility limits of the added salts, and packaging. In case non-aqueous solvents are used, such as ionic liquids or deep eutectic solvents, temperatures exceeding 100 °C might still be acceptable. The additional liquid electrolyte handling and encapsulation might add to the total cost of the chip. Given that the added cost is shared by many bits, it is assumed that this cost will remain low on a per-bit basis.

IV. Proof-of-Principle

From the description of the device's operating principles, it follows that a fundamental proof-of-principle requires (i) the formulation of an electrolyte with the desired *I-V* characteristics from which (ii) controlled A|B stacks can be deposited (corresponding to the write operation) and where (iii) the dissolution potential reveals the A|B stack composition (corresponding to the read operation).

An aqueous plating bath containing 0.05 M $CuSO_4$, 0.70 M $NiSO_4$, 0.11 M $CoSO_4$, 0.44 M citric acid, 1 M NaOH, and 0.24 mM $NaC_{12}H_{25}SO_4$ (sodium dodecyl sulfate) was used [18]. The

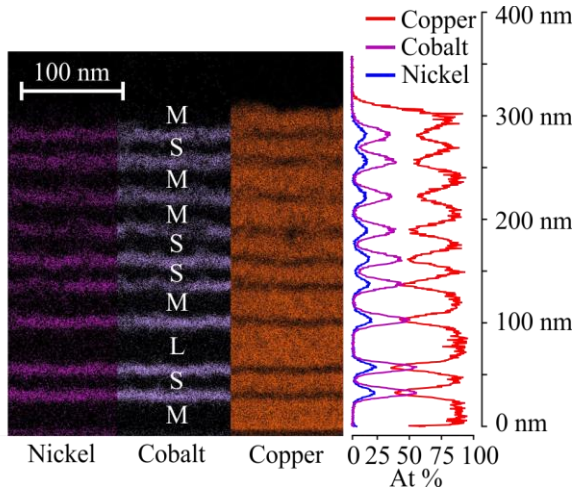

Fig. 3. STEM-EDS cross section of a Cu|Ni–Co stack deposited from a citrate plating bath. The Cu layers are deposited at -0.5 V (vs. Ag/AgCl) and their thickness is varied (deposition times: 25 s (S), 50 s (M), 75 s (L)). Ni–Co is deposited at -1.3 V (vs. Ag/AgCl) and is used as a spacer layer (deposition time 2.5 s).

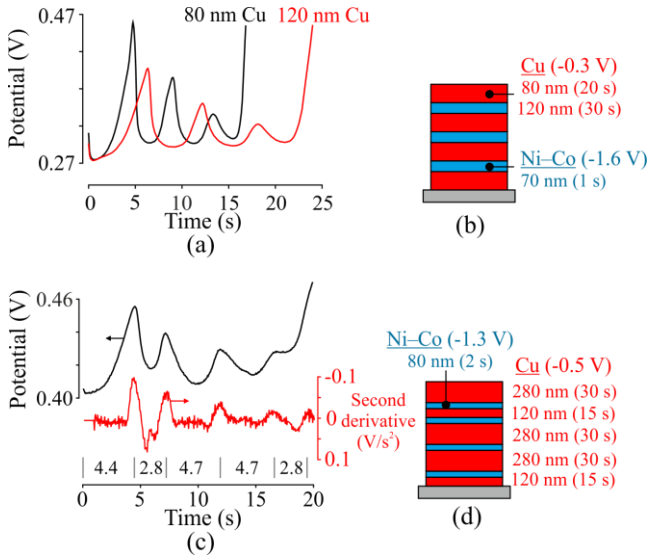

Fig. 4. Read signals for the electrodissolution of electrochemically deposited metal stacks on a rotating disk electrode (4000 rpm, 7.1 mm^2): (a) the dissolution potential at 70 mA/cm^2 for the stacks shown in (b) and (c) dissolution potential at 140 mA/cm^2 for the modulated stack shown in (d). Here, the dissolution potential's second derivative aids Ni–Co peak localization, but also illustrates the signal's degradation.

A and B layers are formed during the reduction of Cu^{2+} and Ni^{2+}+Co^{2+}, respectively yielding metallic Cu and a co-deposit of Ni–Co. Two macroscopic electrode setups were used to validate the concept: (i) Pt blanket samples (95 mm^2) and (ii) a Pt rotating disk electrode (Metrohm Autolab RDE, 7.1 mm^2, 4000 rpm). A Pt wire CE and a 3 M NaCl Ag/AgCl reference electrode (RE) were used. The pulsed deposition and fixed current dissolution were controlled by an Autolab PGSTAT128N (Metrohm) potentiostat.

To demonstrate the write operation, modulated Cu|Ni–Co stacks were deposited on Pt blankets from the proposed plating bath. Energy dispersive X-ray spectroscopy in scanning transmission electron microscopy (STEM-EDS) shows clear thickness variations down to 20 nm in Cu layers separated by

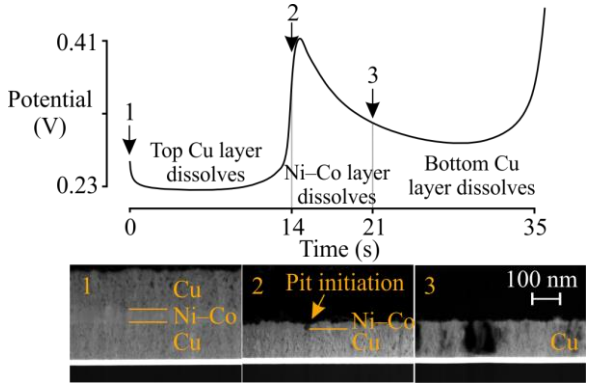

Fig. 5. (Top) Potential transient during the dissolution of a Cu|Ni–Co|Cu stack deposited on a Pt blanketed wafer (95 mm^2) at 10.5 mA/cm^2. (Bottom) Annular bright field scanning transmission electron microscopy (ABF-STEM) images at different stages of dissolution (as indicated in top figure): (1) as deposited stack, (2) top Cu layer is entirely dissolved, and (3) intermediate between the Ni–Co peak and full stack removal.

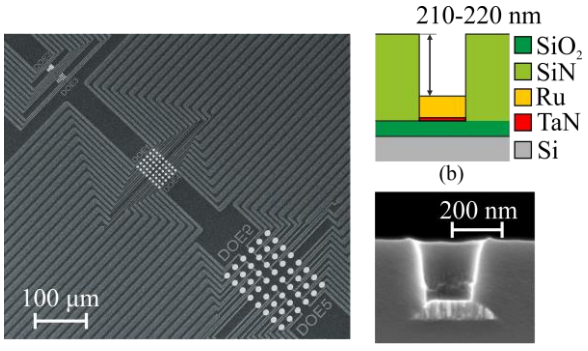

Fig. 6. Microelectrode arrays (diameters 10 µm, 4 µm, 1.5 µm, 700 nm, and 150 nm) for scaled experiments: (a) Top view SEM showing the 10 µm, 4 µm, and 1.5 µm electrodes, (b) schematic of the electrode's cross section, and (c) cross-sectional SEM of a 150 nm electrode.

Ni–Co spacer layers (Fig. 3). Due to the polycrystallinity of the deposit, the individual layers gradually roughen during stack deposition. Smoother deposits can be obtained by adding brightening and leveling agents to the electrolyte [25-27].

To demonstrate the read operation, Cu|Ni–Co layers with different Cu layer thicknesses were electrochemically deposited onto an RDE and subsequently dissolved (Fig. 4a-b). As Ni–Co layers dissolve at more anodic potentials compared to Cu layers, a peak in the dissolution potential is observed each time a Ni–Co layer dissolves. Due to the applied constant dissolution current, the duration in between the Ni–Co peaks provides information about the Cu layer thickness. Similarly, modulations within the same Cu|Ni–Co stack are also detected (Fig. 4c-d). At present, the read signal during stack dissolution becomes less pronounced for layers located at the bottom of the stack. This is attributed to: (i) the roughness of the deposit itself (Fig. 3), (ii) the non-uniform current distribution on a macroscopic electrode (especially near the RDE's edge, see Section V), and (iii) the formation of pits in the Ni–Co layers so that underlying Cu layers are prematurely exposed and preferentially attacked (Fig. 5).

To investigate how the W/R operation scales from large millimeter-sized electrodes to much smaller micrometer-sized electrodes, we also performed experiments on Ru

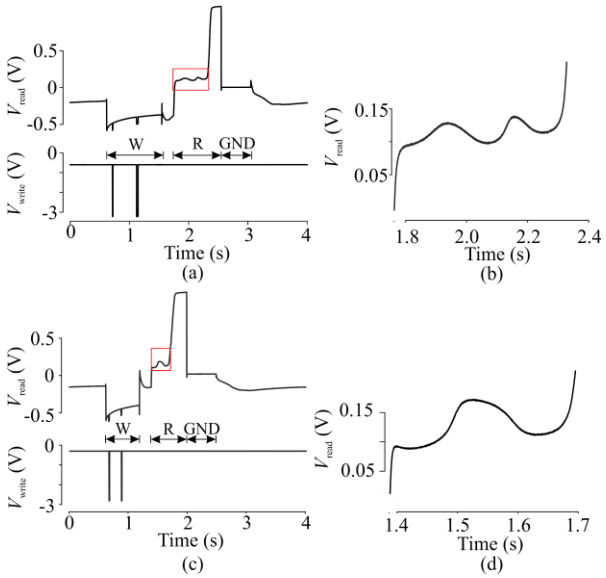

Fig. 7. Write/read cycles using ø4 µm electrodes. A Cu|Ni–Co|Cu|Ni–Co|Cu stack is written (W) by connecting the microelectrode to a Keysight 81110A Pulse Generator (V_{write}, note the two pulses for Ni–Co layer deposition). Otherwise, the microelectrode is connected to an Axon Axopatch 200B (V_{read}), which applies 9 nA for reading (R) the stack. After stack dissolution the WE and CE are short-circuited to ground (GND). The total deposition times are 0.95 s (a) and 0.57 s (c). A zoomed version of the dissolution potential transient for (a) and (c) are seen in (b) and (d), respectively. Note that for the 0.57 s deposition time in (c), only one Ni–Co peak is detected (d).

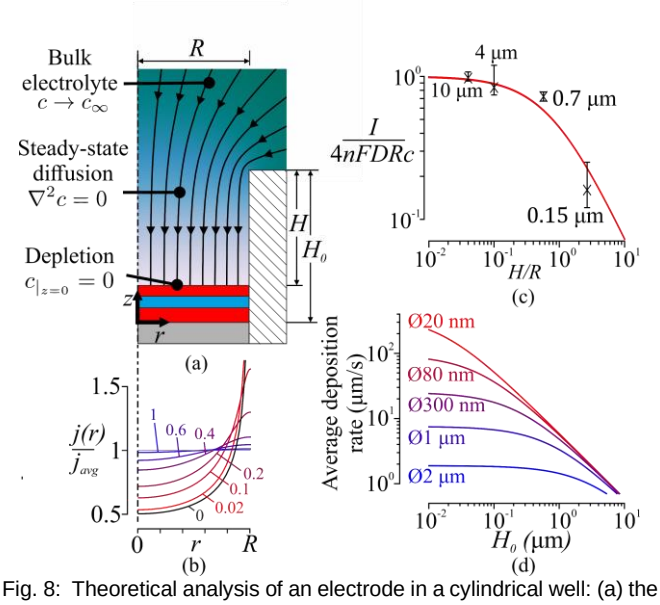

Fig. 8: Theoretical analysis of an electrode in a cylindrical well: (a) the geometry with the model equations and boundary conditions indicated, (b) the current density distribution $j(r)$ (proportional to the deposition/dissolution rate) normalized by the average current density j_{avg} for different aspect ratios H/R, (c) the theoretical (line) and experimental (average: ×, intervals: data range) diffusion limited current for the microelectrodes shown in Fig. 6 using 10 mM $K_3Fe(CN)_6/K_4Fe(CN)_6$ in 1 M KCl, and (d) the deposition rate averaged over time to fill a well for a Cu + Ni–Co plating bath with 500 mM Cu^{2+}, 2 M Ni^{2+}+Co^{2+} where Cu layer thicknesses are on average 1.5 nm and Ni–Co layers are 0.5 nm.

microelectrode arrays with diameters ranging from 150 nm to 10 µm (Fig. 6). Here a Cu plate was used as both CE and RE. Pulsed deposition was performed by a Keysight 81110A Pulse Pattern Generator and the fixed current dissolution by an Axon Axopatch 200B. An Axon Digidata 1550B controlled the electrode/instrument relays, triggered the instruments, and digitized their outputs.

W/R cycle times for Ø4 µm electrodes reduce significantly compared to the large electrodes (Fig. 7a-b). Notably, a 5-layer is deposited or dissolved within a second. This is much faster compared to the >1 mm^2 electrodes which require 50 s to 100 s for depositing a similar stack and 10 s to 20 s for dissolving it. In contrast to the large electrodes, the read signal modulation of the microelectrodes is weaker: the Ni–Co peaks are broad, and modulations are smaller than 50 mV, preventing further deposition time reductions or clear layer modulations (Fig. 7c-d). This is attributed to the deposit's roughness and the non-uniform current distribution on disks (see Section V). Additionally, a high parasitic capacitance due to the long electrical connections (on-chip, wire bonding, and PCB) and switching relays is suspected to degrade the read signal. For this reason, smaller electrodes cannot be evaluated using the current setup and carefully designed test structures or on-chip sensing circuits are needed to detect the signals of smaller cells.

V. Theoretical Scaling Calculations

Experiments showed a clear deposition/dissolution rate increase (shorter W/R times) for microelectrodes compared to millimeter-sized electrodes. In this section, we use theoretical calculations to estimate how the deposition rate and current distribution change for increasingly smaller electrodes in deeper wells. As both the deposition rate and dissolution rate are ultimately limited by the diffusion of metal ions towards or away from the metal stack's surface, we provide an estimate of the diffusion-limited deposition rate, which is typically the most time-consuming step.

To estimate how the deposition rate will scale for smaller and deeper electrodes, it suffices to solve the diffusion equation for the depositing metal. As the concentration profile quickly adapts to the growing layer, a quasi-steady state can be assumed (Fig. 8a). From literature [28-31] it is known that (i) electrodes with smaller diameters provide faster deposition rates, which was confirmed experimentally for our microelectrodes, and (ii) deeper wells have a more uniform current distribution, which we illustrated using finite element simulations (COMSOL Multiphysics, Fig. 8a-b). A useful approximation to these simulations for the instantaneous current I (max. 3 % relative error vs. simulations) of an electrode with radius R (m) in well with depth H (m) is given by [29]

$$I = \frac{4nFcDR}{1 + \frac{4}{\pi}\frac{H}{R}}, \tag{1}$$

with n the number of exchanged electrons, F Faraday's constant (96485 C/mol), c (mol/m^3) the bulk ion concentration, and D (m^2/s) its diffusion coefficient. We experimentally verified Eq. (1) for our microelectrode arrays using the hexacyanoferrate(II)/hexacyanoferrate(III) redox couple and measuring the current at ±0.5 V (WE vs. CE) with an Agilent 4156C Precision Semiconductor Parameter Analyzer (Fig. 8c).

From Eq. (1), a prediction of the instantaneous diffusion limited deposition rate v (m/s) of a metal with molar mass M_w (kg/mol) and density ρ (kg/m^3) follows

$$v = \frac{M_w c}{\rho} \frac{D}{H + \frac{\pi R}{4}}. \quad (2)$$

Note that as the well is filled, H gradually decreases. This results in an increased deposition rate v as the filling process progresses. In addition, the well is filled by at least two metals A and B with dissimilar electrolyte concentrations and physical properties. The overall deposition rate averaged over the time for filling the entire well with a stack with layer thicknesses h_A for A and h_B for B is then given by

$$v_{\text{avg}} = \frac{\frac{M_{w,A} c_A D_A}{\rho_A} + \frac{M_{w,B} c_B D_B}{\rho_B}}{1 + \frac{\rho_A}{M_{w,A} c_A D_A} \frac{M_{w,B} c_B D_B}{\rho_B} \frac{h_A}{h_A + h_B}} \frac{1}{\frac{\pi R}{4} + \frac{H}{2}}. \quad (3)$$

Using the Cu(A) + Ni–Co(B) system as an example ($\rho \approx 8900$ kg/m^3, $D \approx 0.7 \times 10^{-9}$ m^2/s, and $M_w \approx 0.06$ kg/mol) for the nanowells and encoding scheme given in Section II (R = 10 nm, h_A = 1.5 nm on average, and h_B = 0.5 nm) with an electrolyte containing 500 mM Cu^{2+} and 2 M Co^{2+}+Ni^{2+}, the average growth rate then results in about ~10 µm/s for a well with initial depth H < 700 nm (Fig. 8d). Although such a device would already reach a gross bit density of 220 Gbit/mm^2, electrolytes that allow for higher metal ion loadings must be explored to achieve ~10 µm/s for wells with H > 3.3 µm (1 Tbit/mm^2).

VI. Conclusion and Outlook

We presented a memory concept that encodes information as composition and thickness modulations in electrodeposited metal stacks. In support of the concept, we provided an experimental demonstration of the elementary write/read operation on large (>1 mm^2) and micrometer-sized electrodes. Notably, we experimentally showed that an average modulation length of 20 nm/bit can be written using a Cu/Ni–Co materials system and layers as thin as 80 nm can be read back. For a next step, we are preparing to test nanowells of 80 nm diameter, 1000 nm depth, and 160 nm pitch capable of storing 2 Gbit/mm^2. This device will also allow (i) a critical evaluation of cycling endurance, which was not yet demonstrated in this paper, (ii) further investigate the response time for much smaller electrodes, and (iii) evaluate the effect of temperature on the device characteristics (increased deposition rates, electrodeposition kinetics, plating bath stability). Ultimately, we anticipate that through further scaling efforts (smaller diameters, deeper wells, smaller pitch), continual plating bath improvements (smoother and thinner layers), and novel device architectures (write/read strategies, encoding schemes, parallelization, and support circuits), the information density can be pushed towards the 1 Tbit/mm^2 range.

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