A 67mW D-band FMCW I/Q Radar Receiver with an N-path Spillover Notch Filter in 28nm CMOS

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Abstract—A 139.5-157.7 GHz D-band I/Q radar receiver with an on-chip antenna and a spillover resilient N-path baseband filter is presented. Spillover and its manifestation based on the chirp duration is discussed and a filter for spillover mitigation is implemented. The radar is characterized with 18 GHz RF bandwidth, 13 mm range resolution, 55 dB conversion gain, 8 dB NF and 26 dB narrow-band spillover attenuation. The receiver is also capable of selectively mitigating close-by large reflectors and the system power consumption is 67 mW.

Index Terms—D-band radar, mm-wave LNA, I/Q receiver, Spillover attenuation, N-path filter, low-power receiver

I. INTRODUCTION

ALONG with conventional applications like ranging and detection, modern radars are evolving to handle more complex operations. Started as a tool for telemetry, spectroscopy and military reconnaissance [1], the radars made their way into the domestic and mobile applications as well. Among many architectures of radars, due to its sensitivity to the given power [2] and simplicity in the architecture, the frequency-modulated continuous-wave (FMCW) radars were preferred choice for the early research in the field of mercantile marine [3] and ionospheric echo detection [4]. Aligning with the improvements in the signal processing and memory technologies, exploiting the mm-wave frequency band (30-300 GHz) as a carrier frequency began in early 1980s [5] and the applications in the mm-wave band has been expanding ever since.

Moving to the higher carrier frequency is multi-fold beneficial to radars. For complex application spaces like high resolution 3-D imaging, and human-machine interactions like gesture sensing, a large radio-frequency (RF) bandwidth is necessary. As the f_{max} of the transistor crosses 300 GHz, realizing the radars in the frequency band around 150 GHz where a large bandwidth is available, is challenging but feasible. A large RF bandwidth yields better range resolution c/(2∗BW), where c is the speed of light and BW is the RF bandwidth. Hence, realizing the radars in the mm-wave frequency band, especially the D-band (110-170 GHz) where the fractional bandwidth of 15% or more is feasible, is advantageous in terms of range

resolution (R_{res}). Along with the increased range resolution, moving to high carrier frequencies offers a better displacement sensitivity expressed as phase rotation for unit displacement. The form factor of the on-chip passives and antennas shrink, as the frequency of operation increases, facilitating tightly packed and more compact arrays suitable for applications like 3-D imaging.

The recent state-of-the art mm-wave radars exploit the above mentioned advantages of the high frequency bands. Realized in different technologies such as CMOS, SiGe BiCMOS, the radars demonstrate highly integrated systems with on-chip antennas [6], designed for imaging, precision measurements including vital signs detection and gesture recognition [7]–[18]. However, the power dissipated in the front-end of the receivers of these radar systems, to improve the bandwidth and noise figure (NF) can be a bottleneck for low-power, highly integrated systems such as imaging arrays. As the dimension of the arrays increases, the power consumption of each unit of TX or RX becomes significant. Also, in a radar system the leakage from transmitter (TX) to the receiver (RX), termed as spillover, can cause compression or saturation in the RX signal path. In [6], [15] and [19] for example, a portion of the total power is spent to make the radar resilient to this spillover. Especially for the RX where the spillover is the limiting factor when the TX and RX are close to each other, the resilience to spillover becomes crucial.

This work addresses the problems mentioned above with an 18 GHz BW I/Q receiver in 28 nm bulk CMOS with 8 dB NF, 26 dB of narrow band spillover attenuation and consuming 67 mW. The designed receiver achieves 13% fractional bandwidth with its LNA and passive mixer-based front-end operating at 150 GHz using a low coupling factor (k_m), high-Q inter-stage transformer for impedance matching. A broadband, low power I/Q LO at 150 GHz is generated with an on-chip Branch Line Coupler (BLC). The spillover and its chirp duration dependency is studied in detail and a unique tunable solution in the form of N-path filter is implemented at baseband, enabling the receiver to selectively mitigate nearby targets and achieve a narrowband attenuation of 26 dB on the spillover. The selective and narrowband attenuation of the spillover/large reflector is unique to this work, and it enables the receiver to be resilient to chirp duration as fast as 6.6 μs.

In this article the radar receiver presented in [20] is elaborated in terms of 1) spillover manifestation discussion 2) Link budget analysis of the receiver 3) in-depth analysis and design considerations of the receiver blocks 4) new measurements and
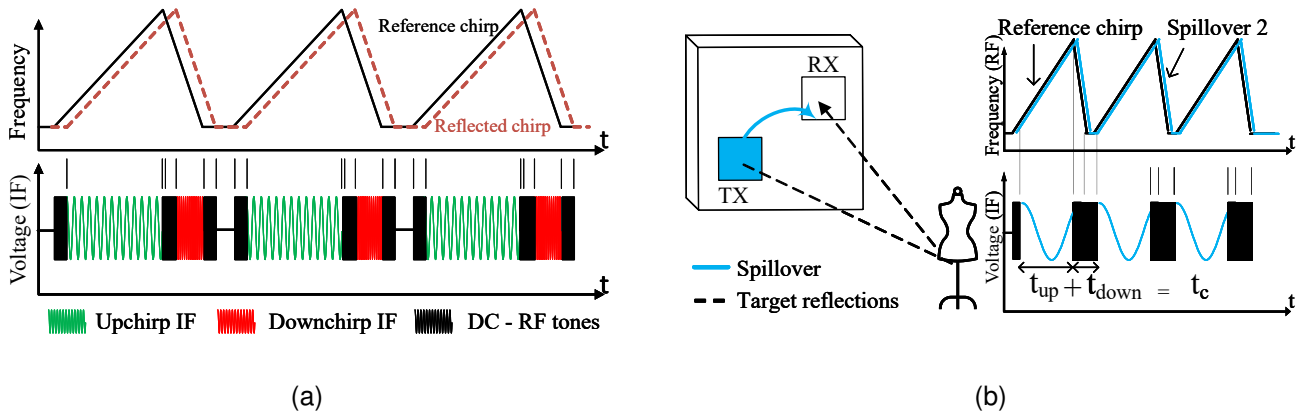
Fig. 1. Downconversion of correlated signals in a FMCW system (a) IF signals (b) Spillover.

demonstration of the range resolution of the radar 5) demonstration of the compatibility of the filter with the Doppler measurements. Section II details discussion on the spillover, its relationship with the chirp duration and predictability. Next in Section III, the link budget analysis of the receiver and the attenuation requirements at the baseband are discussed. Section IV describes the receiver architecture and a brief description of the blocks, followed by Section V where the front-end circuit design is detailed. Next, in Section VI the details of the baseband circuits are given. Measurements and the details of the setups verifying the functionality of the receiver and comparison with the state-of-the art are given in Section VII. The article is concluded in Section VIII.

II. SPILLOVER AND ITS CHIRP DURATION DEPENDENCY

In an FMCW radar system (see Fig.1a) the linear frequency modulated chirp is transmitted, and its reflections from objects are correlated with a reference chirp in the receiver to produce signals at a (relatively low) intermediate frequency (IF). The frequency of each IF tone is proportional to the time of flight between each target and the receiver, thus the distance from the target can be decoded. The IF is a composite signal consisting of all the tones unique to each target or reflector in the environment. Along with the targets, the signal also contains a tone which is a result of the direct coupling between the TX and the RX, which is termed as spillover (Fig.1b). As the spillover at the RF input and the reference chirp at the transmit side have a very low mutual delay, the spillover manifests as a large low-frequency tone after downconversion. The spillover can limit the performance of the radar by compressing or even saturating the receiver signal path. Or, upon downconversion, it can cause nonlinear distortion resulting in extra tones, corresponding then to ghost targets. Hence the receiver design should address this issue.

There are several methods to mitigate the spillover at RF, or at baseband through active or passive means in FMCW radars and non-FMCW schemes like PMCW and pulse radars. Passive spillover cancellation can be achieved with high linearity and minimum impact on the receiver performance when the TX and RX are together on-chip [21]–[24]. This scheme results in lossy and bulky on-chip components costing area

during the integration in bulk CMOS. On the other hand, active spillover cancellation has a low area footprint but it impacts the RX with noise and distortion [25]–[30]. In the receiver, the spillover can be mitigated right after the antenna [30] or after the LNA or at the baseband after downconversion [29], [15], [31]. When implemented at RF there is always a noise figure and power consumption penalty. At the LNA output, an analog feedback loop sensing and subtracting the spillover with a copy is used in [19] which achieves mitigation but, at the cost of close to 50 mW of power consumption in the front-end. The RF spillover cancellation is also employed in non-FMCW schemes like PMCW and pulse transceivers, that requires additional digital signal processing units leading to increased power consumption in the front-end and system level [14] and degradation of the conversion gain [32]. Spillover can also be addressed at the LO chain where a delay correlating to the spillover is introduced to push the frequency of the downconverted spillover to DC [15] this requires additional fine tuning of the LO and costs power and buffering at RF. But, when the spillover mitigation is done at the baseband, the NF of the RX is not affected and with suitable architecture of the FE and the baseband, this can be done without the excessive power consumption or linearity concerns.

The spillover level at RX can be mainly attributed to the free space path loss between the antennas. Also, at mm-wave frequencies, components in the vicinity of the path between the antennas affect the power received at the RX side. To accurately predict the spillover level at RX, one can rely on EM simulations. The frequency of the spillover however, is obviously a direct function of the distance between the TX and RX, but it must be noticed that also the chirp duration influences the evident frequency of the spillover upon downconversion. Now, let's consider the case with only spillover from TX to the RX, and observe the time domain waveform of the spillover like in Fig.1b. The spillover being a low-frequency signal gets interrupted, and will reset once with every chirp of duration t_c. Thus, the chirp duration which is the sum of chirp rise time t_{up} and reset time t_{down} influences the frequency of the spillover. During the time t_{up}, the wanted IF frequencies are present. The signals at the IF output during t_{down} are skipped in this analysis.
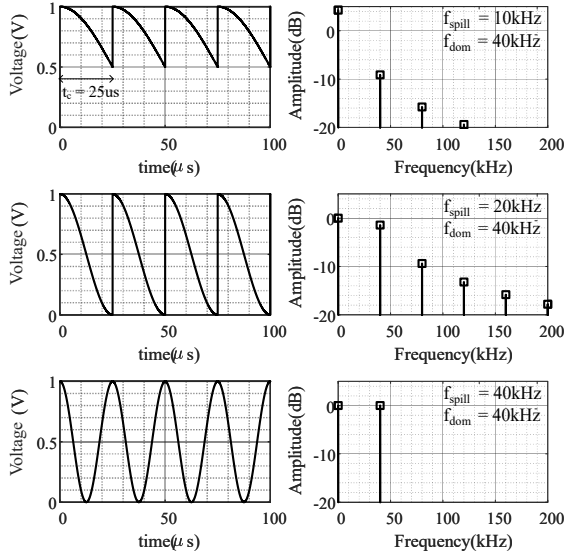
Fig. 2. Spectrum of the spillover with chirp windowing.

Fig. 3. Spectrum of the spillover with finite t_{down}

This interaction can be seen as a multiplication of a chirp function $f_c(t)$ and a sinusoid x(t) at the output of the mixer as shown below and repeats with each chirp. Within the single chirp the output can be defined as:
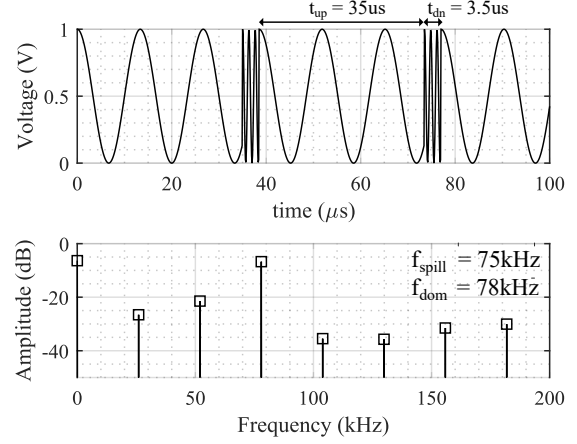
$$y(t) = x(t) \cdot f_c(t) \qquad (1)$$

where,

$$f_c(t) = \begin{cases} 1, & \text{if } 0 < t < t_{up} \\ 0, & \text{if } t_{up} < t < t_c \end{cases}, x(t) = A\cos(\omega t + \phi_0) \qquad (2)$$

Further, ω is determined by the TX-to-RX distance. Next we consider an example scenario where the t_c is taken as 25 μs with t_{up} = 25 μs and t_{down} = 0. The simulated baseband output signals for different delays of TX-to-RX coupling resulting in different spillover frequencies are considered. These spillovers are then subjected to the chirp function as described in (2) with the before mentioned timings and the spectrum is observed as shown in Fig.2. For the first case (top) a spillover of 10 kHz is let in the system and the wave is reset before it completes a cycle, hence it doesn't appear in the spectrum as 10 kHz but its power is distributed among the harmonics of frequency f_c which is $1/t_c$ i.e., 40 kHz. Similarly in the second case (middle), where the spillover of 20 kHz is let in the system and again since the spillover doesn't complete a sinusoid, its power is once again distributed in the harmonics of f_c. But in the third case when the spillover is taken as 40 kHz and it completes a sinusoid, the spectrum of the signal no longer contains harmonics but a single tone at f_c = 40 kHz. Among these cases, one can observe the dominant tone (f_{dom}) is always at 40 kHz which corresponds to $f_c = 1/t_c = 1/25$ μs.

With the above experiment, the following conclusions can be drawn:

a) for $f_{spill} < f_c$: The sinusoid is not complete and the spillover power is distributed among the harmonics of the f_c and dominant tone is at f_c.

b) for $f_{spill} = n*f_c$: The sinusoid is complete and the spillover is found as one tone at f_c.

c) for $f_{spill} > f_c$: The spillover completes a sinusoid but still due to the windowing, the spillover starts to appear at the next higher harmonic of the f_c. Whichever harmonic of f_c is closer to the spillover frequency will have the dominant tone. For example in the case when spillover is at 50 kHz, the dominant tone will still be at 40 kHz but power of the next harmonic i.e., 80 kHz increases. When the spillover is for example at 70 kHz, the dominant tone is at 80 kHz and the power at 40 kHz is reduced.

For the above examples we considered a zero t_{down} to simplify the explanation of the concept. But, in a practical system there will be a finite t_{down}. In such a case also, the spillover manifestation explained before holds good. For example, lets take a system with finite t_{down} of 3.5 μs and t_{up} of 35 μs. The total chirp time t_c, in this case will be 38.5 μs thus, the expected spillover components will be in the multiples of $1/t_c$ i.e., 26 kHz as shown in Fig.3. Here a spillover of 75 kHz is passed into the system and spillover during the up chirp time and down chirp time can be observed in the time domain waveform. The since the up chirp spillover frequency is higher than $1/t_c$, the spillover is shifted to the higher harmonic (3_{rd}) of $1/t_c$ which is 78 kHz. The spectrum shows the behavior of the spillover similar to the previous example with zero t_{down}, maintaining the predictability of the spillover frequency even with the finite t_{down}.

As the spillover is a very low frequency signal, its frequency can be approximated as f_c. With shorter and faster chirps, this approximation is even more valid. Hence, we can predict the position of the spillover based on the f_c and a narrow band filtering solution can be employed for attenuating the dominant tone. This windowing phenomenon was also observed in the unprocessed baseband outputs through the spectrum analyser for the 60 GHz radar described in [31].

It is important to note that the behavior of the other high

TABLE I
LINK BUDGET KEY SPECIFICATION ASSUMPTIONS

No	Specification	Value	Units
1	Center Frequency	145	GHz
2	RF bandwidth	20	GHz
3	Range (max)	8	m
4	Range (min)	0.5	m
5	Spillover coupling	-35	dB
6	Transmitter power	8	dBm
7	Noise Figure	8	dB
8	IP1dB (FE)	-25	dBm
9	OP1dB (BB)	-4	dBm
10	Processing Gain	55	dB
11	SNDR threshold	18	dB

Fig. 4. SNDR as a function of spillover attenuation and the reflector RCS.

frequency IF tones unique to each target is similar to the case c) discussed above and any nearby large reflectors in front of radars will always be in one of the harmonics of the f_c upon downconversion. This effect also holds good for the case where there are multiple spillovers coming from different transmitters. Though the delay of the these spillovers in comparison with the reference chirp is different, if the down-converted spillover tones are less than f_c, then they will end up in the same harmonic bin. Thus, any solution applied to the mitigation of the spillover can also be used to get rid of the nearby targets and the spillovers from the multiple transmitters.

On top of the windowing effect, as mentioned in the beginning of this section, the spillover frequency is directly proportional to the distance between TX and RX and the slope of the chirp (MHz/μs). Depending upon the application scenario, it is common to change the chirp rate and duration in a multi-purpose radar. This directly changes the f_c thus the spillover position. For the faster chirp duration f_c can be as high as 0.5 MHz. A tunable high-pass/narrow-band filter is thus required, to avoid compression of the baseband.

From the above experiments and the configuration conditions of the radar, we need a narrow band attenuation which should be constant and tunable over the frequencies. An N-path filter at the baseband can provide a low-power, tunable solution as the frequency of operation is in lower kHz range. In this work, such an N-path filter is implemented to build a resilient MIMO compatible receiver element.

III. LINK BUDGET

In the previous section, the manifestation of the spillover in relationship with the chirp duration is discussed. With that system knowledge, the link budget analysis of the receiver is presented.

For a long range radar, the atmospheric scattering determines the maximum detectable range for a fixed SNDR threshold. In our case, the radar is designed for two purposes namely imaging and people detection thus the required range is less than 10 m at which the atmospheric scattering is negligible.

The link budget analysis for this receiver is split into two parts: 1) For the first part, the spillover attenuation is kept sufficiently high and a nearby large reflector's radar cross section (RCS) is assumed sufficiently less to prevent the distortions from these two sources from affecting the SNDR
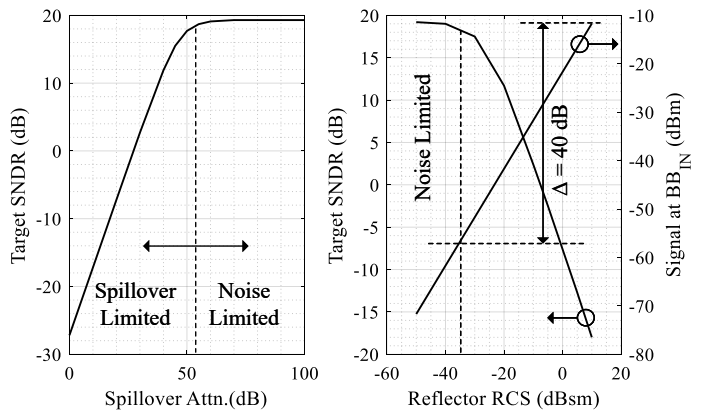
of the target which has very small RCS. With other distortions removed, the limitation on the SNDR due to the noise alone becomes evident. 2) Next, The degradation of the target SNDR is viewed as a function of the spillover attenuation and, as a function of the RCS of the nearby reflector which indicates the necessary spillover/nearby target attenuation required in the receiver. Next, the required attenuation is compared against the attenuation offered by the conventional 2nd HPF to assess the need of additional attenuation in the system.

For the first part the system assumptions made for the key receiver specifications are summarized in Table I. As described in Sec.I, 15% fractional bandwidth at 145 GHz is feasible thus a 20 GHz bandwidth is assumed and the resulting R_{res} is 8mm which is desired for the imaging application. For the given operating range of 8 m and 0.5 m with assumed chirp duration starting from 50 μs, the target IF at the baseband spans from 1.4 MHz to 22 MHz. It should be noted that the chirp duration determines the IF range of the system including the spillover frequency as discussed in the previous section. For a separation of 1 cm between TX and RX antennas, over the air coupling of -35 dB is calculated and considered. Thus, for a given 8 dBm of transmitter power, the spillover appearing at the LNA input is -27 dBm. This sets the compression point for the receiver. The processing gain including the range and Doppler processing is assumed to be 55 dB and the SNDR threshold is 18 dB. For the further information on calculating the link budget parameters, readers can refer [35]. With these initial specs the radar can detect the set of objects for both scenarios as summarized in Table II.

In the presented cases, the smallest object detectable by the radar will be at 8 m with the RCS of -20 dBsm. The case2 indicates the large object that can be imaged by the radar at 0.5 m with 12 dBsm RCS. The input power corresponding to the largest in-band object is -50 dBm which is the required in-band IP1dB of the receiver.

TABLE II
RCS, DISTANCE AND P_{IN} OF TARGETED CASES.

Specification	Case1	Case2
RCS (dBsm)	-20	12
Distance (m)	8	0.5
Power at the RX input (dBm)	-130	-50
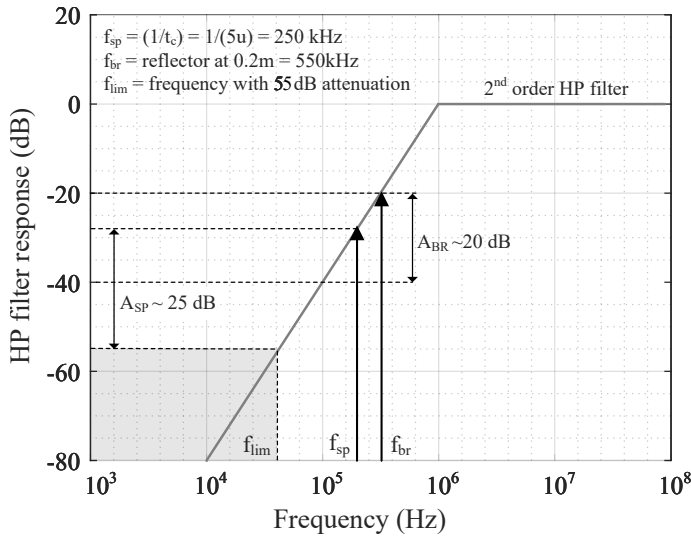
Fig. 5. Attenuation comparison with a 2nd order HPF

Fig. 6. Receiver architecture and the IC micrograph.

Next as a second part of the link budget analysis, the target SNDR degradation as a function of spillover attenuation and the nearby big reflector RCS is considered. For this analysis the target corresponding to case1 of Table II at 8 m and RCS of -20 dBsm is considered. The variation of the target SNDR is shown in Fig.4. In the left plot, the target SNDR variation with spillover attenuation in the baseband is shown. Until the 55 dB spillover attenuation, the improvement in the SNDR is seen, after that the SNDR stagnates at 19 dB and is noise limited. Any improvement on the spillover attenuation beyond 55 dB will not improve the SNDR. This sets a requirement of 55 dB of spillover attenuation in the system at the baseband. On the right plot, the spillover attenuation is kept at -70 dB (now the SNDR is not limited by the spillover attenuation) and a nearby large reflector at 0.2 m from the receiver is introduced and the RCS of the same is increased. From the plot, we can observe that the reflector RCS below -35 dBsm will not improve the target SNDR, as it is noise limited. As the target RCS increases the required attenuation on the reflector power (right axis) at the baseband (assuming 25 dB of front-end gain), also increases to bring the SNDR back to 18 dB. To tolerate a big reflector at 0.2 m with 10 dBsm RCS, we need at least 40 dB attenuation. The power corresponding to this big reflector at the LNA input in -35 dBm which is 10 dB less than the previously required input compression of -25 dBm, and the corresponding baseband frequency is 570 kHz.

In a radar receiver, a common approach is to place a high pass filter right after the mixer to filter out the spillover. Assuming such a scenario, with a 2nd order HPF with cut-off at 1 MHz, the available and required attenuation are compared next. As shown in Fig. 5, a 2nd order HPF at 1 MHz offers attenuation greater than -55 dB below the frequency f_{lim} which corresponds to 60 kHz. Any frequency of spillover that is above f_{lim} needs additional attenuation to reach -55 dB. For the fast chirp duration like 5 μs, the corresponding spillover frequency f_{sp} is 250 kHz and sufficient attenuation is not available from the HPF alone. Hence, for a 250 kHz spillover, an additional 25 dB attenuation is required. Similarly, the
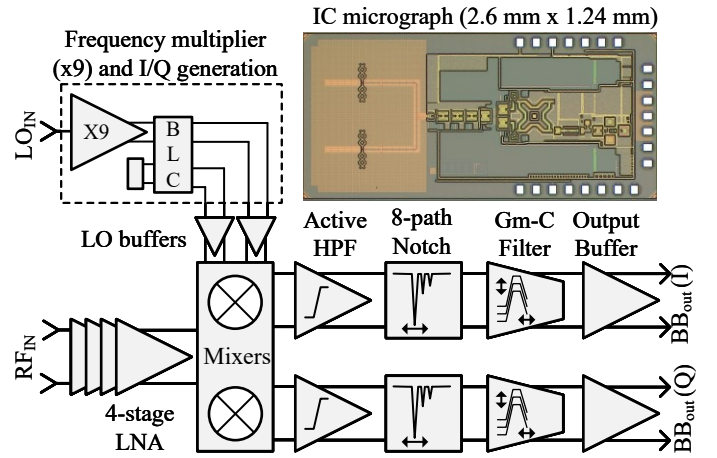
big reflector at 0.2 m (f_{br}= 550 kHz) experiences around 20 dB attenuation from the HPF, to reach the required 40 dB attenuation an additional 20 dB attenuation is required. Thus, the receiver must have 25 dB attenuation which should be programmable and an N-path filter (N=8) can provide the required programmable filter frequency and the attenuation.

It has to be noted that the HPF cut-off frequency considered is 1 MHz which is already quite high. For the scenarios which demand lower cut-off frequency like gesture recognition, due to insufficient attenuation from the HPF, the required attenuation to meet the SNDR threshold increases even more.

IV. RECEIVER ARCHITECTURE

The receiver as shown in Fig.6 is designed in a 28 nm bulk CMOS process and occupies an area of 2.6 mm X 1.24 mm. The front-end of the receiver has an on-chip antenna followed by a four-stage LNA optimized for gain, noise and broadband performance around 150 GHz. The LNA is followed by I/Q passive voltage sampling mixers to enhance the linearity of the front-end and provide a low-power I/Q downconversion. In comparison to the real-only baseband, the I/Q baseband receiver offers added benefits. The direction of the target movement can be discerned using an I/Q receiver. In addition to that, there is a benefit of improved noise figure up to 3 dB, improved interference tolerance and nearby object detection when I and Q channels are processed together [33], [34]. The mixers are fed by LO buffers preceded with a branch line coupler (BLC). This generates a broadband I/Q signal on-chip from the 150 GHz LO signal provided by 9-fold frequency multiplier (x9). The baseband at the output of the mixer consists of an active high-pass filter (HPF) which gives the first stage of attenuation for the spillover. The next stage is an 8-path notch filter providing a tunable narrow-band attenuation for the spillover while the rest of the high frequency IF remains unaffected. The variable gain and low-pass filtering (LPF) for the receiver is provided by the Gm-C filter in the next stage and the output buffer couples to the off-chip signal processing chain.
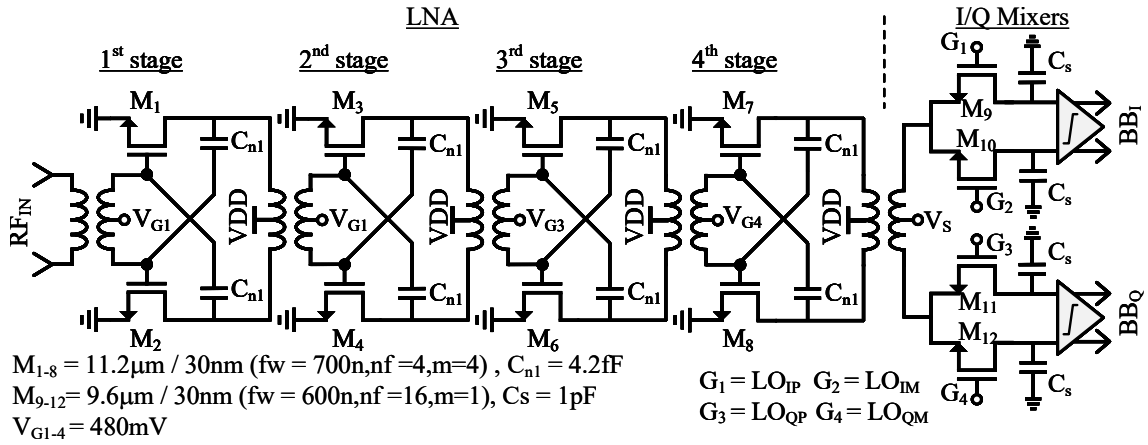
Fig. 7. Circuit diagram of the LNA and the I/Q mixer with device and component dimensions.

V. THE FRONT-END

As the f_{max} of the transistors in 28 nm is around 300 GHz, working at half of that at 150 GHz is challenging but still feasible. However, the other limitation to achieve a high gain and a high bandwidth simultaneously are the inter-stage matching and losses associated with it. In this section, the front-end circuits of this receiver and the generation of a broadband I/Q LO signal are discussed.

A. Low Noise Amplifier (LNA) and the mixers

At the input of the LNA is an on-chip sub-arrayed dipole antenna utilizing the substrate wave cancellation technique described in [36]. Without this cancellation, the losses due to the substrate waves heavily reduce the efficiency of the integrated antennas. To achieve this cancellation, the substrate thickness of the IC is customized and milled down to a 100 μm thickness. The resulting antenna efficiency is 62% in comparison with the 52% of a single dipole antenna. Further details on the on-chip antenna are given in [35].

The LNA that follows the on-chip antenna has four differential common-source stages with capacitive neutralization. The inter-stage matching is realized with transformers as shown in Fig.7. The gain degradation of the amplifier due to the gate-drain capacitance C_{gd} is compensated by neutralization capacitors C_n. The increase in the C_n beyond neutralization increases the gain but at the risk of decreased the stability of the amplifier core. With the choice of 4.2 fF of C_n, the available gain is close to 8 dB with a minimum value for the stability factor k_f of 1.2. The core transistors in each stage consist of 4 parallel connections of 4-finger units with a 700 nm fingerwidth. The consumption per arm is 3.25 mA, yielding a current density of 290 $\mu A/\mu m$ and the f_{max} of the transistor post layout is 280 GHz.

The input of the LNA is matched to the on-chip antenna with a tightly coupled 1:2 turn transformer. Since the high coupling factor of this transformer yields one peak in the transfer function in the frequency band of interest, it is placed at 145 GHz to simultaneously realize a conjugate impedance match and noise matching. To obtain broadband performance, the inter-stage matching networks use low-k_m high-Q inverting transformers. The low k_m high-Q transformers offer broad

bandwidth while incurring a comparable insertion loss to conventional tightly coupled high k_m transformers as the quality factor of the inductors is higher than 15 at mm-wave frequencies. The design of the inter-stage matching networks start with the simple equations yielding the preliminary values of the coupling factor, inductance of the primary and secondary turns of the transformers as described in [37].

$$|k_m| = \frac{\omega_H^2 - \omega_L^2}{\omega_H^2 + \omega_L^2} \tag{3}$$

$$L_p = \frac{1}{\omega_L^2 C_p (1 + |k_m|)\sqrt{\xi}} \tag{4}$$

$$L_s = \frac{\sqrt{\xi}}{\omega_L^2 C_s (1 + |k_m|)} \tag{5}$$

where, k_m = coupling factor, ω_H, ω_L = higher and lower complex pole frequencies of the transformer, L_p, L_s = inductance of the primary and secondary coil, ξ = pre-emphasis parameter to adjust the amplitude of the poles in the transfer function [37], C_p, C_s = equivalent parallel capacitance on the primary and secondary side.

The load at the drain of the first stage and the gate of the next stage of the LNA is modelled as primary and secondary parallel RC and the values are substituted in the design equations with the desired bandwidth. The value of k_m, L_p and L_s thus obtained can be used to design the inverting or non-inverting type transformer to do the matching. For better broadband response [37] the non-inverting transformers are used in this work. The design is started for the 30 GHz of bandwidth and the values obtained by the equations above are then further optimized with the design. As the design equations do not consider the coupling from the other transformers in the chain, detailed EM simulations are used to capture this. The coupling between the stages can lead to the distortions in the overall transfer function and can cause stability issues. To minimize the inter-stage coupling, the turns of the transformers in each stage are surrounded by a ground tub consisting of lower metal layers till the top metal to isolate the turns as shown in Fig.8. The transformer chain including the input transformer and the LNA mixer interface is 450 μm long and is extracted together. The input transformer has a quality factor of

TRF$_{INP}$ Lp = 45pH , Ls = 101pH, |k$_m$|= 0.6
TRF$_{INT}$ Lp = 98pH , Ls = 102pH, |k$_m$|= - 0.18
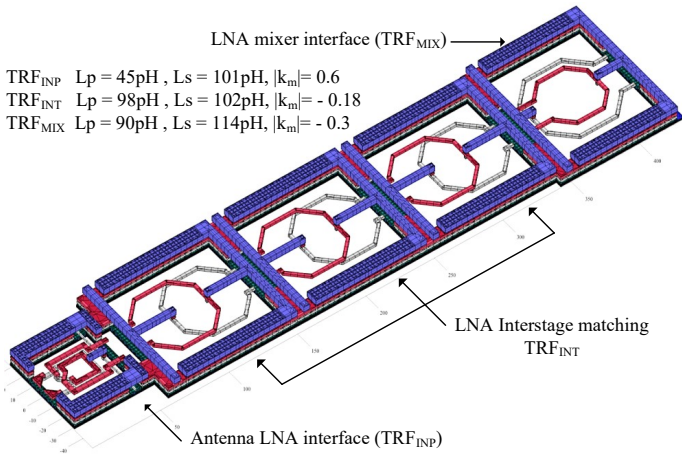TRF$_{MIX}$ Lp = 90pH , Ls = 114pH, |k$_m$|= - 0.3

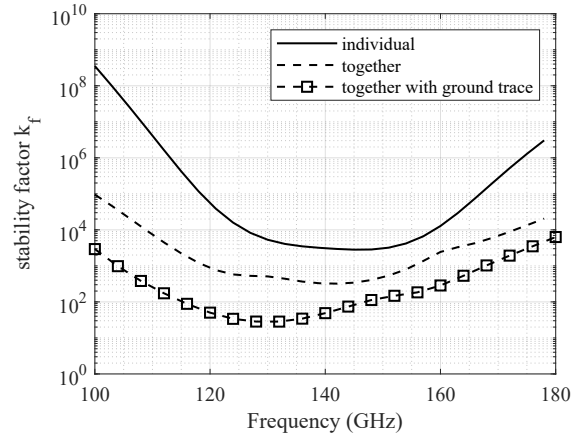Fig. 8. LNA transformers with the component values.

Fig. 10. Stability factor k$_f$ variation with the extraction.

15, whereas the inter-stage transformers have a quality factor of 18.

The simulated available gain G$_A$ of the LNA is 18 dB with 27 GHz of bandwidth (Fig.9). The input matching (S11) is optimized for 145 GHz and degrades as we move to the edge of the band. The LNA achieves a simulated noise figure of 8 dB (SSB) and the stability factor of the amplifier is around 27 minimum. The stability factor of the amplifier degrades as we move from individual transformer extraction to the collective transformer extractions as shown in Fig.10. As the over-the-air coupling and substrate coupling increases the interaction among the transformers, this reduces the reverse isolation and can cause stability issues. In the three stages, starting from the case where the passives are extracted individually, the k$_f$ is close to 2.8e3 but with increased integration with other transformers and with the ground trace (connecting the individual ground rings of the transformers to the main ground line), it reduces to 27. Even with the reduction of the stability factor, the amplifier is unconditionally stable but, it is crucial to pay attention to this degradation and consider it in the design. The results presented for the LNA in Fig.9 are from case where all the passives and the ground trace are extracted together. The LNA in total consumes 22.5 mW of power and exhibits a -16 dBm IP1dB.

The LNA is interfaced to the mixer with a similar transformer as inter-stage matching circuit. This interface transformer gives an additional voltage gain as well as DC isolation from the LNA to the mixer. With 18 dB of LNA gain, the impact of the mixer noise is less than 1 dB on the overall NF of the front-end. However, the linearity of the mixers is still crucial. As a low-power and linear solution, a passive voltage sampling mixers is chosen. The mixer consists of four transistors as shown in Fig.7 and Fig.11. The two ends of the secondary of the LNA-mixer interface transformer are connected to either the I or the Q channel. That avoids a crossover connection and minimizes the coupling between the I and Q channels. Upon downconversion, the sampled voltages are held on 1 pF grounded capacitors (C_S) which are connected to the first stage of the baseband. The mixer sources are biased at 600 mV and the gates are at 750 mV. The simulated conversion gain of the LNA and mixer with the EM extracted passives and the LO chain is shown in Fig.12. The noise figure degradation is less than 0.5 dB and the 3-dB bandwidth of the front-end is 20 GHz.
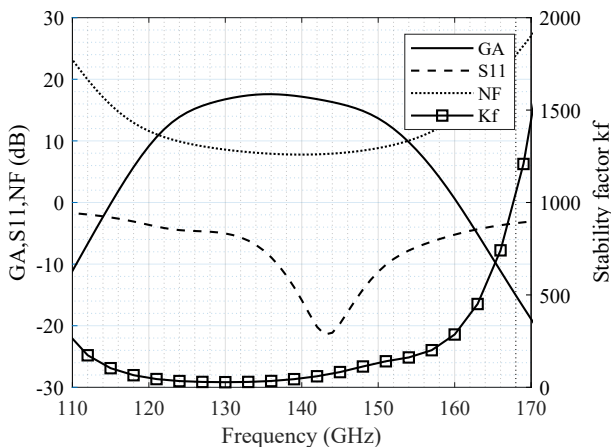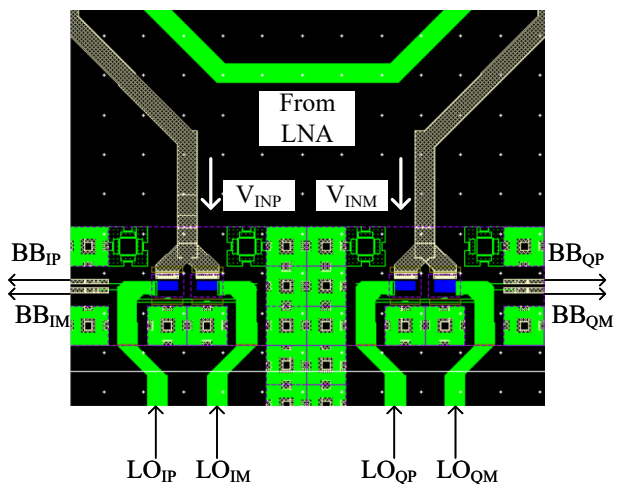

Fig. 9. Simulated performance of the LNA.

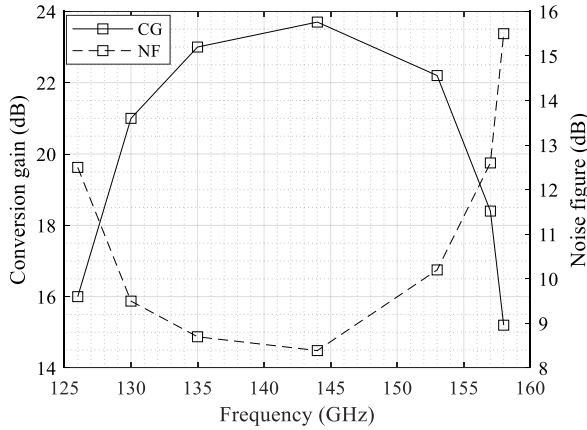Fig. 11. Input and the I/Q LO signals routing to the mixer.

Fig. 12. Simulated conversion gain and the Noise Figure of the front-end.

B. LO chain and the I/Q generation

To provide the necessary swing to the I/Q mixers to down-convert the signals, the LO chain in this work uses a multiply by 9 chain (x9) comprising of two cascaded frequency triplers followed by a gain boosted amplifier stage. Following the amplifier is the on-chip Branch Line Coupler (BLC) which is employed as a passive low-power solution to generate the broadband I/Q signals to the mixer. The branch line coupler is interfaced to the LO buffers which have same dimensions as single LNA stage and the output of the buffer is coupled to the mixer gates using the before mentioned low-k_m high-Q transformers to obtain the maximum swing.

The frequency band centered around 16 GHz is multiplied by 9 to reach the 144 GHz band. The frequency multiplier chain consists of phase-controlled frequency triplers at D-band and V-band exploiting phase aligned harmonic generation for high efficiency, conversion gain and output power which eliminates the need of the extra buffering stages thus providing the low power solution. The amplifier at the output of the x9 chain uses a wide-band maximum achievable gain (G_{max}) core to mitigate the gain limitation of D-band amplifiers. The triplers and the amplifier following them is re-used from the [38] and in-depth technical details can be found there.

As we move to the D-band, the $\lambda/4$ of the wavelength approaches close to 250 μm. These lengths are realizable on-chip, thus a passive and wide-band coupler can be used in this design. Among the different architectures of the couplers,

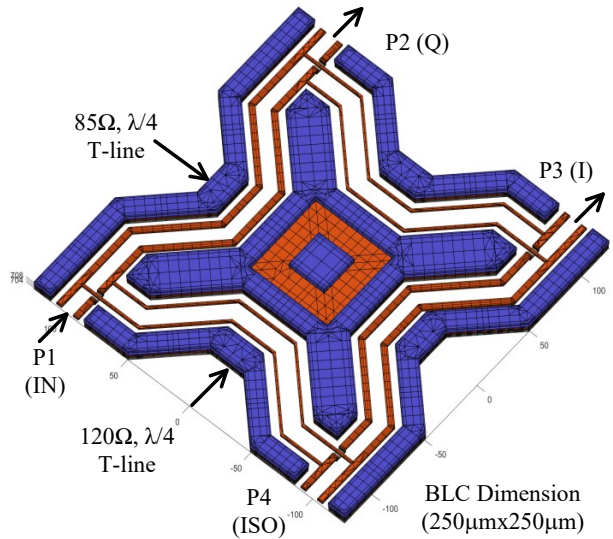Fig. 13. Top schematic of the LO chain with x9.

Fig. 14. EM extracted view of the BLC.

the BLC offers a good trade-off between the area and the performance [39] at mm-wave frequencies. The structure of such a coupler as shown in the left inlet of the Fig.13 consists of four differential arms. The top arm which connects the input port P1 to the output port P2 gives the quadrature signal Q at the output and is a $Z_0/\sqrt{2}$, $\lambda/4$ differential transmission line. The in-phase port P3 is connected to P2 with a similar differential transmission line but with characteristic impedance of Z_0. An isolation resistor of value Z_0 is connected to P4 which is connected to the P1 and P3 by transmission lines of characteristic impedance Z_0 and $Z_0/\sqrt{2}$ respectively. Z_0 is chosen to be 120 Ω since it is the highest realizable characteristic impedance in this technology at mm-wave frequency and facilitates the easier match to the input of the LO buffer.

Since the BLC by design requires long (250 μm+) transmission lines, maintaining the symmetry in all four arms of the coupler is crucial. The symmetric layout as shown in Fig.14 is designed and the EM extracted with the ground shields. The area in the middle of the coupler is covered with the grounded metals thus isolating the arms from each other. The crossing of the metals at the interconnections is also maintained symmetric by construction and extracted results of the BLC is as shown in Fig.15. The coupler gives an additional 1dB insertion loss on top of the 3 dB loss due to power division (Fig.15a) and the S21 and S31 are aligned at around 145 GHz. The amplitude and phase difference plot (Fig.15b) shows a 1dB amplitude difference over the bandwidth ranging from 120-170 GHz. The phase difference of $\pm 5^0$ is obtained from 130-160 GHz thus providing an image rejection ratio of >25 dB with 30 GHz of bandwidth.

The output of the BLC is matched with the input of the LO buffer via shunted inductor and transmission lines (Z_0=85 Ω). The LO buffer is then matched to the passive mixer gates which require a minimum of 600 mV swing. Fig.16 shows the simulated the output swing for the different signal powers at the input of the BLC. For input powers greater than -3 dB the BLC sufficiently provides the required swing thus enabling the broadband I/Q LO. Next the full front-end with LO with the
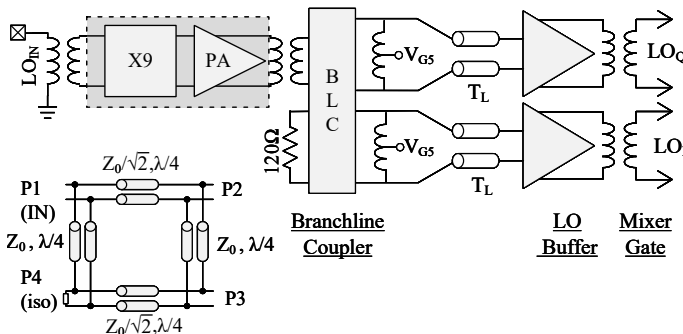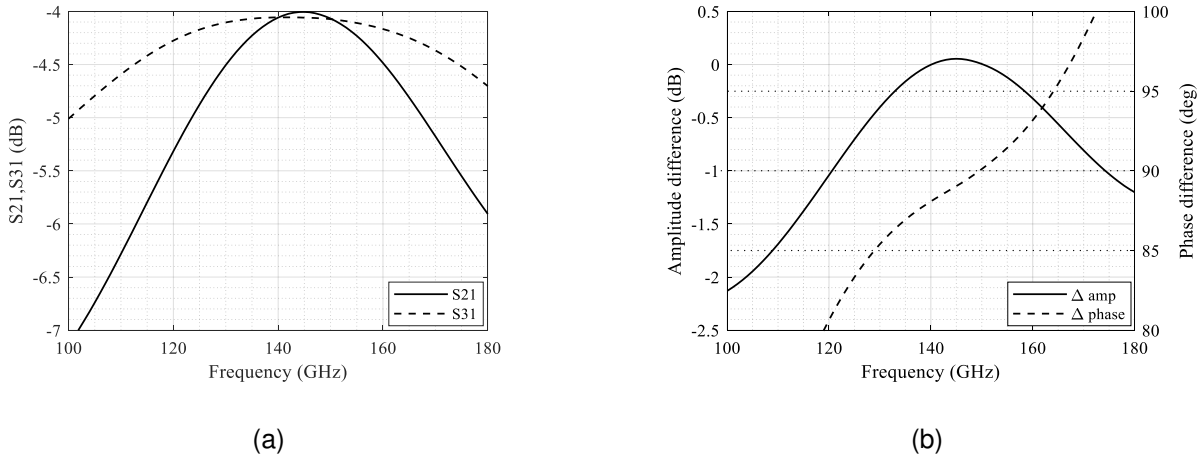
Fig. 15. Simulated performance of the BLC. (a) S21 and S31. (b) The amplitude and the phase difference of the two outputs.
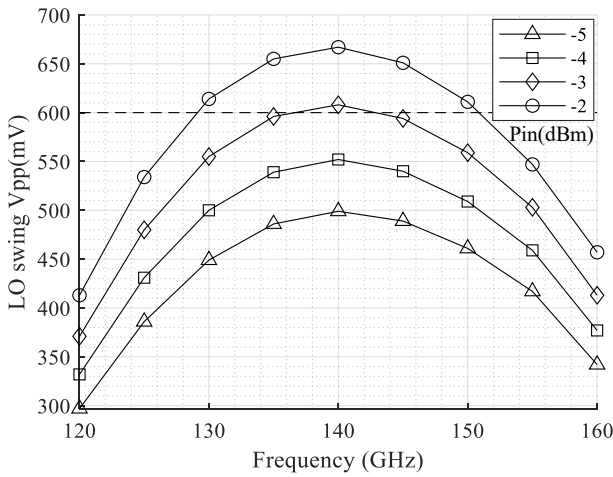

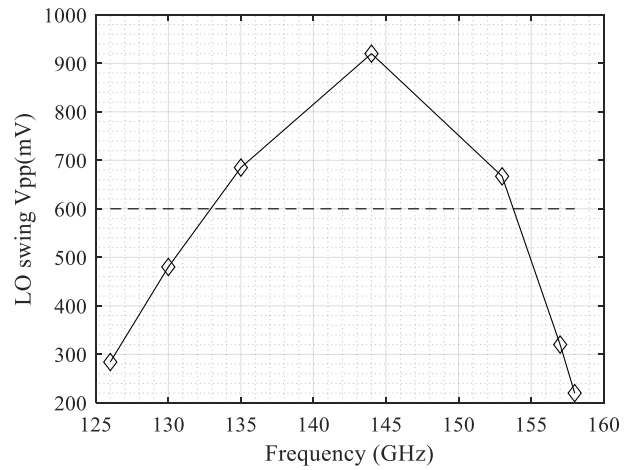Fig. 16. Variation of the LO swing with the input power to the BLC.

Fig. 17. Simulated LO swing at the mixer gates.

x9 chain is simulated to check the swing at the mixer gates and the results are as shown in Fig.17. With the input power of 8 dBm at the x9 input, the LO chain yields 600 mV and above swing from 134 GHz to 154 GHz consuming 48 mW in total.

VI. BASEBAND SECTION

In the section II, the spillover and its dependency on the chirp duration and the choice of the filter to mitigate its effect is discussed. The design of such filter and the baseband circuits used in the I and Q paths are discussed in detail in this section. The baseband architecture as shown in the Fig.18 consists of a source degenerated high pass (HP) filter after the mixer, followed by an N-path filter with 8 12.5% duty-cycled clocks. The variable gain in the baseband is obtained by a Gm-C filter which also provides a third order low pass (LP) filter with an additional HP filter.

A. Active High-pass filter

In the down-converted IF signal, the spillover can modulate with the other target tones to produce undesired intermodula-
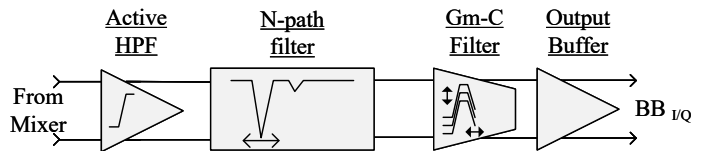

Fig. 18. Top-level architecture of the baseband.

tion tones, if the spillover is large. Since the IM product of the spillover and the target tones are in-band, they can not be addressed once the spillover voltage is converted to current in the G_m stage following the mixer. The active HP filter proposed in [31] addresses the spillover voltage-to-current conversion by degenerating the G_m at the source of the input differential pair at low frequencies while operating as a normal differential pair at high frequencies. The simplified schematic of the filter is shown in Fig.19 (left). In this work the filter modified from [31] is used a first block and provides 10 dB gain with a first order HP filter with cut-off at 1.6 MHz and consumes 1 mW power.
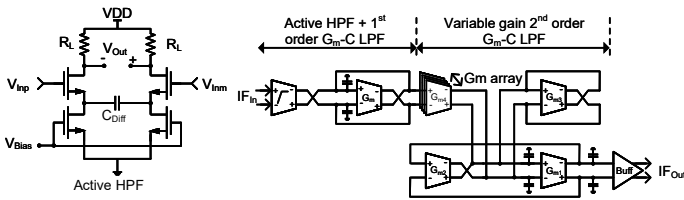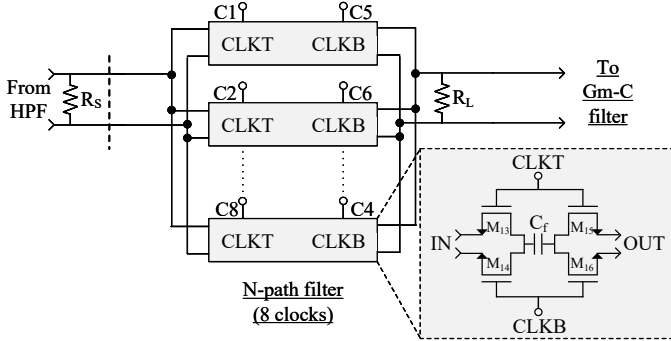
Fig. 19. Simplified schematic of the HPF and G_m-C filter

$M_{13-16} = 30\mu m / 30nm$ (fw = 1μ, nf =30, m=1) , C_f = 60pF, RL = 200KΩ

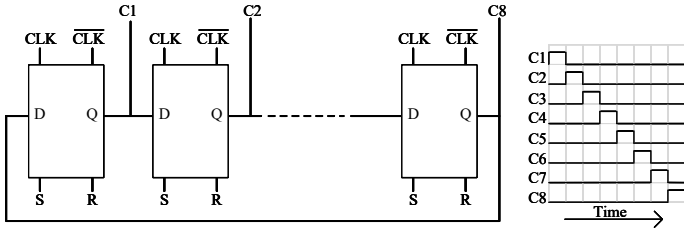Fig. 20. Circuit details of the N-path filter.

Fig. 21. 12.5% DC clocks and the div-by-8 counter.

B. N-path filter

For the narrow band spillover attenuation, an 8 path 12.5% duty-cycle clocked notch filter architecture is chosen. The filter as shown in Fig.20 is implemented as differential structure with 8 parallel switches. Since the filter in this design is differential in nature, this facilitates the re-use of the capacitor C_f. For the detailed design methodology of the N-path filters readers can refer to [40]. The source resistance R_s for the switch is provided by the output impedance of the HPF in the previous stage and a high load resistance R_L is chosen to minimize the insertion loss of the filter. The 8 clocks required for the filter are provided by an on-chip asynchronous counter (Fig.21) where an external clock is divided into 8 12.5% duty-cycled clocks. The simulated transfer function of the filter as shown in the Fig.22 shows an insertion loss of 1.2 dB with a notch depth of 26 dB at fundamental of 20 kHz and the additional notches at the odd harmonics of the fundamental notch due to the differential nature of the filter. As we approach from the fundamental notch frequency towards the HPF cut-off, the effect of these additional notches on the transfer function is negligible hence the filter will not attenuate the targets in-band. The notch frequency is tunable with the external clock, which runs at 8x the chirp rate. The filter is simulated for notch frequencies from 20 kHz to 500 kHz which corresponds to the chirps spanning from 50 μs to 2 μs and a constant 26 dB attenuation is observed.
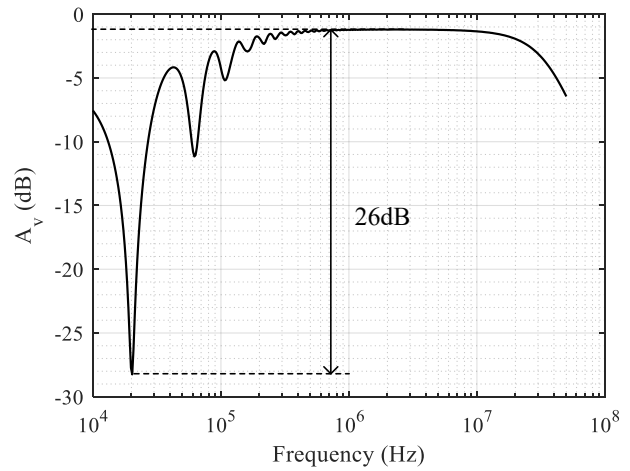

Fig. 22. Simulated transfer function of the N-path filter.

C. Gm-C filters and output buffer

The next stage in the baseband is the modified Gm-C filter which provides a band-pass response unlike the conventional low-pass response. The block uses the principle of the source degeneration used in the first HPF in the baseband for its first order input Gm to provide an additional high-pass filter. The simplified schematic of the G_m-C filter is shown in Fig.19 (right). The Gm-C filter is the re-used from [31] and provides a variable gain of 22 dB. The baseband chain terminates with the output buffer and in-total provides a third order LPF, second order high-pass filter, a tuneable narrow-band notch, and a variable gain of 8-30 dB while consuming 10 mW for both I and Q paths as shown in Fig.23.

D. Receiver: System linearity summary

In this section, simulated system linearity for the in-band targets and the spillover is discussed. For both the cases the RX front-end linearity remains the same, for the baseband depending on where the signal or spillover is, the linearity changes. For the RX front-end (LNA+mixer) the IP1dB is -22 dBm and the in-band IP1dB for the baseband is -25 dBm thus yielding the overall in-band IP1dB of -48 dBm. From the Table II, the largest signal in-band corresponding to the 12 dBsm target at 0.5 m has the power at the input of -50 dBm hence, the receiver doesn't saturate.

For the baseband, when the spillover is at 150 kHz, the receiver can tolerate upto -0.7 dBm of spillover power before the in-band compression starts. Thus, putting the SP1dB of the baseband to -0.7 dB. However, the front-end still has IP1dB of -22 dBm, thus the overall SP1dB of the receiver is -26 dBm. From the link budget assumptions in Table I, the spillover level at the input of the LNA is -27 dBm thus the receiver is 2 dB away from the compression and with the assumed spillover coupling of -35 dB, the receiver will not saturate. When the filter is turned on, overall receiver SP1dB will not improve as the blocks before the N-path filter limit the linearity of the receiver. However, in terms of SNDR as explained in section III, the inclusion of the N-path filter is still beneficial for the radar operation. The summary of the compression values is given in Table III.
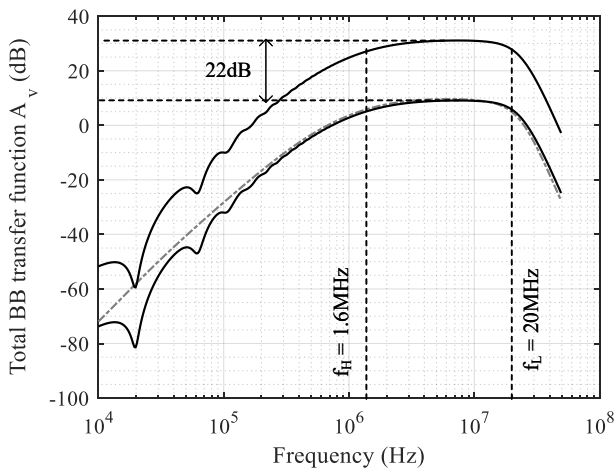
Fig. 23. Simulated transfer function of the baseband.

VII. MEASUREMENTS

The receiver is characterized in two parts. First as a standalone receiver, and then with an on-PCB TX for the spillover and radar measurements. In this section the details on the measurements are given with the setup and discussion.

A. RX characterization

The on-chip antenna present in the RX simplifies the measurements at mm-wave frequencies. To characterize the RX, a D-band horn antenna driven by a VDI D-band extender module is connected to the network analyser PNA-X and the input to the RX is sent over the air. Since the noise contribution of the on-chip antenna is not directly distinguishable from the receiver noise figure and the antenna cannot be measured separately, the measured noise figure is expressed as Effective isotropic noise figure (EINF) [41]. The distance between the horn antenna and the RX is measured and is used for calibrating the measured RX output parameters. Although coupling between all the passives in the LNA has been modelled and extracted to a large extent as described in section V, some undesired gain ripple was noticed during measurements. This has been attributed to the coupling from the LNA to the on-chip antenna, which was unfortunately a structure too complex to be extracted in our EM modelling tool. To reduce this effect, the LNA gain is lowered by reducing its supply to 0.5 V for all measurements. For the conversion gain (CG) measurement of the receiver, a 16 GHz tone at the LO is synchronously swept with the 144 GHz input at the horn antenna with 5 MHz offset. The resulting gain at constant IF of 5 MHz over the RF sweep is as shown in Fig.24. The minimum and maximum CG is 33 dB with a 3 dB BW of 16.4 GHz (139.5-155.9 GHz) and 55 dB with a 3 dB BW of 18.1 GHz (139.5-157.7 GHz), respectively. Compared with the simulated CG, the RF band

TABLE III
SUMMARY OF RX LINEARITY

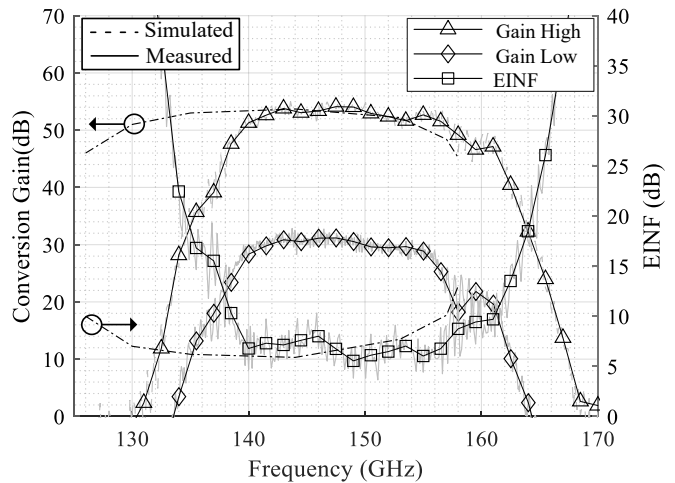| Specification	Obtained	Required
SP1dB (dBm)	-26	-27
IP1dB (in-band) (dBm)	-48	-50

Fig. 24. RF conversion gain and the EINF of the receiver.

has shifted to the higher frequency that can be attributed to the modeling inaccuracies at D-band. Since the antenna cannot be measured separately, the RX NF is expressed as EINF. At 148 GHz an EINF of 5.6 dB is observed with less than 3 dB variation across the BW from which a NF of 8 dB is estimated for the RX. The ripples on the CG and EINF curves result from reflections between the on-chip antenna and the PCB and can be eliminated by placing absorber material on the surface of the PCB around the chip.

The baseband profile as shown in Fig.25 exhibits a gain of 54.5 dB at 150 GHz RF and 6 dB EINF in the passband agreeing with the RF measurements. A HPF corner of 1 MHz is observed, and due to the parasitic pole appearing in the switches of the N-path filter, the IF bandwidth is reduced to 9.3 MHz. For the receiver characterization, the N-path filter is turned off. To characterize the N-path filter in the baseband, the filter is turned on and the external clock which is 8 times the desired filter frequency is given. For different filter frequencies, the response of the RX is as shown in Fig.26. The N-path filter as designed produces a notch providing
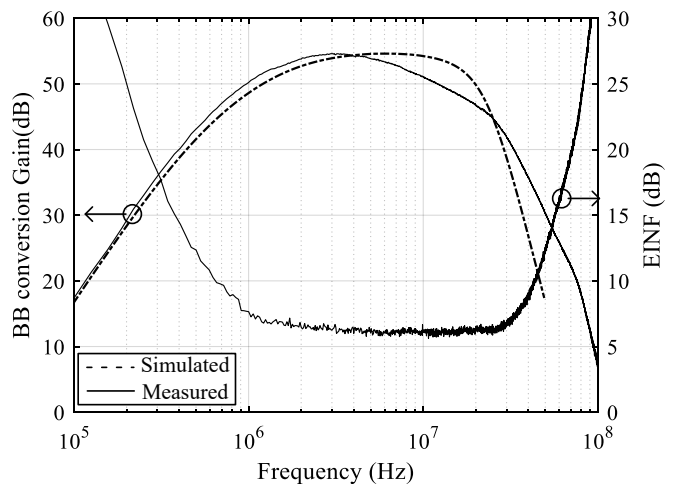

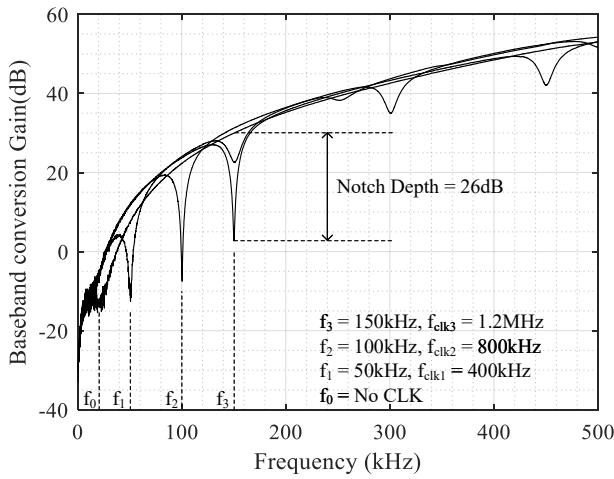Fig. 25. BB conversion gain and the EINF of the receiver.

Fig. 26. Baseband conversion gain with N-path filter.

an additional suppression of 26 dB in comparison with the normal baseband profile. With three test cases of 50 kHz, 100 kHz and 150 kHz the notch depth remains almost constant. While the N-path filter is active, the rest of the baseband profile after the 5th harmonic of the notch frequency, remains largely undisturbed. The tested range of filter frequencies can be translated to the chirps ranging from 20 μs to 6.6 μs and TX-to-RX separation of 15 mm to 45 mm for a 20GHz/20μs chirp slope, enabling spillover attenuation for a large range of chirp duration and the TX-to-RX separations.

B. Spillover and N-path filter characterization

For the spillover measurements, a TX operating in the same frequency band [38] is placed 1 cm apart on the PCB and the setup is shown in Fig.27. Two LOs corresponding to the TX and the RX are swept together at RF with an offset of 150 kHz. As a result, the spillover at baseband is also made to occur at 150 kHz at any given RF. This is equivalent to a 6.6 μs chirp duration and depicts the scenario where the spillover is at higher frequency due to faster chirps. This baseband output is read out into the PNA-X and for the next run, the N-path filter is activated with an external clock 8 times the 150 kHz i.e. 1.2 MHz. The difference in the output power of the RX and the achieved attenuation is shown in the Fig.28. Across the RF profile, the 150 kHz spillover is attenuated by 26 dB and the same holds for variable clock frequencies.
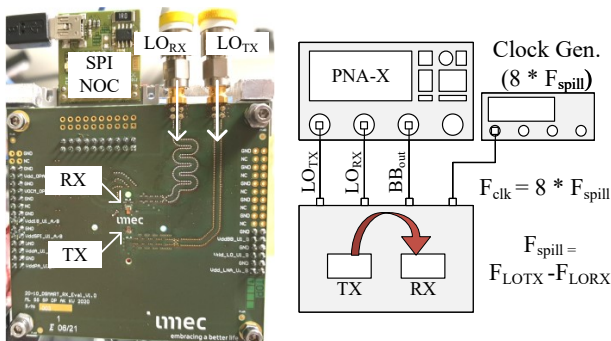

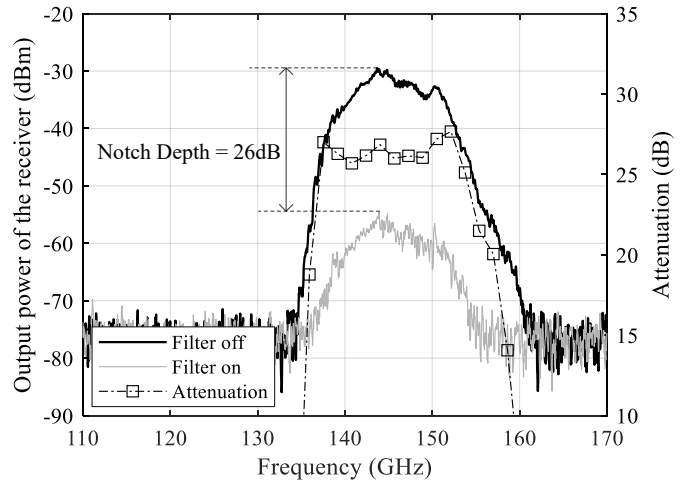Fig. 27. Radar PCB with TX and measurement setup for the spillover.

Fig. 28. Spillover attenuation with N-path filter.

The selectivity of the filter can also be used on a very large nearby non-spillover target in real scenarios. To demonstrate this, a chirp is generated from an instrument (Keysight M8195A) with the chirp duration of t_c= 40 μs, with t_{up} of 35 μs and t_{down} of 5 μs. The filter clock frequency is still taken as 8 times the required filter notch frequency in the presence of finite down-chirp. The filter clock is not correlated with the start of the chirp and the clock is continuously running, spreading the 8 phases over the t_{up} and t_{down}. The filtering happens at the beginning of the baseband chain in the time domain, and the frequency corresponding to the 1/8th of the clock is attenuated, and the rest of the higher frequencies are primarily unaffected. For the addressing distortion caused by the spillover during the t_{down}, the samples collected during the down chirp time is simply discarded as the IF information during the down chirp time is not required. The filter is tuned to attenuate the nearby large target present at 200 kHz (Fig.29). When the filter is turned on, the selected target gets attenuated by 19 dB while the other targets for example at 750 kHz remain unaffected. The observed attenuation of 19 dB is less than the previously characterized attenuation of 26 dB due to the noise levels of the baseband signals. In the spectrum
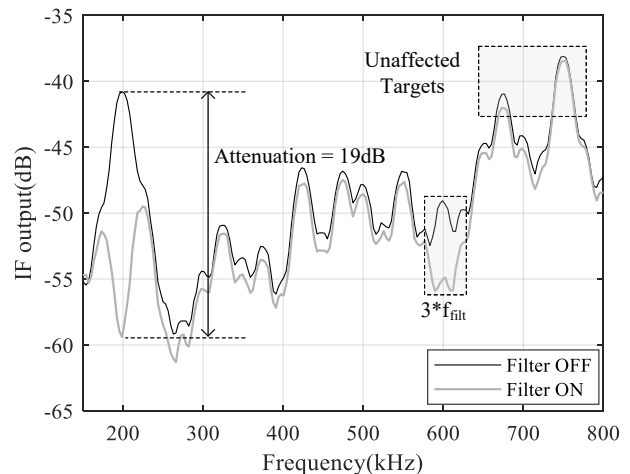

Fig. 29. Selective attenuation of the nearby target.

TABLE IV
COMPARISON WITH THE STATE-OF-THE-ART D-BAND RADAR RECEIVERS.

	This work	[15]	[33]	[42]	[43]	[43]	[44]	[45]	[46]
Technology	**28 CMOS**	28 CMOS	65 CMOS	SiGe HBT	130nm SiGe	130nm SiGe	130nm SiGe	130nm SiGe	22nm FDSOI
Architecture	**FMCW**	FMCW	Pulsed	FMCW	FMCW	FMCW	FMCW	FMCW	FMCW
Antenna	**On-Chip**	On-chip	In PKG	-	-	-	On-Chip	-	-
Frequency (GHz)	**147**	145	161	143	130	124.5	160	120	155
RF BW (GHz)	**18**	13	7	14	32	11	8	12	9
RF CG (dB)	**55**	87	29	19.5	25	13	24	12.5	15
NF (dB)	**8#**	8	22	13.5	19	11.8	--	13	7.5-10
R_{res} (mm) ideal/measured	**8.3 / 13**	11.5 / 30	21/ --	10.7 / 30	5 / --	13 / --	18.7 / 32	12.5 / --	16.6 / --
Area (mm^2)	**3.6**	3.3	20	--	0.14$	0.1$	5.4	2.07	2.75
Power (mW)	**67***	114	1250	370+	425	326	1.05	66$	87.5$
# : Estimated from EINF, *: LNA measured with 0.5V VDD, +: TRX power, $: Front-end only									

Fig. 30.   Range resolution of the receiver.

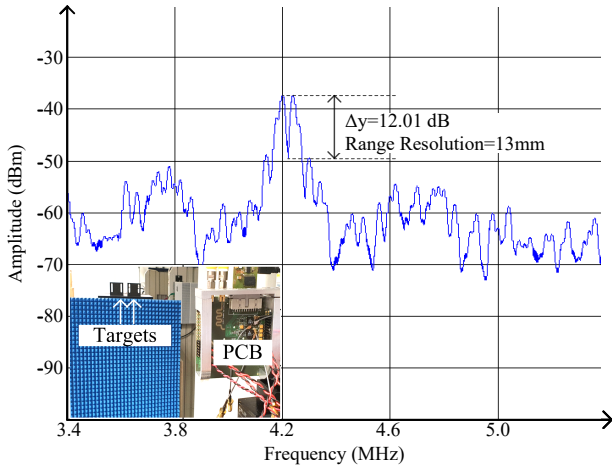Fig. 31.   Moving target detection with the filter.

shown in Fig.29 the IF tones can be observed at harmonics of 25 kHz ($1/t_c$) as described in Section II.

With the presence of the on-PCB TX, the system measurements of the radar are conducted next. As a validation of the 18 GHz RF bandwidth, the range resolution (R_{res}) measurements were setup as shown in the bottom left of the Fig.30. The LO chirp centered at 16 GHz with 2 GHz bandwidth was given to RX and TX. Two identical targets are kept orthogonal to the radar and one of the target is moved towards the other target and the separation in the main-lobes of the tones in the spectrum is observed. At the distance of 13mm between the targets a 12 dB amplitude difference is observed and upon moving the targets closer, the difference drops and the targets are no longer distinguishable. Thus a R_{res} of 13 mm is obtained. The deviation in the R_{res} of 8.3 mm (RF BW = 18 GHz) can be attributed to the window function [35] ($w_f = 1.5$ for Hanning) yielding $R_{res}*w_f = 12.5$ mm while 13 mm was measured.

As a crucial last experiment, the radar is subjected to the velocity measurement of the moving targets. As demonstrated in Fig.29, the amplitude of the targets in non-filter frequencies are

not affected. Similarly to validate the phase domain distortions introduced by the filter, the velocity measurements are done on a moving target and compared with the results obtained when the filter is turned on. A motorized target moving towards and away from the radar is captured and the results are shown in Fig.31. The target is moving with the speed of ±1 m/s (+ for towards the radar and - for away from the radar) between 1.5 m and 1 m range, and is captured with the same range and velocity in both cases. This demonstration concludes the experiments and asserts the N-path filter's compatibility with the radar operations.

With these results the receiver is compared with the state-of-the-art D-band radar receivers in Table.IV. The designed receiver with center frequency of 147 GHz achieves 18 GHz of bandwidth, 13 mm R_{res} with 8 dB NF for 67 mW of continuous mode power consumption. The work is comparable or better than the state-of-the-art in terms of NF, Bandwidth and power consumption with a unique 26 dB of narrow band spillover attenuation.

VIII. Conclusions

A low-power D-band I/Q radar receiver in 28 nm CMOS is presented. The study of the spillover and chirp duration dependency is presented and from that a filtering approach has been derived. A linear low-power front-end with an 18 GHz bandwidth qualifies as a scalable MIMO receiver element and supports complex sensing scenarios with a 13 mm range resolution. At baseband, an N-path narrow band filter is designed and is adaptable to the chirp duration spanning from 20 μs to 6.6 μs and TX-to-RX distances of 15 mm to 45 mm. The filter provides a narrow-band 26 dB spillover attenuation without affecting the range or Doppler functionality of the radar. The baseband circuitry is capable of handling multiple spillovers and has proven to selectively remove the nearby targets. The work stands out among the state-of-the-art receivers in terms of achieved bandwidth, noise figure and power consumption with a unique narrow-band spillover attenuation.

Acknowledgments

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IX. Biography Section

Anirudh Kankuppe (Graduate Student Member, IEEE) received the M.Sc. degree in Microelectronics and Microsystems from the Hamburg University of Technology, Hamburg, Germany in 2017. He was a Design Engineer with Cadence Design systems, India from 2012 to 2014. During his M.Sc., he was a recipient of Gifted Student Scholarship from TU Hamburg and National Merit Scholarship from Government of India in 2005. He is pursuing a Ph.D. in mm-wave and RF integrated circuits with Vrije Universiteit Brussel, Brussels, Belgium in collaboration with imec, Leuven, Belgium and currently working as a Researcher in the Advanced RF group at imec, Leuven, Belgium.

His research is focused on mm-wave radar circuits, receivers and wireline ADCs.

Sehoon Park (Graduate Student Member, IEEE) received the B.Sc. degree in electronic engineering from Hanyang University, Seoul, South Korea, in 2014, and the M.Sc. degree in information technology from the University of Stuttgart, Stuttgart, Germany, in 2017. He is currently pursuing the Ph.D. degree at Vrije Universiteit Brussel (VUB), Brussels, Belgium, in collaboration with imec, Leuven, Belgium.

His research interests include mm-wave/sub-THz integrated circuits and radars.

Kristof Vaesen (Member, IEEE) received an industrial engineering degree in 1996 and a M.S. degree in electrical engineering from the Catholic University of Leuven, Belgium, in 1998. He joined the High Density Interconnect and systems Packaging group, imec, Leuven, Belgium, later in the same year. He started working on single package integration of RF front-ends and has been designing RF building blocks in thin film RF MCM-D technology. In 2012, he joined the mm-wave design group of imec.

Since then he's research activities were focused towards the design and modeling of mm-wave passives and the implementation of CMOS mm-wave circuit blocks.

Dae-Woong Park (Member, IEEE) received the B.S. degree from the Department of Semiconductor Systems Engineering, Sungkyunkwan University, Seoul, South Korea, in 2013, and the M.S. and Ph.D. degrees from the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2015 and 2018, respectively. From 2018 to 2019, he was with the Information and Electronics Research Institute, KAIST, as a PostDoctoral Research Fellow. Since 2019, he has been with mm-wave team, Interuniversity Microelectronic Center (IMEC), Leuven, Belgium, as a senior researcher.

His interests include device physics, extremely high-frequency (THz), mmwave, RF integrated circuits, and systems based on CMOS technology.

Barend Van Liempd (Member, IEEE) received the B.Sc. and M.Sc. degree in electrical engineering at the Eindhoven University of Technology, Eindhoven, The Netherlands, in 2009 and 2011, respectively, and the Ph.D. degree in 2017 at the Vrije Universiteit Brussel, Brussels, Belgium, in collaboration with imec, Heverlee, Belgium. His Ph.D. dissertation concerned tunable, highly integrated RF front-end circuits and modules in SOI CMOS.

Since 2011 he was with IMEC, first as an R&D Engineer, and later as a Senior Researcher and Program Manager. He was appointed R&D Manager in 2021, and now leads imec's neuromorphic radar team. His research interests are RF and mm-Wave circuits for wireless and sensing applications.

He has authored or co-authored more than 50 papers, patents and patent applications. He was the (co)recipient of the 2015 NXP Prize at the European Microwave IC (EuMIC) conference and the 2019 Lewis Winner Award for Outstanding Paper at the International Solid-State Circuits Conference (ISSCC).

Siddhartha Sinha (Member, IEEE) graduated with a Bachelor's Degree in Electronics Engineering from Visweswaraya Technological University, India in 2003 and a Master's Degree in Microwave Engineering from Technical University Munich, Germany in 2008. Between 2004–2006, he was employed as a scientist at Defence R&D Organisation (DRDO), Bangalore, India. Between 2010–2015, he was a scientist with the Ferdinand-Braun-Institut (FBH), Berlin, Germany. Since 2015, he is a researcher at IMEC, Leuven, Belgium.

His research interests include electromagnetic simulations and equivalent circuit modeling, millimeter wave and sub-terahertz interconnects and components, microwave metrology, millimeter wave phased array antennas, MIMO systems and antenna measurements.

Piet Wambacq (Senior Member, IEEE) received the M.Sc. degree in electrical engineering and the Ph.D. degree from Katholieke Universiteit Leuven, Leuven, Belgium, in 1986 and 1996, respectively. In 1996, he joined imec, Leuven, where he is currently a Fellow, working on analog/RF/mm-wave IC design in various technologies for wireless applications. Since 2000, he has been a Professor with Vrije Universiteit Brussel (VUB), Brussels, Belgium. He has authored or coauthored six books and more than 300 articles in edited books, international journals, and conferences.

Dr. Wambacq was a member of the Program Committee of the Design, Automation and Test Conference (DATE) from 2000 to 2007. He has been a member of the Program Committee of International Solid-State Circuits Conference (ISSCC) from 2012 to 2020 with the role of RF Subcommittee Chair from 2016 to 2020. He was a corecipient of the Best Paper Award at the DATE in 2002 and 2005 and the EOS/ESD Symposium in 2004, the Jan Van Vessem Award for the Outstanding European Paper at ISSCC 2015, and the Best Paper Award at the International New Circuits and Systems Conference (NEWCAS) 2019 Conference. He currently chairs the RF Subcommittee of European Solid-State Circuits Conference (ESSCIRC). He was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I from 2002 to 2004. He has been a Distinguished Lecturer of the IEEE SolidState Circuits Society from 2016 to 2018.

Jan Craninckx (Fellow, IEEE) received the M.S. and Ph.D. degrees (summa cum laude) in microelectronics from the ESAT-MICAS Laboratories, KU Leuven, Leuven, Belgium, in 1992 and 1997, respectively. His Ph.D. work was on the design of lowphase noise CMOS integrated voltage-controlled oscillators (VCOs) and phase-locked loops (PLLs) for frequency synthesis.

From 1997 to 2002, he worked at Alcatel Microelectronics (later part of STMicroelectronics), Brussels, Belgium, as a Senior RF Engineer on the integration of RF transceivers for Global System for Mobile Communications (GSM), digital enhanced cordless telecommunications (DECT), Bluetooth, and WLAN. In 2002, he joined imec, Leuven, as a Principal Scientist working on RF, analog, and mixed-signal circuit design. He is currently an imec fellow. He has authored or coauthored more than 200 articles, book chapters, and patents. His research focuses on the design of RF transceiver front ends in nanoscale CMOS, covering all aspects of RF, mmwave, analog, and data converter designs.

Dr. Craninckx has been a Regular Member of the Technical Program Committee for several SSCS conferences. He was an elected SSCS AdCom member from 2017 to 2019. He was the Chair of the SSCS Benelux Chapter from 2006 to 2011. He also serves as an RF Subcommittee Chair of the IEEE International Solid-State Circuits Conference. He was an Associate Editor and the Editor-in-Chief of the IEEE JOURNAL OF SOLID-STATE CIRCUITS from 2009 to 2016 and 2016 to 2019, respectively. He was an SSCS Distinguished Lecturer from 2012 to 2013.