

Joule heating investigation for advanced interconnect schemes with airgaps

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Abstract— In this paper, we present a modeling study to investigate the self-heating effect on advanced metallization schemes with airgaps using an experimentally calibrated finite element model. We compared N3 technology node with N2 integrated with airgaps. Despite the higher metal density of the fully dense Ru lines (50%) at the lower metal levels in the N2 structure with airgaps, the N2 stack is more susceptible to self-heating than the N3 structure with 25% line density, showing that the IMD has an important impact on the interconnect self-heating. We quantified the effect of the line density and IMD on the interconnect temperature increase. We found that decreasing the line density from 50% to 15% increases the temperature with 40% in the interconnect structure. A reduction of the low-k thermal conductivity values below 1 W/m-K shows to accelerate the temperature increase in the BEOL.

Keywords—*BEOL, Scaled interconnect, Joule heating, Finite element model, Ru lines, Airgaps.*

I. INTRODUCTION

Ru already proves to be a good alternative metal to replace Cu due to its superior reliability. Ru metallization shows to have an excellent electromigration behavior [1, 2], and it has proved to be a barrierless option [1] even when integrated with airgaps [3]. However, what is still a concern is the temperature rise due to Joule heating [4]. The increase of required current density and electrical resistivity due to scaling combined with poor thermal conductivity of low-k dielectric material increases the susceptibility for Joule heating at operation conditions. It becomes even more severe when these low-k dielectrics with already poor thermal conductivity are replaced by airgaps. High temperature levels trigger several reliability issues, such as an increase in mechanical stresses which could lead to delamination and enhanced electromigration. In this paper we use a combination of temperature measurements and finite element modeling (FEM) to investigate the Joule heating on advanced metallization schemes with airgaps.

II. MODEL CALIBRATION

A 3D finite element model has been created accordingly to the 2-metal level Ru interconnect with airgaps. The detail of the test structure is presented in [3, 5]. Figure 2 shows the detail of FE model.

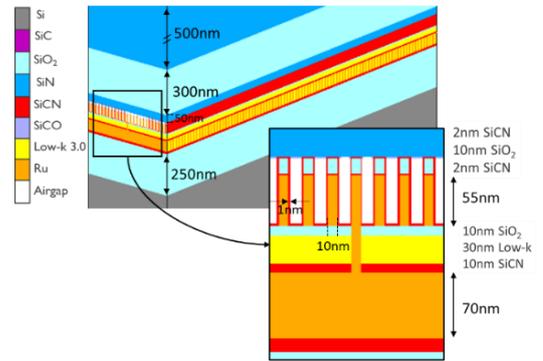


Figure 2: Finite element model of 2 metal level Ru lines with airgaps

Measurements were conducted on lines with a critical dimension (CD) of 10 nm and a length of 100 μm . To quantify the self-heating, two sets of experiments were performed. In the first one, the current is sent through M2 lines without via connection and the average heating is estimated in the same line. The other experiment is proposed to investigate the effect of the via, thus the current is sent from M1, through the via to reach M2 where the heating is estimated. The temperature increase is calculated based on the R. vs. T and R vs. I trend through (1) [1, 4]. The estimated temperature increase is an average over the entire structure:

$$\Delta T = \frac{\Delta R}{R_0} \frac{1}{TCR} = BI^2 \quad (1)$$

The results of joule heating measurements are used to calibrate the FEM.

The Joule heating results are shown in Figure 3. For both sets of experiments the FEM results agreed very well to the heating measurement. The measurement results show no significant difference between the 2 sets of experiment, thus by these experiment no impact of the via is observed. However, it is important to remind that the heating measurement considers the average temperature increase along the entire structure.

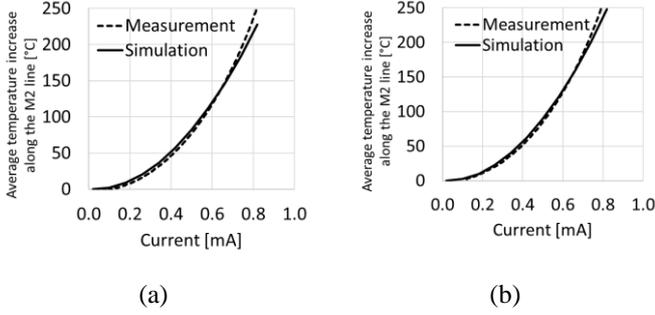


Figure 3: (a) Currents sent to M2 and heating measured in M2 and (b) Currents sent to M1 and heating measured in M2

The absolute temperature along the M2 line is obtained from FEM and shown in Figure 4. The temperature in M2 line is constant when the current is sent through M2, Figure 4 (a). However, by sending currents from M1, a high temperature at the edges of M2 is observed at the via position, Figure 4 (b). This high temperature is induced by current crowding at the small via. Since the heating measurement considers only the temperature average along the line, it is not possible to observe the local heating generated by the presence of the via in the experiments results.

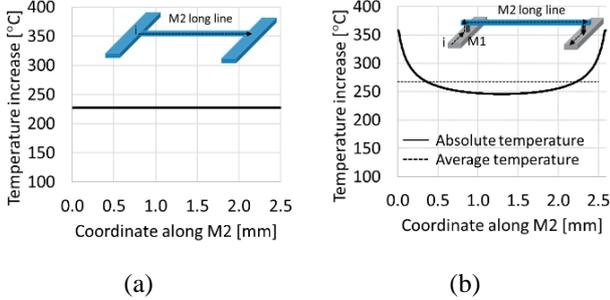


Figure 4: Temperature along M2 line at 100µA for (a) currents sent through M2 and (b) current sent through M1

Only by combining heating measurement and calibrated FEM is possible to thoroughly investigate the effect of the temperature rise in the interconnect structure. Additionally, it is possible to examine the presence of local hot spots. This hot spot can increase mechanical stresses which could lead to delamination and enhanced electromigration.

III. ADVANCED METALIZATION SCHEMES

A 3D coupled electric-thermal finite element model (FEM) has been used to investigate the Joule heating effect on an advance metallization scheme. The analysis has been performed using a commercial FEM software, MSC Marc®. The model based on N3 technology node will be compared with a more advanced node, N2, integrated with airgaps (AG). The model consists of a 12-metal level BEOL structure. The dimension of Mint and M2 lines are 11nm wide lines with aspect ratio (AR) 2.5 and 9nm wide line, AR 3 for N3 and N2, respectively. M1 and M3 are 15nm wide line AR 2 for N3 technology node while for N2, these lines are 14nm wide line AR 2. Mint, M1 and M2 are Ru lines for both technology node. N2 still has Ru M3, while N3 presents Cu lines in the same metal level. From M4 to M12, the lines are Cu. M4 and M5 are 25nm AR 2 and 24nm AR 2 for N3 and N2, respectively. From M6 to M12 the lines present a more relax dimension being 40nm Cu wide lines with AR 2. The more advanced technology node, N2, present airgap from M1 to M3

Ru lines. Low-k 3.0 is the intermetal dielectric (IMC) for the remaining metal level besides the top M12 on which a more robust SiO₂ IMD is used. Figure 5 shows the details of the FE models with the lines dimension for (a) N3 and (b) N2 technology node.

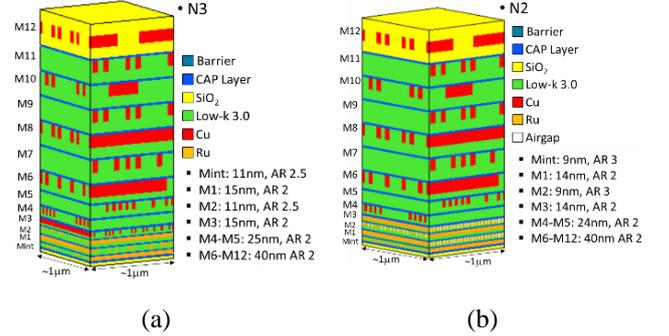


Figure 5: Finite element model of (a) N3 technology node and (b) N2 with airgaps

The vias have been assumed to be randomly distributed with 1% density on each layer. For Cu vias, a TaN barrier has been included in the model since this barrier presents a high electrical resistance and can thus generate a high local temperature. Ru vias have been modeled barrierless.

The line density is assumed to be 25% for all metal levels in the N3 stack. Due to the airgaps surrounding the narrow Ru lines, the N2 model counts on fully dense lines (50%) from Mint to M3, for the higher metal levels a 25% line density is assumed.

For the metal material properties used in the model, the thermal conductivity and electrical resistivity have been derived as function of line width for Ru and Cu lines based on experimental data [6] and Monte Carlo simulations.

Figure 6 shows the boundary conditions applied to the model. For this study, equivalent boundary conditions corresponding to a low power package in a mobile application have been applied on top and bottom of the interconnect structure while the side walls were kept adiabatic, Figure 6 (a). To mimic the power line, voltage was applied to force an electric current to flow from Ru Mint to Cu M12 lines. Additionally, currents have been applied to every vertically running lines connected to the power line, as shown in Figure 6 (b). The electrical current considered in this study ranges from 0 to 100µA at each line.

IV. RESULTS AND DISCUSSION

In order to investigate the effect of the airgap surrounding the narrow Ru lines, the temperature in the Mint, M1, M2 and M3 lines have been isolated and Figure 7 (a) shows the temperature distribution in these lines. Although N2 presents fully dense lines at these levels, it still shows that the extremely poor thermal conductivity of airgap has a major impact on the temperature. Figure 7 (b) shows the temperature increase as function of the current applied. The poor thermal conductivity of airgaps deteriorates the heat removal and leads to a temperature increase of around 20% in Ru lines with airgap at 100µA compared to the N3 stack with 25% line density

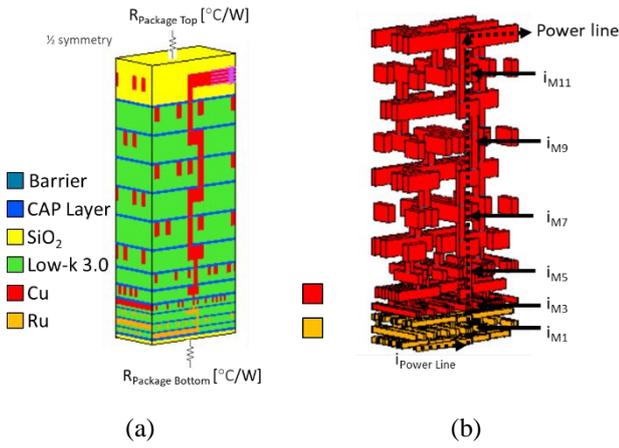


Figure 6: Finite element model boundary conditions: (a) Top and bottom thermal resistance and (b) Electrical current

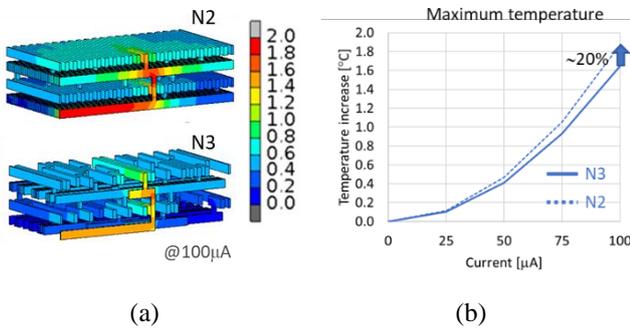


Figure 7: (a) Temperature gradient of Ru narrow lines for N2 and N3 technology node and (b) temperature increase as function of current comparison for N2 and N3

A. Effect of line density

To quantify the effect of the metal content on the Joule heating the line density is varied from fully dense structures down to 15% metal density. In this case the N3 interconnect structure with low-k was used to eliminate the effect of the airgap. Figure 8 shows the maximum temperature increase in the interconnect structure as function of the line density. The result show that by reducing the metal content from 50% to 15% a temperature increases of 40% is observed. The temperature increase is found to be linear with line density.

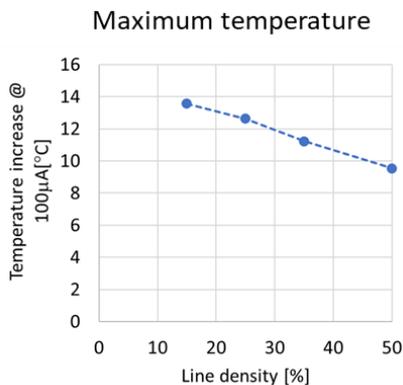


Figure 8: temperature increases as function of line density

B. Effect of Intermetal Dielectric (IMD)

The comparison of N3 and N2 in Figure 7 shows that the IMD is an important parameter to conduct the heat away from the BEOL structure. Thus, it is important to understand the thermal impact of the low-k thermal conductivity. Figure 9 shows the temperature increases in the BEOL as function of the low-k thermal conductivity. The results show a fast temperature increase in BEOL for low-k thermal conductivity below 1W/mK. It is important to note that the thermal conductivity of most of the currently used low-k materials is in this range, increasing the concerning for joule heating.

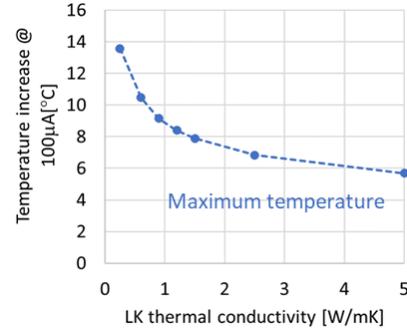


Figure 9: Effect of IMD thermal conductivity on the temperature increase of BEOL structure

V. CONCLUSION

We calibrated our FE model using self-heating measurements on a 2-metal line BEOL structure with airgaps. The calibrated FE model was extended to a more advanced 12-layer BEOL structure to compare the thermal behavior of N3 and N2. Due to the combination of a high electrical resistivity of the scaled metal lines and the use of airgaps with extremely poor thermal conductivity we showed that N2 technology node with airgaps shows to be more susceptible to Joule heating compared to N3 technology node without airgaps. Results shows a 20% increase in the N2 Ru lines with airgaps compared to N3, which suggests a higher reliability risk. Higher metal density showed to help to reduce the self-heating. A reduction of the metal density from 50% to 15% resulted in an increase of 40% for the temperature in the BEOL. The low-k thermal conductivity showed to be a very critical parameter to the heat dissipation, and it was found that temperature in the interconnect structure increases very fast for a reduction of the IMD thermal conductivity below 1W/m-K.

REFERENCES

- [1] O. Varela Pedreira, et al, "Reliability Study on Cobalt and Ruthenium as Alternative Metals for Advanced Interconnects", IEEE IRPS, pp. 6B.2, 2017
- [2] C.-K. Hu, et al, "Future on-chip interconnect metallization and electromigration", IEEE IRPS, pp. 4F.1, 2018
- [3] A. Lesniewska, et al, "Reliability of a DME Ru Semidamascene scheme with 16nm wide Airgaps", IEEE IRPS, 3F.2, 2021
- [4] M. Lofrano, et al, "Joule Heating study in scaled Cu, Co and Ru interconnects", IEEE ITC, Belgium 2019
- [5] G. Murdoch, et al, "Semidamascene Interconnects for 2nm node and Beyond", IEEE ITC, October 2020.
- [6] I. Ciofi, et al., IEEE Transactions on Electron Devices 66, 5, May 2019.