Reliability of Barrierless PVD Mo

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***Abstract*—** We evaluate the reliability of barrierless Mo metallization on various dielectrics that are used in both BEOL and MOL integration schemes. In particular, we assess the risk of metal drift-induced failure in SiO_2, LK3.0, SiCO and Si_3N_4 films by performing TDDB measurements on MIM planar capacitors. We show that Mo does not drift in SiO_2, LK3.0, and SiCO. Despite a thoroughly failure analysis no definitive conclusion could be reached for the Si_3N_4 films.

Keywords—Mo, TDDB, metal drift, barrierless, BEOL, MOL

I. Introduction

As the critical dimension of integrated circuits kept shrinking over the years, it has become clear that a major factor affecting the performances of devices both at the Middle-of-line (MOL) and Back-end-of-line (BEOL) level are the metals used for contacts and interconnects, primarily W and Cu, respectively. Since its commercial introduction in over two decades ago [1], Cu has been the dominant interconnect material due to its low resistivity; however, as the cross-section area of Cu interconnects scaled down, their line resistance increased dramatically [2]. This is due to the fact that the width of the Cu metal lines is larger than the electron mean free path, increasing dramatically the contribution of electron surface scattering to the Cu resistivity [3], [4]. Another detrimental aspect of Cu interconnects is the fact that they require a thick barrier/liner to prevent the diffusion of Cu ions into dielectric films. To preserve its functionality, the barrier cannot be easily scaled, resulting in a smaller Cu cross-sectional area and higher line resistance as the dimensions of interconnect lines are reduced. MOL metal contacts suffer a similar issue: a thick Ti/TiN liner/barrier system is used in conjunction with W. The continuous dimensional scaling has led to a reduction of the volume filled with W compared to the part occupied by the Ti/TiN system, resulting in a significant increase in contact resistance [5]. Moreover, new features, such as Bower Power Rail that would boost device performances, also require novel metallization schemes [6]. Alternative metals have been proposed to overcome this issue and replace both Cu interconnects and W contacts [7]. It has been experimentally shown that metals such as Co, Ru, Mo and Ir have lower resistivity than conventional metals at scaled dimensions [4]. Moreover, many alternative metals require very thin or no barrier/liner at all, allowing for a larger effective conducting metal area and lower line resistance. Co has been already introduced in commercial devices [8] while very promising results have been published for both Ru interconnects [9] and Ru contacts [10] with only a 0.3nm-thick TiN adhesion layer. In this work we study the reliability of barrierless Mo, another promising alternative metal for various applications, on different BEOL and MOL dielectrics. In particular we assess the risk of metal drift induced failure in SiO_2, Si_3N_4, SiCO and Low-k 3.0 (LK3.0) thin dielectric films.

II. Experimental Details

A. Test vehicle and materials

To assess the risk of metal-drift induced failure we relied on metal-insulator-metal (MIM) planar capacitors (p-caps) [11], with an area of 100 µm x 100 µm (Fig. 1a). A 10nm-thick TiN layer, which is not susceptible to metal drift, is used as bottom electrode (BE) while the top electrode (TE) is made using the metallization under investigation. For each dielectric, two metallization schemes were fabricated: (1) reference wafers with a thick TaN/Ta barrier and Cu and (2) wafers with barrierless PVD Mo, capped with 5nm TiN followed by TaN/Ta and Cu to fill the rest of the via. The 4nm-thick TaN/Ta layer ensures that Cu does not drift into the dielectric. The four dielectrics used in this study were: PE-CVD SiO_2, CVD LK3.0, CVD SiCO and PE-ALD Si_3N_4. All films were 20nm-thick, and no adhesion layer was used between PVD Mo and any of the dielectrics. The normal failure mode for the p-caps is intrinsic dielectric breakdown. However, because of the asymmetric design of the test vehicle, different failure mechanisms can be induced depending on the polarity of the stress bias applied to the TE (Fig. 1b): metal drift can occur only at the top interface, where PVD is used for the TE. An overview of the experimental splits is provided in Table I. The reference wafers, fabricated using a long-standing and well-established imec flow, are used to assess the intrinsic dielectric response under for positive stress voltages since they are not expected to be affected by Cu drift.

B. Methodology

Device failure was primarily evaluated by performing Time-Dependent Dielectric Breakdown (TDDB) measurements on the p-caps at 100°C and 200°C. The latter are needed in order to stress devices at low fields, in the filament formation regime [12], while maintaining a reasonable testing time (<10^5 s/device). Various positive and negative electric fields were used to stress the p-caps until failure. After extrapolating the experimental time-to-failure at $t_{63.2\%}$ ($TTF_{63.2\%}$) for each stress field, the power law model ($t_{63.2\%} \sim E^{-m}$) [13] was used to extract the field acceleration factor (m) and the Weibull slope (β), for positive (m_{V+}) and negative (m_{V-}) stress fields separately.

III. Experimental Results

A. Time-Dependent Dielectric Breakdown Measurements

The TDDB data obtained at 100°C and 200°C for all the systems under evaluation are plotted in Fig. 2. Each subfigure shows data from a different dielectric to provide a direct comparison between the barrierless Mo and the reference Cu wafers at each temperature. On the one hand, it is clear from the plots that for p-caps with SiO_2 (Fig. 2a-b), LK3.0 (Fig. 2 c-d) and SiCO (Fig. 2 e-f), positive and

negative TDDB data match well for the two metallization schemes at both temperatures. Very similar failure times were obtained for the barrierless Mo and Cu reference splits, suggesting that the underlying failure mechanism is the same, i.e. intrinsic dielectric breakdown. On the other hand, for both Si_3N_4 wafers (barrierless Mo and TaNTa/Cu), a substantial difference is observed at 200°C between positive and negative TDDB data (Fig. 2g-h). The difference is clearly visible also in Fig. 3, that provides a direct comparison between positive (m_{V+}) and negative (m_{V-}) field acceleration factors for all the systems at 100°C and 200°C. In particular, m_{V+} at 200°C drops significantly for both Si_3N_4 wafers compared to the extracted values at 100°C while m_{V-} is very similar. Normally, such a divergence is considered to be a sign of metal drift-induced failure. However, because it is observed also for the TaNTa/Cu reference wafer, a thorough failure analysis of the two wafers was performed before reaching any conclusion. At the same time, for p-caps with SiO_2, LK3.0 and SiCO, m_{V+} and m_{V-} are nearly identical at both temperatures and metallization schemes, confirming that intrinsic dielectric breakdown is the sole failure mechanism, hence Mo can be used without a barrier in combination with these dielectrics.

B. Failure Analysis on the Si_3N_4 wafers

Because we did not expect to observe metal drift with the TaNTa/Cu reference wafer, a TEM inspection was performed on a pristine die to verify the integrity and continuity of the TaNTa barrier. The three TEM pictures shown in Fig. 4a-c were obtained at three different location of the barrier/dielectric interface. At the bottom of the p-cap (Fig. 4a-b), where the device is stressed, the TaNTa barrier thickness is very close to the 4nm-thick nominal value, sufficient to prevent Cu ions from drifting into the Si_3N_4 film. Although towards the edges (Fig. 4c) the barrier is slightly thinner, the local electric field is not large enough to induce metal drift. It was not possible to inspect p-caps after failure occurred, neither for Cu nor for Mo metallization scheme, to verify the presence of metal at the breakdown location because of the large area of the devices. To further exclude any the impact of the p-cap edges, we compared the current densities, recorded on non-stressed devices, for three different device sizes (100 µm, 50 µm and 10µum) at 100°C (not shown) and 200°C for all the wafers. The J-E curves for the Si_3N_4 and the SiO_2 wafers are plotted in Fig. 5a and Fig. 5b, respectively. J is the same for all the dimensions, confirming that the edges do not play any role in the device failure for neither of the two dielectrics. It is worth noting that J_{Si3N4} is much larger, due to the lower Si_3N_4 band gap compared to SiO_2, LK3.0 and SiCO. Additional TDDB measurements were performed at 150°C in order to obtain additional data points for certain stress fields and extract the thermal activation energies (E_A) for all the samples, as plotted in Fig. 6. For each dielectric, the same field value was used for both stress polarities. As for field acceleration factors, the E_A values obtained for negative stress voltages provide an insight into the intrinsic response of the systems. The extracted thermal activation energy values for SiO_2, LK3.0 and SiCO do not change with stress polarity and metallization scheme, confirming that the failure is driven by intrinsic dielectric breakdown. On the contrary, for the Si_3N_4 wafers there is a clear difference between the E_A values extracted for positive and negative stress fields and the former depends on the metallization scheme. The dependence of the activation energy on stress polarity is also visible in J-E plots in Fig. 5b. Nonetheless, the values are quite low for all the dielectrics and very close to those reported in literature for systems not affected by metal drift-induced failure ($E_A \leq 0.5$ eV) [10], [14], [15]. On the contrary, much higher energy values have been reported for other alternative metals with cohesive energies similar to Mo ($E_A \geq 0.8$ eV) [12], [16]. Finally, we also compared the I-t curves (Fig. 5c-d) and performed Triangular Voltage Sweep (TVS) measurements on both Si_3N_4 samples (not shown). None of the samples showed stress-induced leakage current-like (SILC) behavior and no mobile ions were detected by TVS [17]. None of the applied techniques provided clear evidence that metal drift-induced causes the failure of the two Si_3N_4 wafers. If so, Cu and Mo would be responsible for the reference and barrierless wafers, respectively. In fact, the 5nm-thick capping layer deposited on top of the PVD Mo, provides an additional barrier against Cu drift. Although no definite conclusion could be reached about the Si_3N_4 wafers, based on the additional structural and electrical data collected, we believe that difference between positive and negative TDDB data is likely linked to intrinsic Si_3N_4 characteristics rather than to metal drift. In particular, the large leakage current, makes SiN very sensitive to contact resistance that, in turn, strongly depends on the metal electrode.

IV. Conclusions

We reported on the reliability of barrierless PVD Mo on a range of BEOL and MOL dielectrics. Our study focused primarily on assessing the risk of metal drift-induced failure. Experimental data clearly show that PVD Mo can be used without a barrier, or adhesion layer, on SiO_2, LK3.0 and SiCO dielectric films. The barrierless systems were tested with success against imec TaNTa/Cu reference process. At the same time, we were not able to conclusively show that PVD Mo can be used barrierless also on PE-ALD Si_3N_4. Although, from TDDB measurements it appears that both the Mo barrierless and the Cu reference wafers with Si_3N_4fail because of metal drift-induced failure, the follow-up investigation did not provide clear evidence of it. It is likely that a still-unidentified intrinsic characteristic of the Si_3N_4 films led a strong polar-dependent response under stress.

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Table I. Detailed list of the samples investigated in this study. No barrier/liner was present between the dielectric film and PVC Mo.

Dielectric	Barrier	Metallization
20nm PE-CVD SiO_2	4nm TaNTa	Cu
20nm PE-CVD SiO_2	/	PVD Mo
20nm CVD LK3.0	4nm TaNTa	Cu
20nm CVD LK3.0	/	PVD Mo
20nm CVD SiCO	4nm TaNTa	Cu
20nm CVD SiCO	/	PVD Mo
20nm PE-ALD Si_3N_4	4nm TaNTa	Cu
20nm PE-ALD Si_3N_4	/	PVD Mo

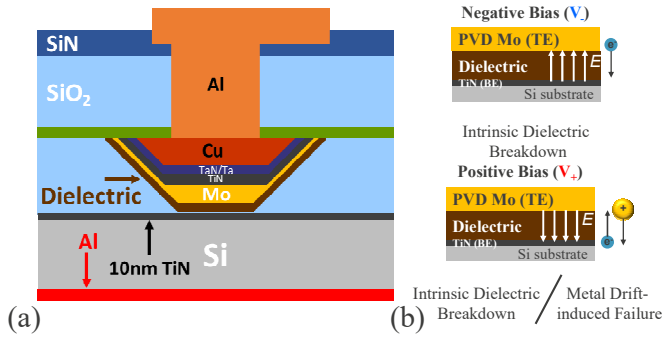

Figure 1. (a) Schematic of the p-cap: the TaN/Ta barrier is needed to prevent Cu from drifting through the TE and into the dielectrics. (b) Different failure mechanisms can be induced depending on the polarity of the stress voltage.

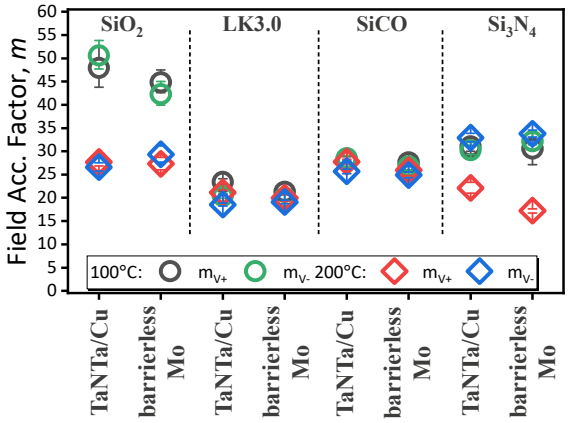

Figure 3. Field acceleration Factors extracted from positive (m_{V+}) and negative (m_{V-}) TDDB data at 100°C and 200°C. Normally, a large mismatch between m_{V+} and m_{V-} is a sign of metal drift-induced failure.

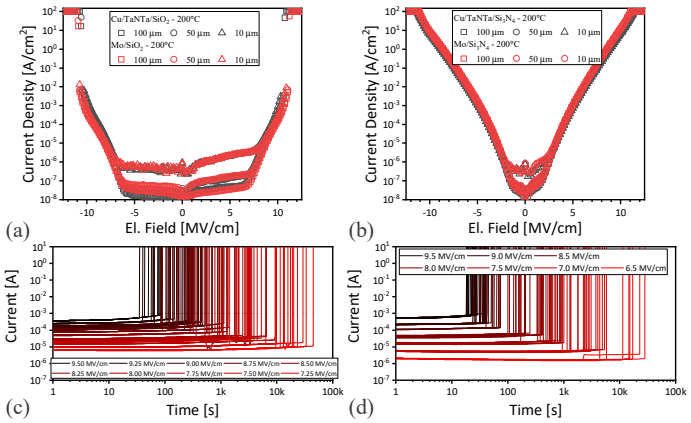

Figure 5. J-E curves obtained for (a) SiO_2 and (b) Si_3N_4 wafers at 200°C on devices with side length of 100 µm, 50 µm and 10 µm. I-t curves for Si_3N_4 wafers with (c) TaNTa/Cu and (d) barrierless Mo metalizations for positive stress fields.

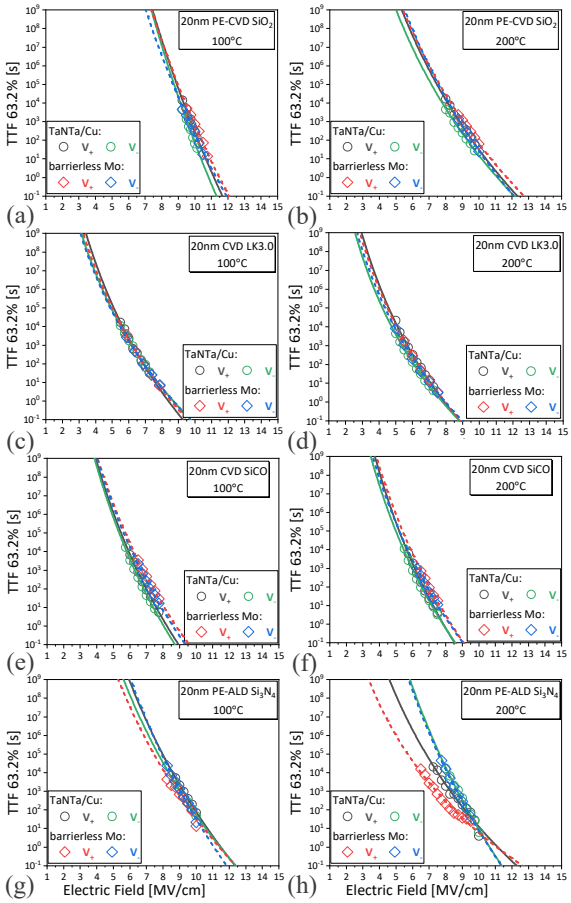

Figure 2. TDDB data obtained at (a) 100°C and (b) 200°C for a wide range of positive and negative stress voltages. TDDB data are grouped by dielectric and temperature: in each subplot a direct comparison between the TaNTa/Cu reference and the barrierless Mo wafers.

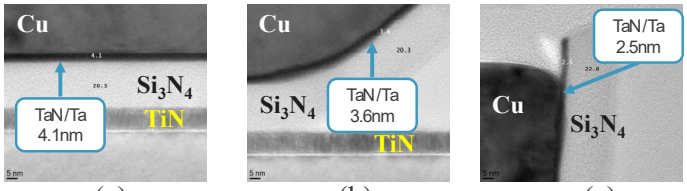

Figure 4. TEM inspections performed at the (a) bottom-center, (b) bottom-edge and (c) top-edge of the Si_3N_4/TaNTa/Cu wafer to verify the thickness of the TaNTa barrier, expected to be 4nm (nominal value).

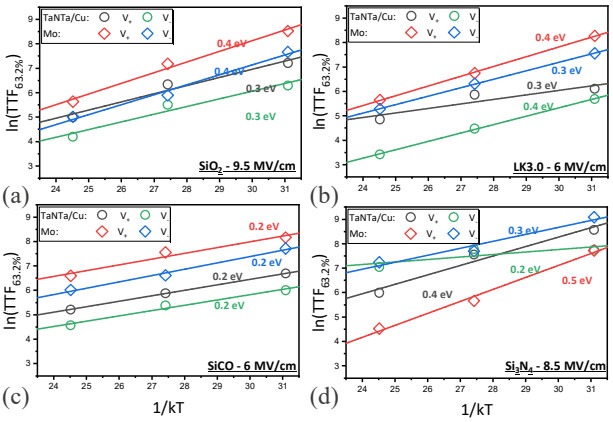

Figure 6. Thermal Activation Energy for (a) SiO_2, (b) LK3.0, (c) SiCO and (d) Si_3N_4, extracted for all the systems from TDDB data at 100°C, 150°C and 200°C using both positive and negative stress fields.