HBM and CDM ESD Performance of Advanced Silicon Photonic Components

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Abstract – ESD robustness for self-protected advanced Silicon photonic components integrated into optical interposers is reported, including industry-first CDM data. HBM performance in reverse bias polarity is shown to be the limiting factor and is correlated to the optical component width. The Ge-EAM modulator with heater is found to be the weakest element CDM-wise.

I. Introduction

Optical I/O (OIO) interfaces using Silicon or other Group IV based photonic components are a promising and upcoming cost-efficient technology for low power and high bandwidth optical links between CMOS ICs at the chip-to-chip or board-to-board level [1]. These OIO interfaces enable data transfer from the electrical domain to the optical domain, and then back to the electrical domain.

For the Si-photonics studied here, at the optical transmitter (TX) end, an external laser beam is modulated by Si or Ge modulators and is then transmitted via Si waveguides in the Silicon-On-Insulator (SOI) optical interposer. At the receiver (RX) end, the optical signal is converted into an electrical signal using Ge photodetectors. Figure 1 illustrates this integration of the optical components with the optical interposer [1-3]. As for other 2.5D interposer integrations, all the optical components are exposed to ESD threats during the assembly [4].

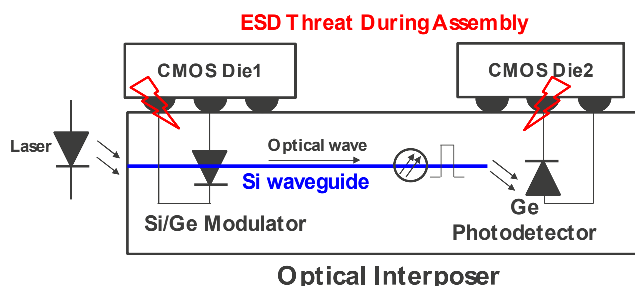

Figure 1: Schematic representation of an optical interposer with external laser beam, Si/Ge modulators, Si waveguide and Ge photodetectors. ESD threats occur during the 2.5D assembly, when the CMOS dies are stacked onto the optical interposer.

Once assembled, the optical I/O interfaces are no longer exposed to ESD threats of the external world. Therefore, the ESD level of optical I/Os must only meet an ESD specification defined by the S20.20 Standard, i.e., 100V HBM and 200V CDM [5].

ESD robustness of Si modulators and Ge photodetectors has been discussed in [4]. In that work, the components could barely pass the HBM ESD specification and no CDM data was presented in that or other publications. A special ESD protection device of a grounded base NPN bipolar transistor was proposed to improve ESD performance; however, adding this dedicated ESD protection device was expected to deteriorate the electrical and optical performance of the OIO components.

A solution adopting self-protecting ESD capability for the Si-photonic components is clearly preferred for commercial optical interposers. Very limited publications have disclosed the ESD robustness of the Si-photonic components in optical interposers [4]. This paper reports ESD data on this approach; both HBM and industry-first CDM measurements of advanced Si-photonic components are presented. Different from [4], Ge photodetectors with a novel contact architecture and modulators with different materials options [1-3] and layout styles are evaluated in this work.

II. OIO Technology and Devices

Here, we have evaluated both Ge photodetectors and the Si/Ge modulators manufactured with a 200mm SOI technology. The cross-section view of the horizontal photodetector is shown in Figure 2a, where a Ge film of ~300nm was grown using selective epitaxy above a

~220nm Si thin film layer [2]. Unlike the vertical device described in [4], this horizontal Ge photodetector has no contact on the top of the Ge film, rather, NiSi contacts were placed at each side of the Ge photodetector into heavily doped Si regions, as shown in Figure 2a. The Ge photodetectors optimized for two different wavelength bands were studied: O-band (1260-1360nm) and C-band (1530-1565nm).

Two types of modulators were also evaluated; firstly, Ge Electro-Absorption Modulators (EAM) [1-3], which operate based on the change of material absorption coefficient; and secondly, depletion-type Si Electro-Optic-Modulators (EOM) [1, 2], which operate based on the phase change of the light. The structure of the Ge EAM is very similar to the Ge photodetectors, with the addition of a thermal tuning heater (required for tight control of the operating wavelength). The Ge EAM had a strip layout style shown in Figure 2b, whereas the Si EOM had a ring layout [3, 4]. Based on their layout styles, the Si EOMs are also commonly known as Si Ring Modulators (RMs) and have the advantages of more compact physical size; yet the Ge EAMs give higher optical bandwidth [2].

The Ge photodetectors and the Ge/Si modulators were directly embedded into the optical interposer with a 500µm long Si waveguide. The four different optical components studied in this work are listed in Table I; they were all optimized for low leakage (dark current) and optical properties.

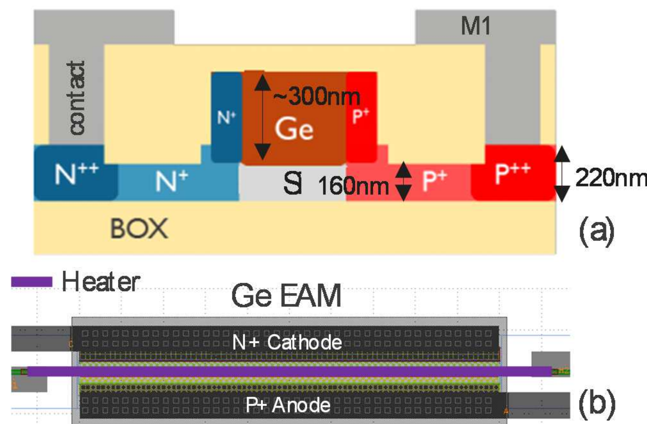

Figure 2: (a) Illustration of the cross-section view of the Ge photodetector in SOI technology. (b) Layout top view of Ge EAM. The heater in the Ge EAM is placed above the Ge epitaxial region.

Table I: The four types of optical I/O components evaluated.

Functions	Devices
Optical I/O Receiver (RX)	O-band Ge Photodetector (PD)
	C-band Ge Photodetector (PD)
Optical I/O Transmitter (TX)	Ge Electro-Absorption Modulator (EAM)
	Si Ring Modulator (RM)

III. ESD Results and Discussion

After the manufacturing, the optical I/O wafer was diced, and the bare dies were assembled into industrial BGA packages for component-level HBM and CDM ESD measurements.

A. HBM ESD

It is important to note that optical components are diodes and can be characterized as such, where positive or negative HBM ESD stress is applied at the p++ anode with respect to a grounded n++ cathode. Device DC I-V curves were characterized from −3V to +1V after each HBM testing level. The positive and negative HBM ESD stresses were increment in +/-25V steps. The ESD passing voltage level was determined from the worst-case of two failure criteria; (i) a decrease of >10% in the forward voltage at a 1µA current level and (ii) an increase of > 500nA in the reverse current at reverse bias of 3V. Figure 3 shows the HBM results of the four optical components listed in Table I.

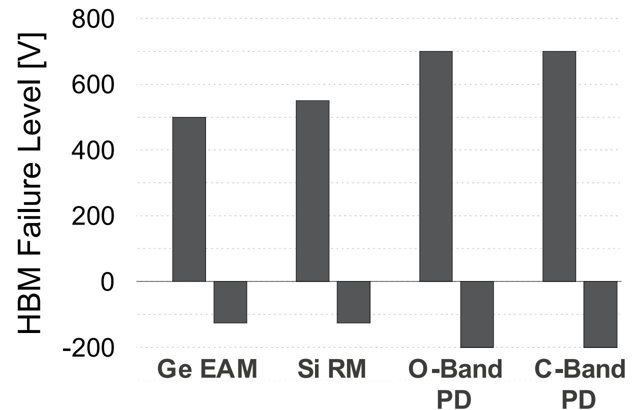

Figure 3: Measured HBM ESD failure levels of the Ge EAM, the Si RM, and the O- and C-band photodetectors (PDs) for positive and negative ESD stresses.

As expected for a self-protected diode, ESD failure levels were much lower for the negative (reverse biased) HBM stress condition. In these four optical components, the Ge EAM had the weakest ESD robustness whilst the Ge photodetectors had the highest robustness. The failure level differences between the devices can be attributed to three aspects: i) the device widths, ii) different materials, and iii) different layout styles.

The HBM robustness is seen to scale linearly with device width for the three Ge devices – the photodetectors (width= 80µm) have correspondingly higher ESD robustness (-200V) compared to the Ge EAM (width= 50µm and ESD robustness= -125V). The Si RM has a similar ESD robustness to the Ge EAM despite much smaller device width (~16µm). Also, the Si RM exhibits a different failure mechanism being more sensitive to failure criterion (i) (forward

voltage) under both positive and negative HBM ESD stress, whereas the Ge EAM was more sensitive to failure criterion (ii) (reverse current), as shown in Figure 4. Fortunately, these optical components all pass the required HBM ESD level of ±100V as defined by the S20.20 Standard. The evaluations of optical/electrical functional performance after HBM ESD stress are described in Section B.

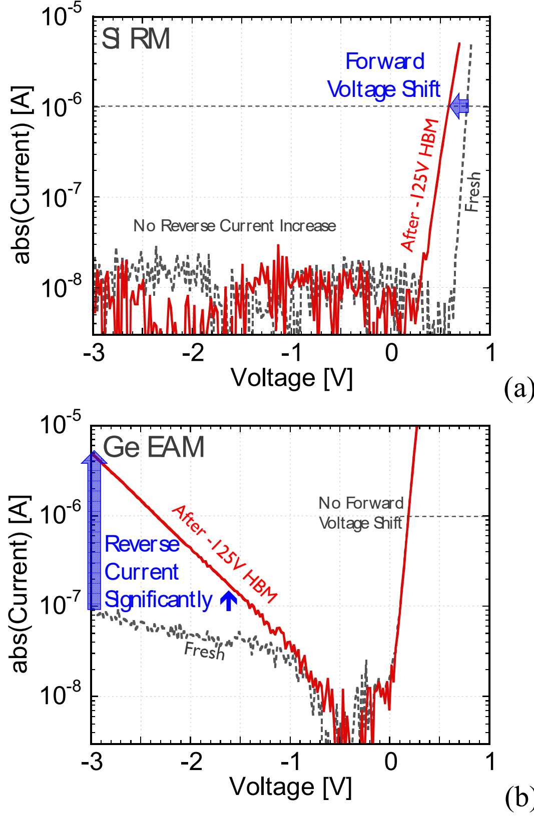

Figure 4: Measured DC IV curves of (a) the Si RM and (b) the Ge EAM before any HBM ESD zap and after the HBM ESD zap of -125V.

B. Performance after HBM Stress

In addition to the DC device behavior after the HBM ESD stress reported in Section A, more detailed analysis of the impact of the HBM ESD stresses upon device performance for the four types of optical components was performed. Device performance was evaluated after two sequential levels of HBM stress: i) ±100V as required to meet the S20.20 specification, and ii) 90% of the observed failure levels for the negative HBM ESD stress condition or 400V for the positive HBM ESD stress condition, as shown in Table II. In addition, the positive and negative HBM stresses were performed separately on different samples.

For Ge EAMs, 4 key functional performances [2, 3] were studied; there being ideality factor, series resistance (*Rs*), extinction ratio (*ER*), and extracted wavelength (λ_{ER}). All were evaluated before and after the HBM stresses, and the corresponding results are shown in Figure 5 and Figure 6. No statistically significant change was seen in the ideality factor from unstressed condition to post-stress condition, as shown in Figure 5. However, the series resistance of the Ge EAM was seen to slightly increase after the 1st round of HBM ESD stress; yet a small decrease was then seen after the 2nd round of HBM ESD stress. This indicates that the changes were small and likely a result of measurement inaccuracy. It should also be noted that the optical performance of *ER* and λ_{ER} for the Ge EAMs were not impacted after the two rounds of HBM ESD stresses, as presented in Figure 6.

Table II: The HBM ESD stress conditions for the post HBM ESD electrical and optical funcational performance evaluations

	Ge EAM & Si RM	O&C -band PDs
1st Round	+100	+100
	-100	-100
2nd Round	+400	+400
	-110	-180

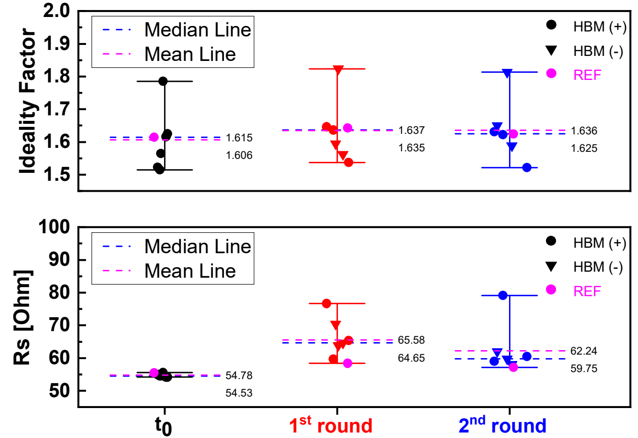

Figure 5: Measured electrical parameters of ideality factor and series resistance (*Rs*) for the Ge EAMs, respectively. t0 indicates fresh samples without any HBM stress. The HBM stress conditions for the two rounds of HBM stress are listed in Table II.

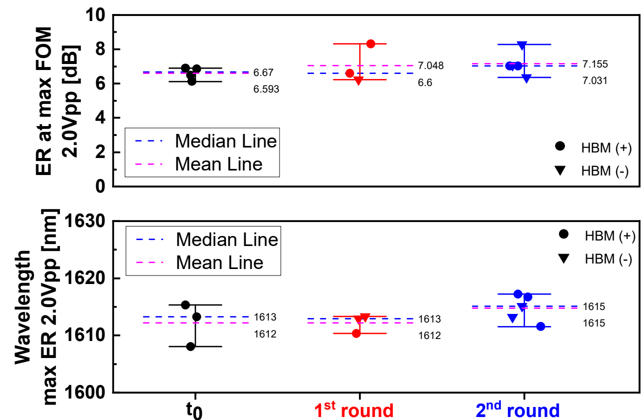

Figure 6: Measured optical parameters of extinction ratio (*ER*) and extracted wavelength (λ_{ER}) for the Ge EAMs, respectively. t0 indicates fresh samples without any HBM stress. The HBM stress conditions for the two rounds of HBM stress are listed in Table II.

Figure 7 and Figure 8 show the corresponding [3] evaluations of electrical and optical performance for the Si RMs before and after HBM stresses. No degradations of the quality factor (Q), the resonance wavelength (λ_{res}) and the modulation efficiencies of the two operating voltage ranges were observed after the two rounds of the HBM stresses. The median and mean values and even the variations of these electrical and optical parameters were not increased after the HBM stresses, as shown in Figure 7 and Figure 8.

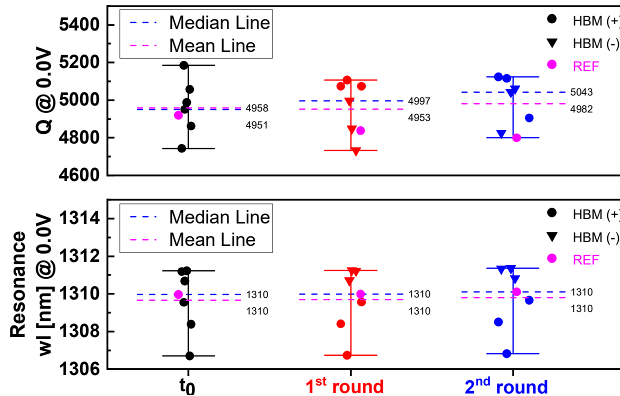

Figure 7: Measured optical parameters of quality factor (Q) and resonance wavelength (λ_{res}) for the Si RMs, respectively. t0 indicates fresh samples without any HBM stress. The HBM stress conditions for the two rounds of HBM stress are listed in Table II.

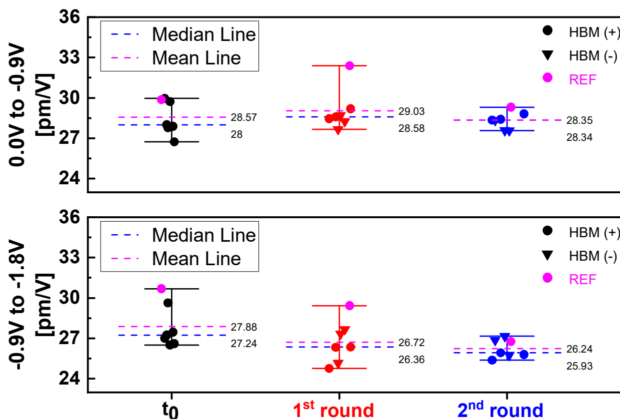

Figure 8: Measured optical parameters of modulation efficiencies from 0V to -0.9V and from -0.9V to 1.8V for the Si RMs, respectively. t0 indicates fresh samples without any HBM stress. The HBM stress conditions for the two rounds of HBM stress are listed in Table II.

Figure 9, 10, 11 show the key electrical and optical parameters for the O-band and C-band PDs before and after HBM stresses. The ideality factor and the series resistance (Rs) have no degradations after the two rounds of the HBM stress, as shown in Figure 9 and 10, respectively. In addition, the normalized responsivity at -1V did not show any degradation for the O-band and C-band PDs, as shown in Figure 11. After these post HBM ESD functional performance certifications, we can further conclude that these optical components all pass the required HBM ESD level of ±100V in the S20.20 Standard.

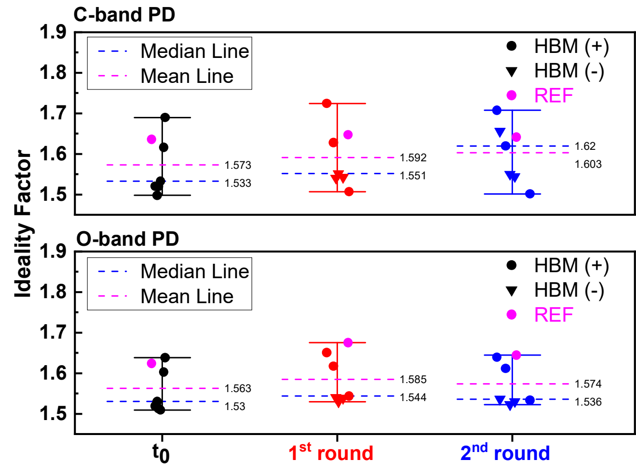

Figure 9: Measured electrical parameters of ideality factor for the C-band PDs and the O-band PDs, respectively. t0 indicates fresh samples without any HBM stress. The HBM stress conditions for the two rounds of HBM stress are listed in Table II.

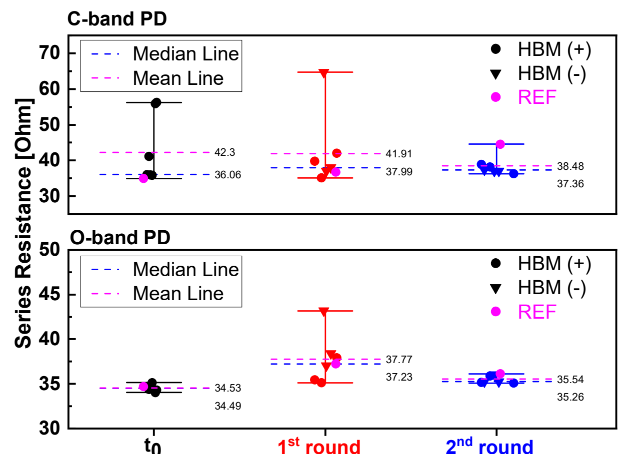

Figure 10: Measured electrical parameters of series resistance (Rs) for the C-band PDs and the O-band PDs, respectively. t0 indicates fresh samples without any HBM stress. The HBM stress conditions for the two rounds of HBM stress are listed in Table II.

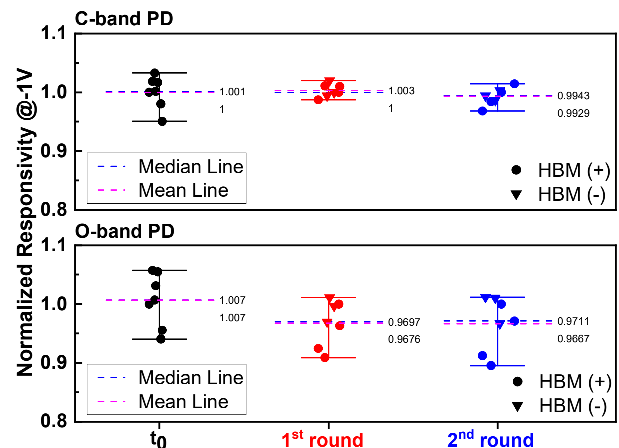

Figure 11: Measured optical parameters of normalized responsibility at -1V for the C-band PDs and the O-band PDs, respectively. t0 indicates fresh samples without any HBM stress. The HBM stress conditions for the two rounds of HBM stress are listed in Table II.

C. TLP IV Characteristics

To further understand the different failure mechanisms between these optical components, corresponding positive and negative 100ns TLP *IV* characteristics are shown in Figure 12(a) and (b), respectively. The expected forward and reverse diode behaviors can be observed in these TLP *IV* results. In Figure 12(a), the *Ron* values of the O- and C-band PDs are lower than those for the EAM due to their larger device sizes. However, the *Ron* of the Si RM is similar to those of the O- and C-band PDs at lower TLP stress current. For higher TLP current >150mA, the *Ron* significantly increases. This increased *Ron* could be attributed to the strong self-heating effect in a more compact layout style (with a worse thermal dissipation) for the Si RM. Conversely, the trend of the positive *It2* differences between these optical components seems to be consistent with the positive HBM results, as presented in Figure 3.

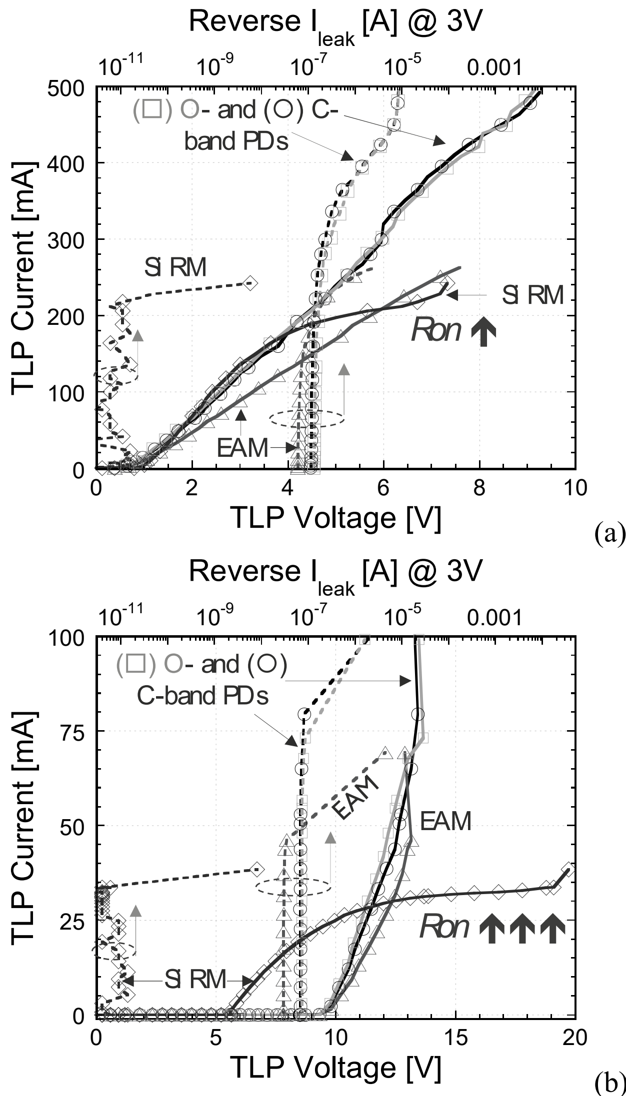

Figure 12: Measured (a) positive and (b) negative 100ns TLP *IV* characteristics of the Ge EAM, the Si RM, and the O-band and C-band Ge PDs.

In Figure 12(b), significant differences in the trigger voltages (*Vt1*) of the Si RM and the Ge based EAM or PDs are observed. In this case, a much stronger *Ron* increase can be observed in the Si RM when the TLP stress current is higher than 25mA. This results in a lower *It2* for the Si RM. In fact, the TLP *It2* of ~34mA is lower than the corresponding peak current (>60mA) of the negative 125V HBM stress level. This miscorrelation between TLP and HBM stress conditions can be related to the difference of the total stress energy in these two stress conditions. Due to a fixed rectangular 100ns pulse width for the TLP stress, its total stress energy can be higher than that of the HBM stress current with exponential decay during the whole stress duration. The higher stress energy can induce more pronounced self-heating effect and further result in the severe *Ron* increase, as observed in Figure 12(b). In general, these optical components with the SOI architecture can be more sensitive to self-heating effect under a high-current ESD stress duration.

D. CDM ESD

The CDM ESD robustness of the optical components was evaluated with dies in FGG400 BGA packages. For each die, both terminals of all the photonic devices were bonded out and the devices were CDM tested in ±25V voltage increments till failure in compliance with ANSI/ESDA/JEDEC JS-002. The same failure criteria and pre-/post-stress test methodology used for the HBM testing were applied to the CDM testing.

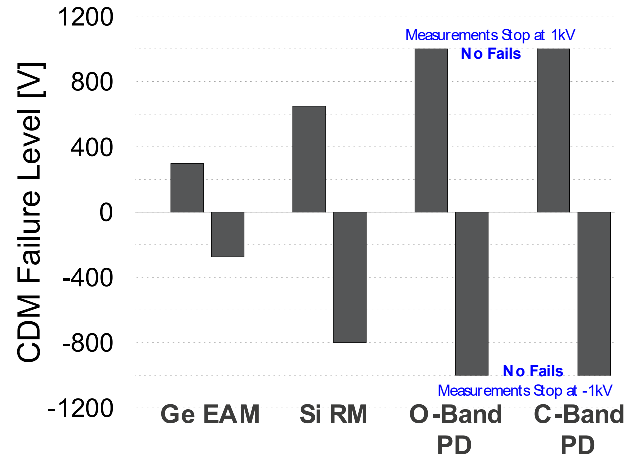

Figure 13: Measured CDM ESD failure levels of the Ge EAM, the Si RM, and the O- and C-band Ge photodetectors. Both Ge photodetectors pass ±1kV CDM (no evaluation was performed beyond ±1kV).

The CDM test results are shown in Figure 13, as follows:

i) As for the HBM testing, the photodetectors had higher ESD robustness than the modulators. In this case, the Ge EAM had significantly lower CDM robustness, as compared to the other devices,

including the Si RM. The Ge EAM failed at 300V and −275V, whereas the Si RM failed at 650V and −800V.

ii) The CDM robustness for all devices was approximately equal in the positive and negative stress directions, unlike the asymmetry seen in the HBM testing.

Unlike in the HBM events, where the ESD discharge path is between two terminals, the CDM discharge is a single terminal event triggered by the Pogo pin touching down on the package BGA. During positive CDM discharge, the positive charges of the device escape to GND via numerous distributed discharge paths coupled to the Pogo pin, whilst the negative charges of the device remain intact at the BOX interface, tied by the electric field of the CDM tester (see Figure 14). Once the CDM discharge is complete, the device will be at the ground potential of the Pogo pin: $V_{device} = 0$.

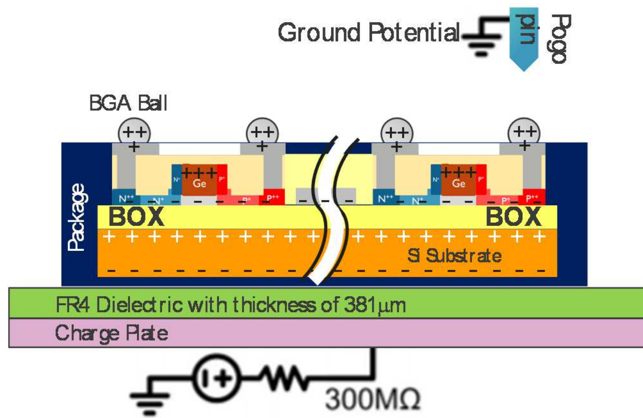

Figure 14: Illustration of positive CDM charge for the SOI device shown in Figure 2a. From the CDM point of view, the DUT is a series chain of capacitors, where the insulating BOX layer separates the conducting plates of the active device (the Si thin film and the Si substrate). During the follow-up CDM *discharge* event, the ground potential of the Pogo pin propagates to the BGA ball of the package, with a discharge impedance defined by the distributed BOX capacitors.

The electrical parameters of the discharge path are invariant of polarity of the CDM stress voltage, as they are mainly defined by the insulating BOX capacitors. The latter are invariant for ± CDM stresses. The observed symmetric CDM robustness agrees with this proposed discharge model. Where relative Ge-EAM weakness correlates with both presence of Ge epitaxy and the heater on the top. Furthermore, the only difference between CDM-weaker Ge-EAM and CDM stronger Ge photodetector is the heater in the Ge-EAM, as shown in Figure 15. The cross-section view in Figure 16 indicates the location of the heater structure.

A cross section failure analyses (FA) was done in an attempt to find a physical location for the CDM damage in the Ge-EAM. A fresh sample before CDM stress exhibited leakage of ~200nA. The leakage steadily increased with CDM stress voltage and at -500V reached ~2µA. Unfortunately, the FA did not reveal any conclusive damage for the sample with 2µA leakage current. To make the damage more pronounced, the CDM stress voltage was further doubled. This resulted in a post CDM stress leakage current of 53 µA and traces of visual discoloration at the Ge-EAM, as presented in Figure 15. The cross-sectional sample polishing towards the discoloration spot revealed granular Ge material at the damage location. The corresponding cross-sectional views are shown in Figure 16(a) and (b). These residues are indicative of the Ge melting followed by condensation into tiny droplets. A 6-second Buffered Oxide Etch (BOE) was performed on the sample of Figure 16(b). Figure 17 shows the result that the Si part of the Ge-EAM remained intact.

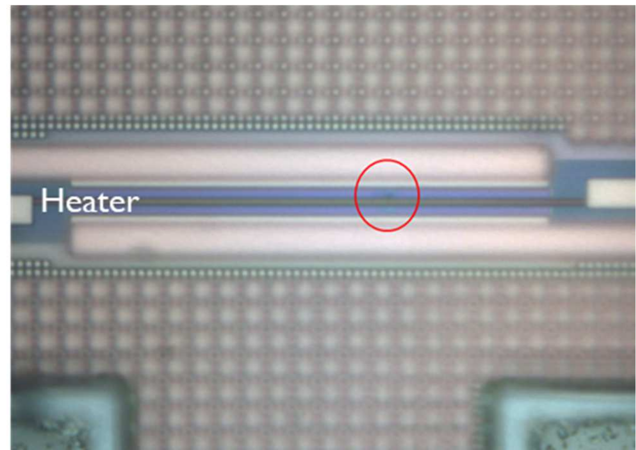

Figure 15: Optical microscope observation of the post CDM failure analysis and red-circled discoloration at the Ge-EAM. The structure of the Ge EAM is very similar to the Ge photodetectors, with the addition of a thermal tuning heater (required for tight control of the operating wavelength).

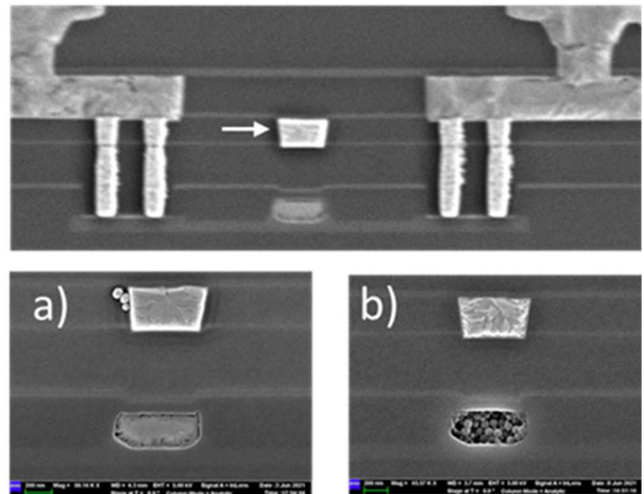

Figure 16: Cross-section view of the Ge EAM, where the arrow points to the heater. a) this zoom-in cross-section is away from the discoloration region, referred to in Figure 15, b) this zoom-in cross-section is at the discoloration region.

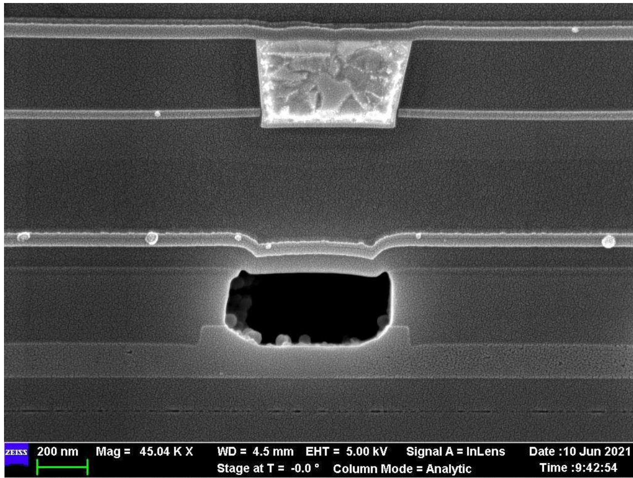

Figure 17: Buffered Oxide Etch (BOE) etch at the cross-section of the sample in Figure 16(b) shows intact Si at the damage location.

The Ge-EAM CDM result leads us to think that the presence of the floating heater facilitates CDM weakness as compared to the similar structure of the Ge-modulator without the heater. This could be attributed to electrostatic inductance. A TCAD simulation would be helpful to evaluate this hypothesis in future. It is clear that the placement of a floating heater should be avoided. Be reminded that the CDM robustness of the photonic devices studied in this work exceeds the S20.20 CDM level (±200V).

In reality, during 2.5/3D assembly, the ability of a bare die to accumulate tribo-electric charges should be related to the self-capacitance of the bare die [6] rather than to the package mutual capacitance (Cm). Since this is an order of magnitude lower than the Cm [6], it indicates that photonic devices in our work by far exceeded the S20.20 CDM requirements. In summary, our findings are as follows:

i) The HBM performance in reverse bias polarity is shown to be the limiting factor for such structures and is correlated to the optical diode width.
ii) The CDM performance of a structure with an unprotected heater is significantly weaker, as compared to structures without heaters.

IV. Conclusion

In this work, both HBM and CDM ESD robustness was evaluated for 4 types of optical I/O: Ge EAM, Si RM modulators, and O-band and C-band photodetectors. Our results show the self-protected ESD designs are adequate to meet with margin the ESD specifications of the S20.20 Standard (i.e. ±100V HBM and ±200V CDM). The results of key functional performance metrices after the HBM ESD stresses further confirm these optical components pass the required HBM ESD specification. In addition, the TLP *IV* characteristics indicate that the Si RM has the more pronounced self-heating effect which results in an unexpected lower *It2* under the negative stress. Finally, the heater was found to be the weakest CDM ESD element of Si-Photonics and therefore may require dedicated ESD protection.

References

[1] P. Absil, K. Croes, A. Lesniewska, P. De Heyn, Y. Ben, B. Snyder, J. De Coster, F. Fodor, V. Simons, S. Balakrishnan, G. Lepage, N. Golshani, S. Lardenois, S. A. Srinivasan, H. Chen, W. Vanherle, R. Loo, R. Boufadil, M. Detalle, A. Miller, P. Verheyen, M. Pantouvaki, and J. Van Campenhout, “Reliable 50Gb/s Silicon photonics platform for next-generation data center optical interconnects,” in *Dig. of IEDM*, 2017, pp. 761-764.

[2] S. A. Srinivasan, M. Pantouvaki, S. Gupta, H.-T. Chen, P. Verheyen, G. Lepage, G. Roelkens, K. Saraswat, D. Van Thourhout, P. Absil, J. Campenhout, “56 Gb/s Germanium Waveguide Electro-Absorption Modulator, *IEEE Journal of Lightwave Technology*, vol. 34, no. 2, pp. 419-424, 2016.

[3] Y. Ban, J. Verbist, M. Vanhoecke, J. Bauwelinck, P. Verheyen, S. Lardenois, M. Pantouvaki, J. Van Campenhout, “Low-Voltage 60Gb/s NRZ and 100Gb/s PAM4 O-band Silicon Ring Modulator,” in *IEEE Optical Interconnects Conference*, 2019, pp. 1-2.

[4] R. Boschke, S.-H. Chen, G. Hellings, M. Scholz, P. De Heyn, P. Verheyen, J. V. Campenhout, D. Linten, A. Thean, and G. Groeseneken, “Bidirectional NPN ESD protection in Silicon photonics technology,” in *Proc. of IRPS*, 2016, pp. 3B.5-1.

[5] ANSI/ESD S20.20-2014, American National Standard.

[6] J. Karp, M. Hart, M. Fakhruddin, C. Kireev, P. Tan, D. Tsaggaris, and M. Rawat, “Interposer FPGA with self-protecting ESD design for inter-die interfaces and its CDM specification,” in *Proc. of IRPS*, 2016, pp. 6A.2.