Wafer-Level LICCDM Device Testing

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Abstract – With the integrated circuit technology evolution towards 2.5D and 3D stacking, wafer-level and bare-die-level electrostatic discharge testing is becoming a necessity. In this work, we use our Low-Impedance Contact CDM tester to measure integrated circuit products and assess the possibilities and potential issues of CDM testing of wafers and bare dies.

I. Introduction

The LICCDM (low-impedance contact charged device model) electrostatic discharge (ESD) tester is an alternative to the industry standard field-induced CDM (FI-CDM) tester for sub-150 V CDM testing. LICCDM solves the variability issues caused mainly by the air discharge observed in the FI-CDM tester [1]–[3]. It also enables wafer-level and bare die testing using commercially available wafer probe stations. Wafer-level ESD testing is interesting because in the system technology co-optimization (STCO) integrated circuit scaling era, wafers and bare dies become products for further (sub-)system co-integrations. It must be mentioned that setups as the capacitively-coupled transmission line pulser (CC-TLP) [4]–[6] and the wafer-level CDM 2 [7] testers enable wafer-level CDM measurements. However, the output impedance of these systems is 50 Ω, while 16.7 Ω has been discussed as a better choice [2], [8], [9].

In this work, as a continuation to our previous publications on LICCDM, [3], [10], we use our in-house LICCDM setup to measure two different application-specific integrated circuit (ASIC) products on wafers and bare dies. The goal of this work is to assess if LICCDM testing on wafers or bare dies is practical and to find the potential issues. Here, for the first time we test integrated circuit products, while our previous work focused solely on verification modules.

Section II describes the setup in more detail and provides the verification measurement results. Section III presents and discusses the ASIC measurement results. Finally, the conclusions are given Section IV.

II. Measurement setups

The measurement setup used for this work consists of the Hanwa HED-T5000 VF-TLP (very fast transmission line pulser), the Tektronix MSO72304DX oscilloscope with 100 GS/s sampling rate and 23 GHz bandwidth, two Keithley 2602B source-measure units, the Tektronix TTR 506A Vector Network Analyzer (VNA) with 100 kHz to 6 GHz bandwidth and the MPI TS3000 automated 300 mm probing system with a triaxial RF wafer chuck. Except for the LICCDM probe, which is described in subsection A, we also used the MPI kelvin probes for DC measurements.

A. LICCDM measurement setup

The LICCDM probe is slightly different from the one presented in [10]. It has an aluminum ground plane with a 5 mm long and 1.5 mm wide peephole, instead of 9 mm × 5.5 mm. Also, the redesigned PCB supporting the probe needle (Figures Figure 1, Figure 2 and Figure 3) has shorter transmission lines. The ground plane is square with 63.5 mm long sides, as specified by the JS-002 CDM standard [11]. Compared to undefined values in [10], the distance of the probe needle tip to the bottom side of the ground plane has been fixed to exactly 0.5 mm. This is similar to the CC-TLP measurement setup [4]. In all experiments presented in this paper, the wafer chuck has been grounded. We used seven verification modules for benchmarking the LICCDM tester. Their sizes are given in Table 1.

The mode of operation of the LICCDM setup is as follows. A VF-TLP or TLP is used as a pulse source. The TLP pulse travels to the LICCDM probe where it encounters a signal junction towards the tested device,

a 50 Ω termination and a 50 Ω transmission line towards the oscilloscope. Therefore, the oscilloscope always triggers on the VF-TLP/TLP pulse regardless of the device under test (DUT). Finally, the current through the DUT is calculated from the difference between the incident (open contact) V_{inc} and transmitted (in contact with DUT) V_{trans} voltage waveforms, divided by the system impedance:

$$I_{DUT} = \frac{3}{50}\left(V_{inc} - V_{trans}\right) \tag{1}$$

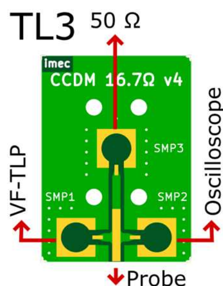

Figure 1 – Schematic of the PCB contains three surface-mounted SMP connectors to connect the VF-TLP, the oscilloscope and the 50 Ω termination. The distance from the coplanar waveguides crossing to the probe needle is 3.0 mm, hence the name TL3.

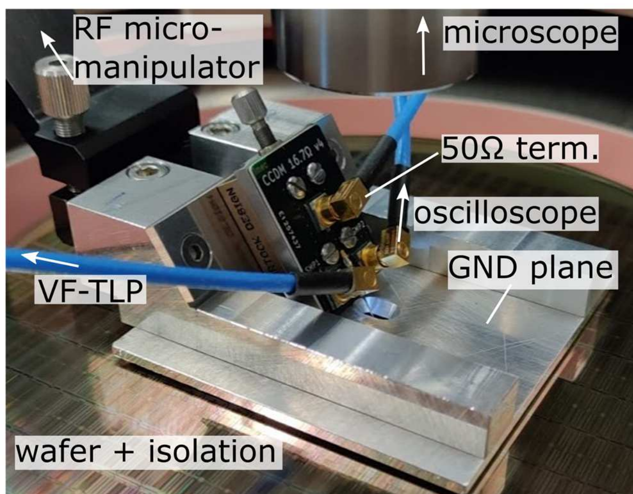

Figure 2 - Photo of the LICCDM setup including the PCB, aluminum ground plane, a 150 mm wafer and the 0.381 mm thick FR4 to insulate the wafer from the chuck underneath. The peephole in the middle of the ground plane is used both for the LICCDM probe needle and as the microscope line of vision.

Table 1 - Set of 7 brass verification modules with names and diameters. The two modules defined in the JS-002 standard [11] use the naming convention from the standard itself. This table is duplicated from [10] for convenience.

Module	***d* [mm]**	**Module**	***d* [mm]**
P1	2.3	JS-002 large	25.4
P2	4.6	P6	35.5
JS-002 small	8.89	P7	41.8
P4	18.2		

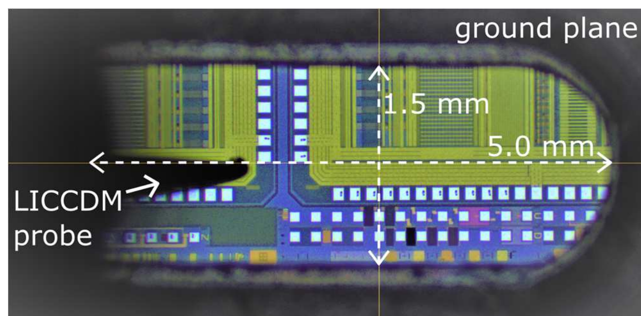

Figure 3 – Microphotograph of the LICCDM ground plane peephole. The probe needle can be seen as a shadow on the left side. The peephole is large enough to observe the wafer/bare dies underneath the LICCDM ground plane. On the contrary, it could be made even smaller as long as the probe needle does not touch the ground plane.

The LICCDM setup used in this paper produces a secondary peak, or pulse tail offset, after the primary peak. This tail offset is not observed in small modules, but only in the JS-002 large verification module and larger, as can be seen in Figure 4. The amplitude of this secondary peak is 40% of the primary peak current in the worst case for the P7 module.

Compared to our previous setups ([3], [10]) where a tail offset with multiple ripples was observed instead of a clear secondary peak, the verification waveforms I_{dut} in this setup have a more pronounced secondary peak. From our previous learnings, this secondary peak is caused by the parasitic coupling to the wafer prober. By modeling our LICCDM setup using the Keysight ADS software, we can confirm that the pulse tail disappears when the wafer prober parasitic impedances and reactances are removed. This model has been previously described in [10] and, with minor modifications to the lumped components values, is still valid for the MPI TS3000 wafer prober.

Figure 5 depicts the extracted peak currents I_{peak} for all seven verification modules for VF-TLP pre-charge voltages $V_{VF\text{-}TLP}$ ranging from 5 to 500 V. I_{peak} increases monotonically with V_{TLP} for all modules except P1 and P2 where the measurement noise is more evident.

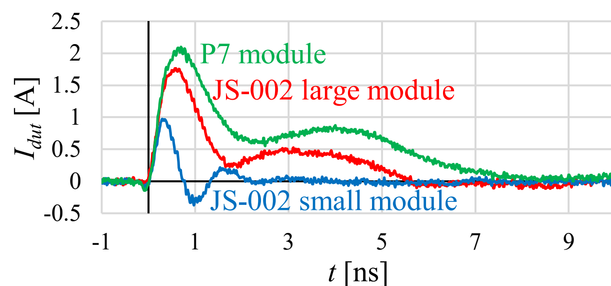

Figure 4 – LICCDM waveforms measured with verification modules using a 100 V VF-TLP pulse, 0.381 mm thick FR4 dielectric and the ground plane height of 0.5 mm. A secondary peak is observed for the large JS-002 and P7 modules. The secondary peak is not present for smaller coins.

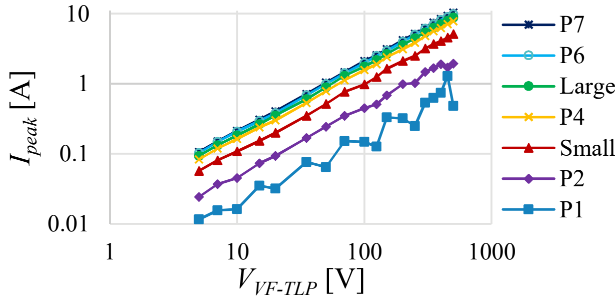

Figure 5 - Extracted peak currents for all verification modules increase monotonically with the VF-TLP pulse amplitude $V_{VF\text{-}TLP}$. The smallest modules P1 and P2 have a very low capacitance towards the LICCDM tester setup. Therefore, the applied VF-TLP pulse creates a limited displacement current flow through these coins, with the peak values comparable to the setup noise level and hence the non-monotonic relation with $V_{VF\text{-}TLP}$.

B. Capacitance measurement setup

Since the LICCDM pulse is defined by the device-under-test (DUT) capacitance towards the tester, this capacitance is sometimes interesting to measure. Since the total DUT capacitance C_{dut} in our wafer-level LICCDM tester has two main components, the capacitance measurement is not trivial. The two capacitive components are, firstly, the capacitance from the DUT towards the wafer chuck below, C_c, and secondly, towards the ground plane above C_g. Therefore, to accurately measure the total DUT capacitance C_{dut}, we must use the same LICCDM probe, as depicted in Figure 6.

As a sanity check, the C_{dut} results for all seven verification modules are extracted from the measured *S11* scattering parameters and depicted in Figure 7 as a function of frequency. Furthermore, the C_{dut} values at 1 MHz are extracted and given in Table 2.

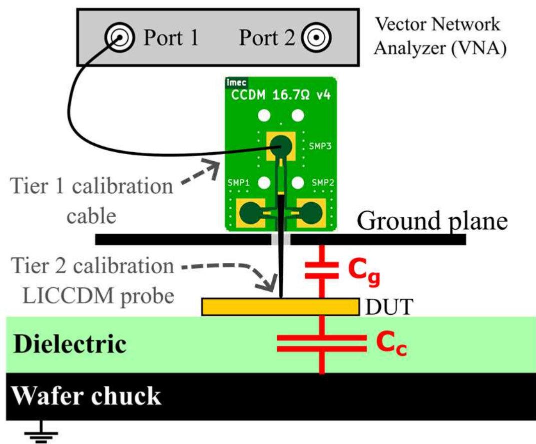

Figure 6 – The capacitance measurement setup using a vector network analyzer (VNA) connected through the LICCDM probe. A two-tier calibration is needed to decouple the unwanted cable and LICCDM probe impact [12]. This setup can capture the total DUT capacitance C_{dut} consisting of the capacitance towards the wafer chuck below C_c and towards the ground plane above C_g.

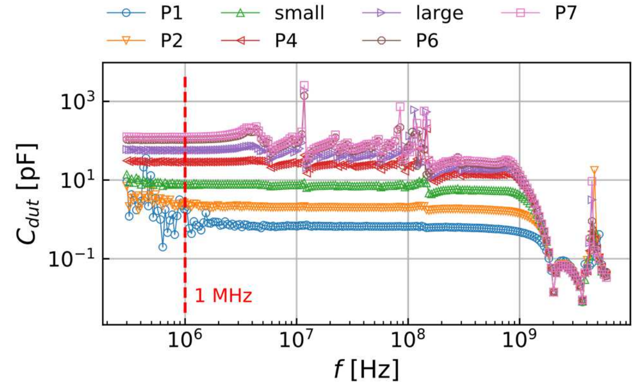

Figure 7 – The total DUT capacitance C_{dut} of all 7 verification modules as a function of frequency f. As expected, the smallest module P1 has the smallest capacitance. Large modules, including P4, have not only larger capacitance values but also show a more complex frequency-dependent behavior in the frequency range from ~10 to 200 MHz. The resonant frequency is found at about 2 GHz where the system reactance shifts from a capacitive to a more inductive behavior.

Table 2 – DUT capacitances C_{dut} extracted from Figure 7 at the frequency value equal to 1 MHz. The values of the small and large JS-002 modules are very close to the values defined in the standard, 6.8 and 55.0 pF, respectively.

Module	C_{dut} [pF]	Module	C_{dut} [pF]
P1	1.27	JS-002 large	57.19
P2	2.30	P6	105.92
JS-002 small	7.85	P7	123.70
P4	28.65		

C. Resistance measurement setup

To further understand our LICCDM measurement results, we have also measured the DUT resistances to neighboring dies and to the wafer substrate. For this we used DC kelvin probes to achieve a kelvin measurement setup, sometimes also called a 4-point resistance measurement setup, to reduce errors from cable resistance. However, in our probes the force and sense channels connect just before the probe needle, so the needle and contact resistances are reported as part of the total device resistance.

III. Wafer-level ASIC measurements and discussion

Two different ASIC designs have been tested (Table 3) and the measurement results from two experiments are presented here. We used a whole wafer from ASIC *I* to experiment how testing a die in the center compares to a die close to the edge of the wafer. The second experiment is on a cut wafer from ASIC *U* to test how the wafer piece size affects the LICCDM measurements.

The following data does not include information about CDM failure levels. The reason for this is that LICCDM is a single probe tester while at least two probes are needed for DC measurements. Consequently, the DUT needs to move from the LICCDM to the DC setup and back after every zap, which can be technically challenging to automate. Therefore, in this paper we focus on the transient LICCDM waveforms and the extracted peak currents.

Table 3 - Summary of the tested ASIC products characteristics.

ASIC	***I***	***U***
Tech. node	0.35 µm 3.3 V CMOS	55 nm 1.2 V CMOS
Wafer size	150 mm (6 inch)	300 mm (12 inch)
Die size	10.0×4.25 mm^2	5.1×5.1 mm^2
Samples	Whole wafer	Wafer pieces
ESD protection	IO ring	IO ring

A. Whole wafer – ASIC *I*

Two experiments have been conducted for this section: firstly, to test the effect of the die position relative to the wafer and wafer chuck, and secondly, to test the influence of the dielectric on the LICCDM results.

Figure 8 depicts the ASIC *I* wafer relative to the wafer chuck and LICCDM ground plane. The measured dies are highlighted in red. These dies were chosen as the three extreme examples an LICCDM wafer measurement could encounter. Firstly, the ground plane for the center die is fully over the wafer, secondly, for the top die half over the wafer and half over the chuck, and thirdly, for the bottom die half over the wafer and half over nothing. Figure 9 depicts the die map and the measured pins are highlighted in red.

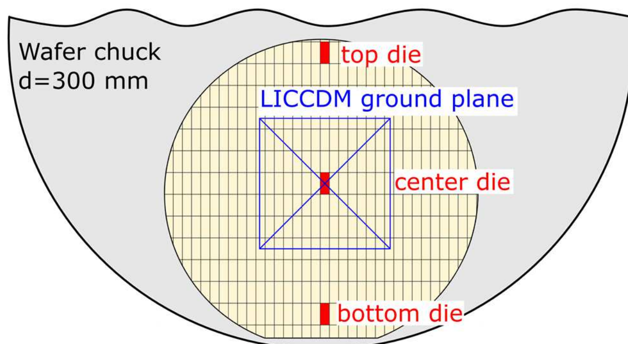

Figure 8 – Position of the ASIC *I* wafer (yellow circle) on the partially depicted wafer chuck (grey semi-circle) and the LICCDM ground plane (crossed blue rectangle), all to scale. The three measured dies are highlighted in red.

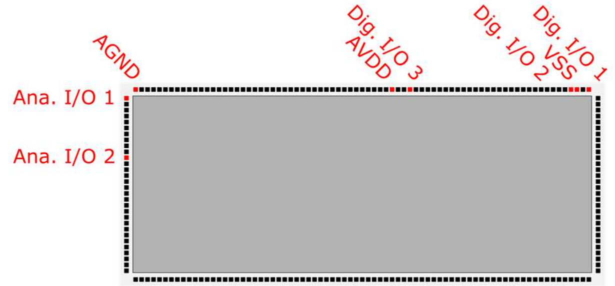

Figure 9 – Die map with measured pins highlighted in red where *Dig. I/O* stand for a digital input/out pin and *Ana. I/O* for the analog input/output pin. *VSS* is the general ground, *AVDD* is the analog power supply and *AGND* is the analog ground pin.

No major differences have been observed when measuring the different pins, Therefore, Figure 10 depicts the waveforms from only two pins in the three measured dies. For both examples, *Dig. I/O* and *AVDD*, the location of the die within the wafer and its position relative to the wafer chuck do not seem to make a significant difference. For reference, the extracted peak currents I_{peak} for all measured pins and dies are depicted in Figure 11, with the worst-case relative difference between the center and bottom die in Figure 12.

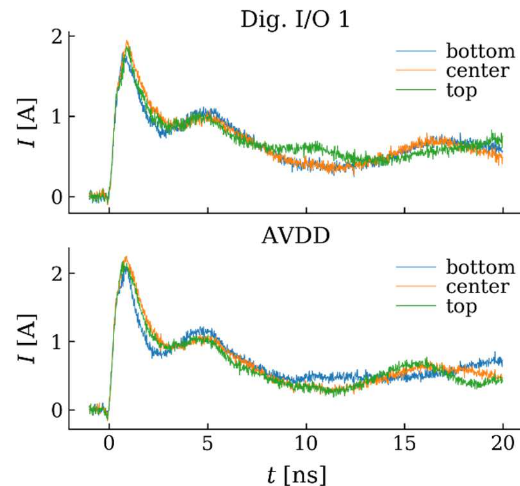

Figure 10 – LICCDM current waveforms for the *Dig. I/O* and *AVDD* pins from all three measured dies do not show significant differences in the primary pulse peak nor in the tail offset. $V_{VF\text{-}TLP} = 100$ V.

Interestingly, removing the FR4 dielectric and placing the wafer directly onto the wafer chuck also does not seem to be significant (Figure 13). To explain this, we measured the die-to-die resistance by contacting the same ground pin on two neighboring dies 4.25 mm away and found it is in the range of 4.0 Ω (probe contact resistance included). The vertical resistance, from the ground pin to the back of the wafer is about 60 Ω. Indeed, with such a low substrate resistance the neighboring dies greatly impact the total capacitance of the measured die, as depicted in Figure 14.

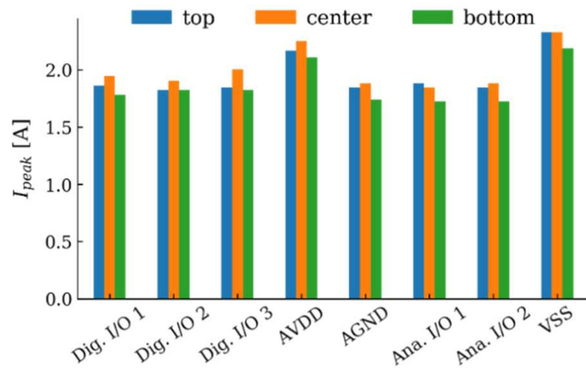

Figure 11 – The extracted peak currents from all measured pins and top/center/bottom dies confirm that the wafer and chuck locations have only a minor impact on the measurement results. $V_{VF\text{-}TLP}$ = 100 V.

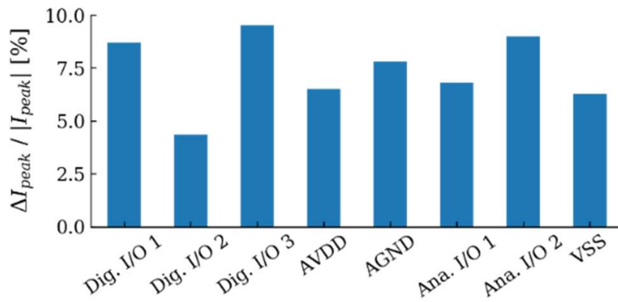

Figure 12 – The worst-case relative differences of the peak currents from Figure 11 are between the center and bottom die. Nevertheless, the maximum difference is smaller than 10%.

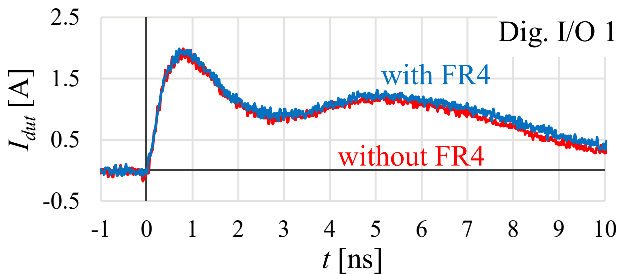

Figure 13 – No significant differences in the LICCDM waveform are observed when zapping the wafer center die with or without the FR4 dielectric underneath it. $V_{VF\text{-}TLP}$ = 100 V.

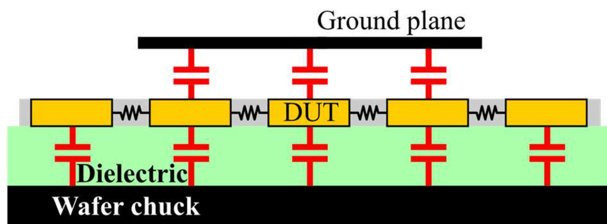

Figure 14 – Wafer with multiple dies can increase the capacitance of the DUT given that there is a capacitive or resistive path between the neighboring dies.

No matter if the dielectric is used to insulate the DUT from the chuck or not, the capacitance of this specific wafer is so large that the 1-ns LICCDM pulse sees it as a short towards the ground. Removing the FR4 dielectric creates an ohmic contact to the chuck of about 60 Ω in parallel with the large capacitance. This again acts like a short for the main LICCDM pulse peak. This explains why there is no significant difference in the LICCDM peak current for both experiments with and without dielectric. Basically, measuring a whole wafer is, in this case, like measuring the wafer chuck itself. Both the peak current and the tail offset are at their plateau values regardless of the dielectric underneath the wafer. Of course, this might change for a different technology in which the dies are electrically better isolated between each other and towards the backside.

B. Wafer cuts – ASIC *U*

Two experiments have been conducted for this section: firstly, to test the effect of the wafer piece size, and secondly, to test the influence of the dielectric on the LICCDM measurements. Except for the FR4 dielectric, this time we also used the dicing tape as dielectric.

While the 0.381 mm thick FR4 is the standardized dielectric for FI-CDM measurements, it is not practical for use in wafer-level measurements to insulate the metallic wafer chuck from the DUT. Except if custom made, the main reason against the FR4 dielectric is that it does not allow applying vacuum on the wafer and even more so on the bare die samples. Therefore, it is difficult to hold the bare die in place during measurements. On the other hand, the dicing tape is fabricated for use in the cleanroom and wafer handling. Even though several different types exist, it is usually electrically insulating. Most importantly, it is sticky on one side, so no matter the bare die size, it will hold it in place without leaving any glue residue when removed.

Figure 15 depicts the different wafer pieces and bare dies used for the measurements presented in this section. The large wafer piece *Wcut-1* is larger than the LICCDM ground plane while the small *Wcut-2* piece is smaller. Single bare dies have also been used. Figure 16 depicts the die map highlighting the measured pins.

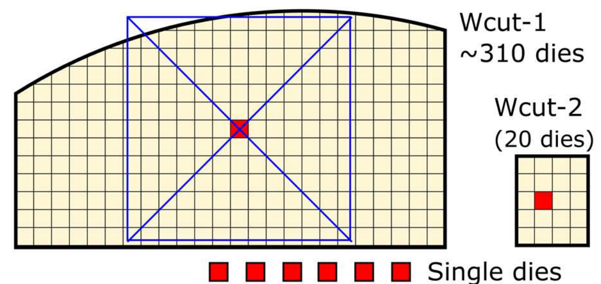

Figure 15 – The ASIC *U* large *Wcut-1* piece containing about 310 single dies, the small *Wcut-2* wafer piece containing 20 dies and single bare dies. Measured dies are highlighted in red. The blue crossed rectangle represents the LICCDM ground plane. The dies, wafer pieces and the LICCDM ground plane are drawn to scale.

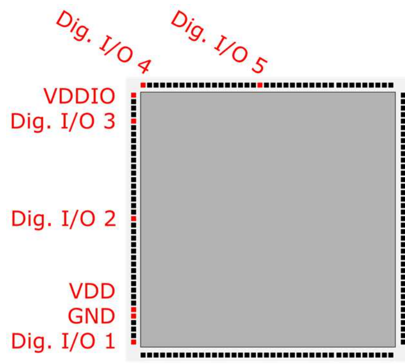

Figure 16 – ASIC *U* die map with measured pins highlighted in red. *Dig. I/O* stand for the digital input/output pin. *GND* is the ground pin, *VDD* is the power supply pin and *VDDIO* is the I/O ring power supply pin.

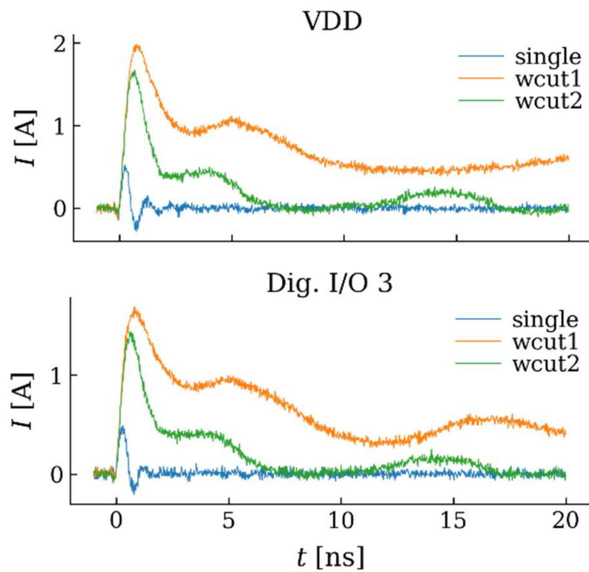

Figure 17 – LICCDM current waveforms from ASIC U *Wcut-1*, *Wcut-2* and a single die with the FR4 dielectric underneath the sample. The trend is equal both for the *VDD* and the *Dig. I/O 3* pins – the single die has a significantly smaller peak current and no tail offset compared to the wafer pieces.

1. LICCDM measurement results

As published before in [13], it is expected that wafers have significantly higher FI-CDM peak currents than single dies. Our experiment confirms this behavior, as can be seen in Figure 17, regardless of the tested pin.

Opposite to the results in subsection A with a full wafer, the use of a dielectric to insulate the smaller wafer pieces from the conductive wafer chuck is more important. Firstly, the tails offset can be drastically reduced by using the dielectric, as depicted in Figure 18. A summary of the peak currents and tail offsets of the *Dig. I/O 3* pin for different wafer piece sizes and dielectrics are depicted in Figure 19 and Figure 20. From this it is clear that the use of a dielectric is critical for the single dies and small wafer pieces, as their peak currents and tail offsets can be strongly affected by it. The dicing tape, being thinner than the FR4 dielectric, results in slightly higher peak currents.

These results hint that the number of neighboring dies in the same wafer piece has a significant effect on the LICCDM pulse shape. Even though the dies in a wafer are separated by scribe lines, they are not always electrically isolated, at least not in the products we tested and presented in this paper. They do share the same substrate which can be conductive. As mentioned before, this might not be true for a different technology with a more electrically resistive substrate.

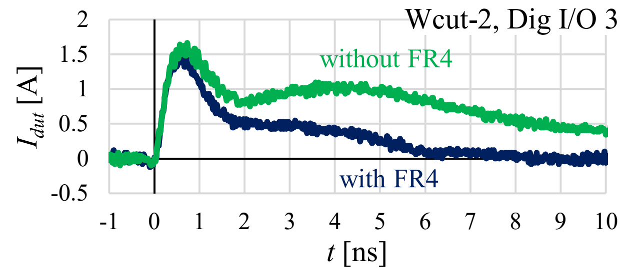

Figure 18 – Using FR4 to insulate the DUT from the chuck can reduce the pulse tail offset. Like for ASIC *I* in subsection A, this effect is not present for Wcut-1 (not shown). $V_{VF\text{-}TLP}$ = 100 V.

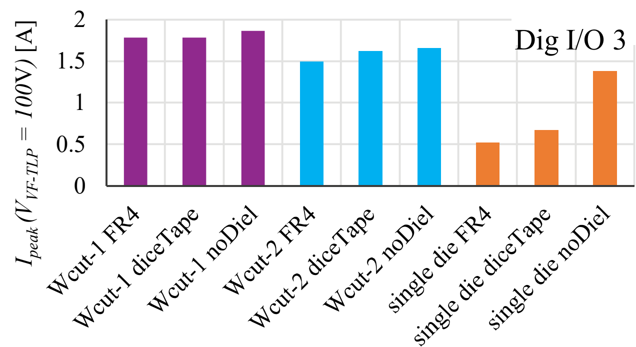

Figure 19 – Peak current I_{peak} data from different samples, from *Wcut-1*, from *Wcut-2* and single dies, all with FR4 or dicing tape as dielectric, or without dielectric. The dielectric has the most significant impact on I_{peak} from the single die.

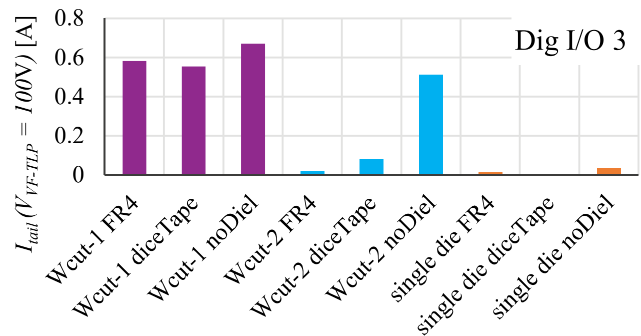

Figure 20 – The pulse tail offset current I_{tail} extracted from waveforms by averaging all points between 7 and 10 ns. I_{tail} reduces with the size of the wafer piece and even more so with insulating the DUT from the chuck with a dielectric.

2. Capacitance measurement results

To better understand the LICCDM test results, we measured the DUT capacitance C_{dut} as depicted in Figure 6. The results for the measured pins in *Wcut-1*, *Wcut-2* and single dies are presented in Figure 21.

As could be expected from the LICCDM test results, the capacitance is strongly correlated with the wafer piece size, at least for the ground and power supply pins. Obviously, the signal pins are well insulated from the power networks and therefore also from neighboring dies.

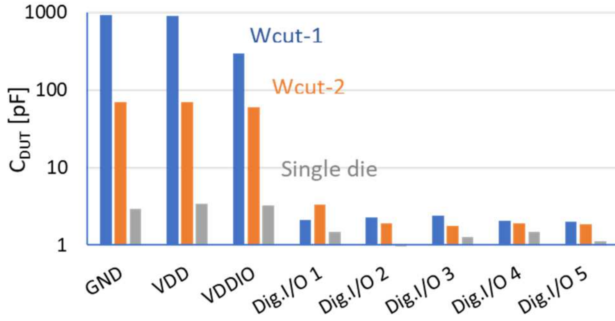

Figure 21 – DUT capacitance C_{dut} extracted from the S11 scattering parameter for samples in *Wcut-1*, *Wcut-2* and single dies insulated by the FR4 dielectric from the wafer chuck. C_{dut} shows a strong correlation with the wafer piece size and spans over three decades for the power supply and ground pins. Dig. I/O are not affected by the wafer piece size since they are insulated from the substrate.

Reflecting on the LICCDM test results Figure 19, the *Dig. I/O 3* peak currents are affected by the wafer piece size more strongly than what the measured capacitance values show in Figure 21. In the experiments on *Dig. I/O 3* with FR4 the *Wcut-1* peak current is about 3.5 times larger than for the single die (Figure 19). The DUT capacitance C_{dut} ratio is 1.8 for the same experiment in Figure 21. There is a twofold explanation to this mismatch between the C_{dut} and I_{peak}. Firstly, the LICCDM test is a large signal measurement that can trigger the ESD protection circuits and therefore temporarily create a low-ohmic connection from the *Dig. I/O* pins to the power distribution networks. Also, the central frequency of the main LICCDM pulse is about 1 GHz (= 1/(1 ns)). Furthermore, I_{peak} can plateau for very large wafer samples, as already explained in Section III.A. Secondly, the VNA uses a small signal measurement technique which cannot activate the ESD protection circuits. Therefore, the *Dig. I/O* remains insulated from the power supply networks. Also, the reported DUT capacitance is measured at 1 MHz. To conclude, it is not straightforward to compare the LICCD I_{peak} currents (Figure 19) to C_{dut} capacitance measurements (Figure 21).

The capacitance difference for the power supply pins can only mean that they are well connected to the neighboring dies. To check is that is true, we calculate the wafer total piece capacitance C_{dut} using the parallel-plate capacitor formula:

$$C_{dut} = \varepsilon_0 \varepsilon_{FR4} \frac{A_{dut}}{d_{FR4}} + \varepsilon_0 \frac{A_{dut}}{h_{gnd-plane}} \quad (2)$$

where ε_0 is the vacuum permittivity and equal to 8.854×10^{-12} C/Vm. ε_{FR4} is the FR4 relative permittivity equal to 4. d_{FR4} is the FR4 dielectric thickness equal to 0.381 mm. $h_{gnd\text{-}plane}$ is the distance from the DUT to the LICCDM ground plane and equal to 0.5 mm. Finally, A_{DUT} is the DUT area, given in Table 4 for the different wafer pieces. The calculated C_{dut} has an excellent match with the measured values, as depicted in Figure 22. This confirms that a wafer piece or a whole wafer can act as a very large single device during LICCDM testing. Therefore, the LICCDM peak current is significantly higher for a wafer than for a single die.

Table 4 – Areas of the measured ASIC *U* wafer pieces.

	A [mm²]
Single die	26.01
Wcut-2 (20 single dies)	520.20
Wcut-1 (~310 single dies)	8,063.10

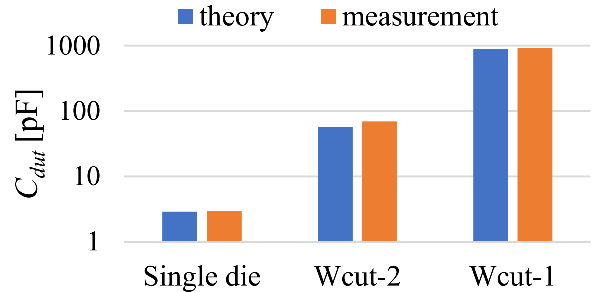

Figure 22 – The DUT capacitance C_{dut} (equal to $C_g + C_c$ from Figure 6) calculated with the parallel-plate capacitor formula matches excellently with the measured C_{dut} for the *GND* pin.

3. Resistance measurement results

As a final confirmation that several dies on a wafer can act as a single device during LICCDM measurements, we measured the resistances of the *GND* pins between neighboring dies and also between the die and the chuck. Indeed, the die-to-die resistance for ASIC *U* is very low, 14 Ω. The die-to-chuck resistance was measured to be 1 MΩ. Figure 23 depicts a cross section of two neighboring dies on a wafer. Indeed, the die-to-die resistance of only 14 Ω explains that during LICCDM testing we are measuring the capacitance of multiple dies in parallel and not a single die, same as in subsection A for ASIC *I*.

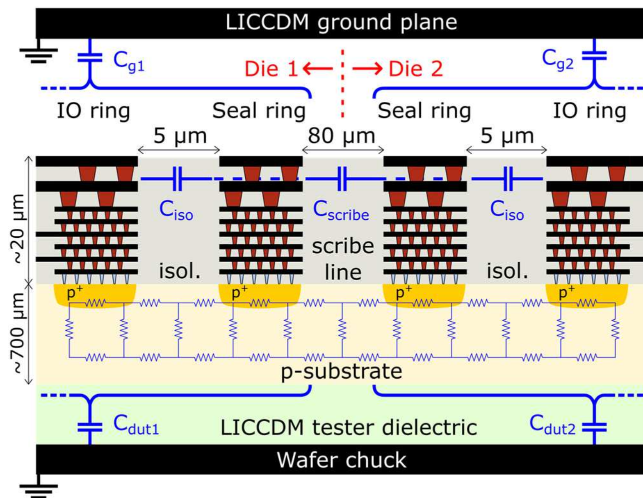

Figure 23 – Drawing of the assumed cross section between two dies on a wafer. The die IO ring is connected to the substrate via the ground network. The seal ring which protects the die during dicing is also connected to the substrate. The distance between the two dies IO rings is about 100 µm. If the substrate can create a low-ohmic connection from one die to the next, it is easy to imagine how the total capacitance of a die is significantly increased when on a wafer.

IV. Conclusions

The wafer-level low-impedance contact CDM (LICCDM) tester was successfully used for testing devices on whole and diced wafers. Wafer pieces of different sizes can influence the measured peak current – larger pieces can give higher peak currents because of a strong coupling to neighboring devices through the substrate. Since the peak current seems to plateau at a certain device size, removing the dielectric underneath the measured wafer has, in our case, an insignificant impact. However, using a dielectric is critical when testing smaller wafer pieces or single dies. Therefore, as a rule of thumb, a dielectric to insulate the wafer from the wafer chuck should always be used for wafer-level LICCDM testing.

A significant difference between the single die and wafer LICCDM measurements has been observed. Nevertheless, this is not a concern if the product is tested in the same format as shipped – a full wafer or single dies. However, it is useful to understand that an integrated circuit products might be more susceptible to CDM ESD damage while in a whole wafer since their capacitance could be increased for several orders of magnitude compared to that of a single die.

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