System Optimization: High-Frequency Buck Converter With 3-D In-Package Air-Core Inductor

Hesheng Lin, *Graduate Student Member, IEEE*, Geert Van der Plas, *Member, IEEE*, Xiao Sun, *Member, IEEE*, Dimitrios Velenis, *Member, IEEE*, Eric Beyne, *Senior Member, IEEE*, and Rudy Lauwereins, *Fellow, IEEE*

***Abstract*— In this work, we present the analytical model of buck converter with 3-D in-package air-core inductor (150 μm thick). To optimize the power efficiency at a targeted power density, models including 3-D inductor and power switches are developed. Compared to 3-D electromagnetic (EM) simulation, the proposed inductor model has a modeling error within 12% for the inductance calculation. With the proposed design methodology, an inductor with Q-factor up to 35 at 300 MHz is achieved. From the system aspect, the loss breakdown in the integrated power converter is investigated. A 0.5 ratio buck converter can reach 88.5% efficiency at 1–5 W/mm^2 based on the optimized inductor designs, with output voltage ranging from 0.7 to 0.9 V and based on 28 nm CMOS.**

***Index Terms*— Air-core inductor, buck converter, design methodology, efficiency optimization, in-package, system integration.**

I. Introduction

NOWADAYS fully-integrated voltage regulators (FIVRs) are widely used in high-performance computing (HPC) systems like laptops, servers, and graphics products, which normally need 45–300 W supply power [1]–[3]. For laptop customers, their first concern is the battery life, and the market consistently moves to thinner and lighter form factors for more portable applications [1]. For instance, the overall thickness (logic die + package) of the microprocessor in the extremely thin laptops and tablets is limited to 1.05 mm [4]. This calls for the FIVRs with high efficiency and thinner package thickness. In order to make the FIVRs much smaller and more energy-efficient, breakthroughs of passive components are required. Taking buck converter as an example, its inductor should be capable of storing high power density (>1 W/mm^2), while keeping small parasitics for ~90% circuit efficiency η to meet the system requirement.

Manuscript received April 30, 2021; revised July 25, 2021; accepted July 31, 2021. Date of publication August 5, 2021; date of current version March 28, 2022. A preliminary version of this article was published in Proceedings of 8th Electronic System-Integration Technology Conference (ESTC), pp. 1–6, Vestfold, Norway, September 2020. Recommended for publication by Associate Editor O. Pop upon evaluation of reviewers' comments.
(Corresponding author: Hesheng Lin.)

Hesheng Lin and Rudy Lauwereins are with imec, 3001 Leuven, Belgium, and also with the Department of Electrical Engineering, KU Leuven, 3000 Leuven, Belgium (e-mail: hesheng.lin@imec.be; rudy.lauwereins@imec.be).

Geert Van der Plas, Xiao Sun, Dimitrios Velenis, and Eric Beyne are with imec, 3001 Leuven, Belgium (e-mail: geert.vanderplas@imec.be; xiao.sun@imec.be; dimitrios.velenis@imec.be; eric.beyne@imec.be).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCPMT.2021.3102435.

Digital Object Identifier 10.1109/TCPMT.2021.3102435

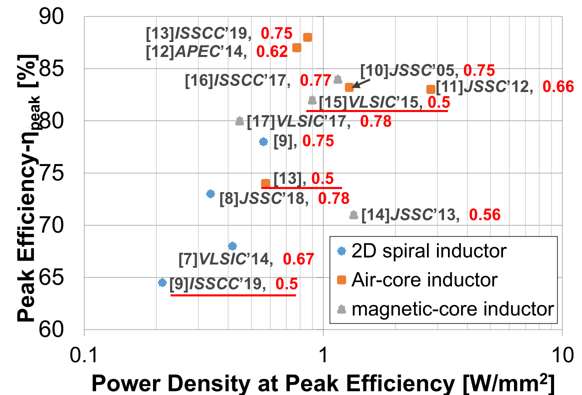

Fig. 1. State-of-the-art literature results for buck converter (only [11]–[15] include PDN into evaluation): peak efficiency η_{peak} versus power density (at η_{peak}). Mark template: reference, buck converter's VCR; Lower VCR value (e.g., 0.5 here) is typically named as higher-ratio design and it has lower efficiency-η from the viewpoint of energy delivery.

We focus on the fully integrated buck converter design, since this converter has more flexible voltage conversion ratios (VCRs) and potentially better efficiency at high-power delivery, when compared with the capacitive converter in [5] and [6]. Fig. 1 lists the literatures of state-of-the-arts [7]–[17] with peak efficiency η_{peak} and the related power density. Their integrated inductor designs are provided in Fig. 2. As shown in Fig. 1, it is promising to design the FIVRs with thin form factor to meet the high-power density and power efficiency for the HPC systems. The power converters with discrete, bulky inductors are out of the scope here, since they are not feasible for system integration [Fig. 3(b) for instance] to meet the thin-package applications.

Generally, there are three kinds of the integrated inductors: 2-D (CMOS-compatible) spiral inductor, 3-D air-core inductor, and magnetic-core inductor. For 2-D spiral inductor, it allows circuits in a monolithic chip. However, its quality factor (Q-factor) is typically within 7 at the switching frequency due to the thin metal layer, which leads to a low efficiency (≤78%) [7]–[9]. Moreover, huge silicon area should be taken for passive components, which is probably not cost-effective. For 3-D air-core inductor, the thick metal layer and inductor height (200 μm) guarantee good Q-factor and peak efficiency η_{peak} (88% at 0.86 W/mm^2, VCR = 0.75) [13]. However,

2156-3950 © 2021 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See https://www.ieee.org/publications/rights/index.html for more information.

Authorized licensed use limited to: IMEC. Downloaded on August 10,2022 at 08:46:26 UTC from IEEE Xplore. Restrictions apply.

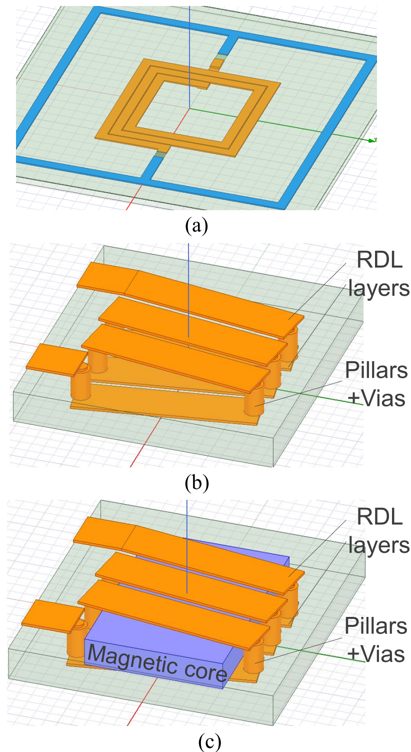

Fig. 2. Three typical inductor fabrications: (a) 2-D spiral inductor, (b) air-core inductor in package, and (c) magnetic-core inductor on logic die or in package.

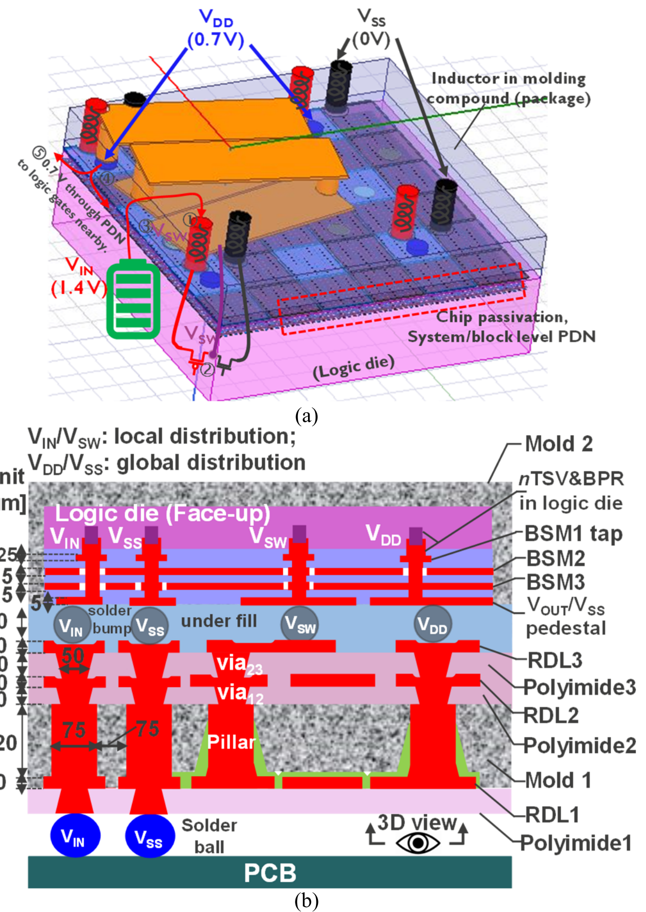

Fig. 3. (a) 3-D view and (b) cross-sectional view of backside power delivery: in-molding inductor (pillar height = 120 μm), backside PDN and the logic die.

the circuit suffers low η_{peak} (74%) for higher VCR = 0.5. The magnetic-core inductor was proposed to move circuit to a lower switching frequency (<150 MHz) to reduce the switching loss. It brings higher efficiency for the buck converter designs: $\eta_{\text{peak}} = 82\%$ at VCR = 0.5 [15], while it brings about the magnetic core-loss and more challenging processing flows. Up to now, effective design guideline for 3-D-integrated buck converter, including power switches, power inductor, and power delivery network (PDN), is still lacking.

Based on the concept of integrating Cu-pillar-based high-Q passives in fan-out wafer-level packaging (FOWLP) [18]–[20], this article presents the design methodology for buck converter with 3-D air-core inductor (inside 200-μm-thick package). The choice of the air-core inductor lays in the fact that it enables full integration, small size, low substrate loss, and high Q-factor with a simpler processing flow. For FOWLP passive technology, a 3-D inductor is fabricated inside the molding compound (~10 μm under the PDN), each regulator can provide the regulated power to every HPC module nearby. The inductor winding consists of two redistribution layers (RDLs), pillars, and vias, and 150-μm minimum pillar pitch would be good for fine-grain power distribution. First, we give a detailed description of the heterogeneous packaging integration of the power delivery including 3-D-integrated buck converter, PDN, and logic die. Subsequently, the modeling of 3-D air-core power inductor together with power switches model is proposed to evaluate the overall system efficiency. In the final part of this work, we evaluate the buck converter's dependency on CMOS switch technology node and output voltage V_{DD}. The loss breakdown and the optimized frequency for power converter are also investigated. Our optimized method shows that a 0.5 ratio buck converter with 1 W/mm^2 of power density can achieve an efficiency $\eta = 88.5\%$ based on 28 nm CMOS.

II. Heterogeneous Package Integration Combining Power Converter, PDN, and Logic Die

Fig. 3 shows the heterogeneous package integration of the backside power delivery, including the integrated buck converter with 3-D air-core inductor, backside PDN, and the logic die. The main principle is given below.

First, the external battery with a supplied voltage $V_{\text{IN}} = 1.4$ V (e.g., VCR = 0.5) goes through the package, bump connection and finally it provides the power to the high-side switch in the buck converter, while its low-side switch is connected with the power grid V_{SS} nearby.

Next, the switching node (V_{sw}) of this regulator goes back to the package and connects with one terminal of the inductor. Thus, a pair of V_{IN}–V_{SS} pads are provided near V_{SW} to reduce the resistive power loss on the logic dies.

Finally, the other terminal of the inductor, V_{DD}, provides the regulated voltage 0.7 V through the backside PDN and distributes the power to the logic circuits nearby. The backside PDN is formed by three backside metal layers BSM1/BSM2/BSM3, and the backside metal layers BSM2/BSM3 can serve as a high-density decoupling capacitor for the PDN using the

Authorized licensed use limited to: IMEC. Downloaded on August 10,2022 at 08:46:26 UTC from IEEE Xplore. Restrictions apply.

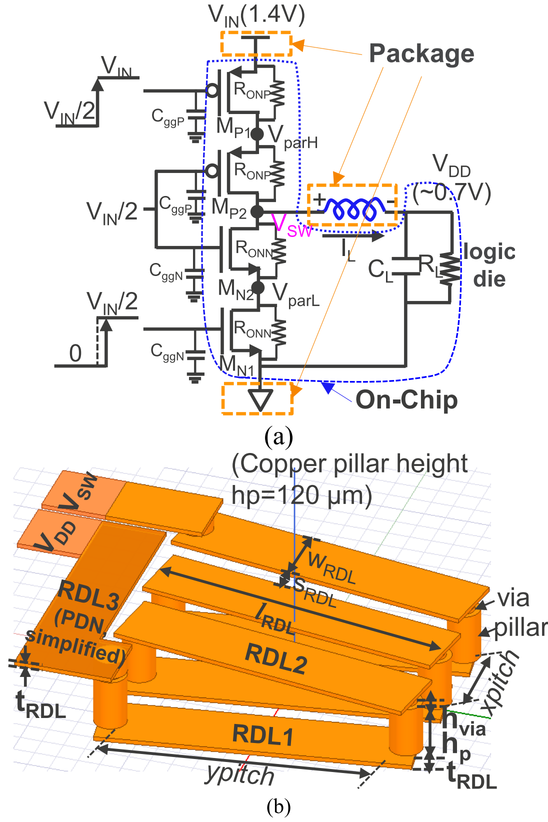

Fig. 4. (a) Schematic of buck converter and (b) its in-package air-core inductor (labeled with inductor dimension).

TABLE I

PARAMETER DESCRIPTION OF INTEGRATED AIR-CORE POWER INDUCTOR

Parameter	Description
n	Winding turns
h_p, D_p	Pillar height and pillar diameter
pitch0	Minimum pillar pitch (=2· D_p)
xpitch, *ypitch*	Real pillar pitch in x-/y- direction (≥*pitch0*)
h_{via}, D_{via}	Height (=10 μm) and diameter (=50 μm) of via-contact
t_{RDL}, s_{RDL}, w_{RDL}	Thickness (=10 μm), spacing (≥10 μm) and width of RDL1 and RDL2; RDL3's thickness is t_{RDL}
pgrid_xpitch, *pgrid_ypitch*	Dimension of inductor unit in x-/y- direction (=400 μm×integer Number)
F	Switching frequency of power switches / current ripple
D	Duty Cycle for power switches' drivers
r=$\Delta I_{pp}/I_{OUT}$	Ratio of inductor's current ripple and DC output current

2.5-D MIM capacitor technology in [5]. The backside PDN option used here has advantages on lower energy and lower IR drops [21]–[23], however, this system integration proposed above is also compatible with the option of front-side PDN. In this design, the interconnects V_{IN} and V_{SW} are only locally distributed to reach the high-side or low-side power switches, while the interconnects V_{DD} and V_{SS} are globally distributed via a third RDL layer (RDL3) to distribute the power uniformly.

Fig. 4 shows the integrated buck converter with a detailed dimension for its in-package air-core inductor. The process parameters of this 3-D inductor including RDL layers, pillars, and vias are shown in Table I. Some rules like RDL thickness or spacing are defined by process limitations. In our optimization below, we use default values of $t_{\text{RDL}} = 10\ \mu$m, $s_{\text{RDL}} = 10\ \mu$m. We constrain the aspect ratio of pillar as 1.6:1. For example, parameters with $h_p = 120\ \mu$m, $D_p = 75\ \mu$m are our default setting, and the scaling of minimal pillar pitch follows the expression shown in (1). The inductor size is determined by the pillar pitch in the x-/y-direction ($x$pitch, $y$pitch)

$$\text{pitch0} = 2 \cdot D_p = 1.25 \cdot h_p. \tag{1}$$

In order to fit each inductor unit (area = $pgrid_xpitch \times p$ $grid_ypitch$) into the power grid of HPC systems, whose minimum $V_{\text{SS}}V_{\text{SS}}$ power pitch is 400 μm, the designed pillar pitch ($x$pitch, $y$pitch) should have discrete values.

There are two difficulties for in-package power inductor design. First, coarse pillar pitch (≥150 μm) and large inductor size are always required. It can be seen in Section IV that the reason for large-size air-core inductor is that we need the passive with large inductance (0.4–2 nH, reducing switching frequency) and low equivalent series resistance (ESR) together to optimize the circuit efficiency. This large passive component would bring considerable power dissipation in backside PDN as well. Moreover, for thin-package integration, the height of the overall inductor is limited, this would bring the challenges to design inductor with high inductance, as the negative coupling is huge between RDL1 and RDL2 wire segments.

III. Modeling of 3-D Air-Core Inductor

For the model of the complete power supply-on-chip, it is divided into three parts: power inductor, power converter, and the PDN. Here we present the detailed model from power device to power converter. First, the model of air-core inductor is given as below, and it has been presented in [20].

For 2-D spiral inductor, it is quite precise to use Grover's and Greenhouse's detailed formulas [24]–[26] for inductance calculation. For an n-turn 3-D inductor shown in Fig. 4(b), vias have $<3\%$ contribution for the overall inductance and their cross-sectional area is very close to the pillars'. The pillars and vias are merged to simplify the calculation. Now the inductor consists of the pillars (height $h'_p = h_p + h_{\text{via}} + t_{\text{RDL}}$) and RDL wire segments. Thus, the inductance evaluation includes $4n$ self-inductance terms, $4n(n-1)$ mutual-inductance terms for wires in the same side, and $4n^2$ mutual-inductance terms for wires in the different sides. Meanwhile, we want to model the contribution from the PDN (RDL3). Thus, one term of PDN self-inductance (L_{selfPDN}) and $4n$ terms of mutual coupling between the PDN and the inductor's RDL wire segments ($M_{\text{PDN,RDL}}$) are considered.

For the self-inductance of the total $4n$ segments, we can use Grover's formulas. The dc self-inductance of a wire with rectangular (2) or circular (3) cross section is expressed as follows:

$$L_{\text{self}}(l, w, t) = 2l\left(\ln\frac{2l}{w+t} + 0.5 + \frac{w+t}{3l}\right) \cdot 10^{-7} \tag{2}$$

$$L_{\text{self}}(l, r) = 2l\left(\ln\frac{2l}{r} - 0.75 + \frac{r}{l}\right) \cdot 10^{-7} \tag{3}$$

where l, w, t, and r are the wire length, rectangular cross sections width, thickness, and circular cross sections radius,

Authorized licensed use limited to: IMEC. Downloaded on August 10,2022 at 08:46:26 UTC from IEEE Xplore. Restrictions apply.

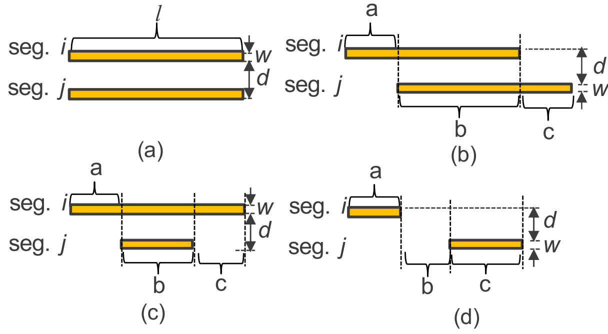

Fig. 5. Pair of segment wires, i and j: (a) perfectly coupling with each other, (b) and (c) with an overlap, and (d) without overlaps.

respectively. In this way, we can solve the inductor's dc self-inductance, which includes pillars combined with vias (circular) and RDLs (rectangular). As the studied integrated power converter operates within 300 MHz, dc inductance is precise for the estimation [25].

Now we want to clarify the calculation rules for different kinds of mutual coupling. As is revealed in [25], if two wire segments are perfectly coupling with each other like Fig. 5(a), their mutual-inductance can be computed from (4) to (6). And M_l represents the mutual-inductance for two wires with length $= l$, width $= w$, and pitch $= d$. For wire with circular cross section (radius $= r$), we can use $\sqrt{\pi} r$ as its wire width

$$M_{ij} = M_l(l, d, w) = 2lQ \cdot 10^{-7} \tag{4}$$

$$Q(l, \mathrm{GMD}) = \ln\left[\frac{l}{\mathrm{GMD}} + \sqrt{1 + \left(\frac{l}{\mathrm{GMD}}\right)^2}\right] - \sqrt{1 + \left(\frac{\mathrm{GMD}}{l}\right)^2} + \frac{\mathrm{GMD}}{l} \tag{5}$$

$$\mathrm{GMD}(d, w) = \exp\left[\mathrm{Ind} - \frac{w^2}{12d^2} - \frac{w^4}{60d^4} - \frac{w^6}{168d^6} - \frac{w^8}{360d^8} - \frac{w^{10}}{660d^{10}} - \cdots\right] \tag{6}$$

where Q is the mutual-inductance parameter which is related to the wire length l and wire's geometric mean distance (GMD). GMD is the function of wires' pitch d and width w.

For another mutual coupling in Fig. 5(b)–(d), the calculation rule is shown in (7a)–(7c), respectively. Here, M_l ($l = a, b, c, a+b+c, a+b, b+c$) is aligned with (4) and Fig. 5(a)

$$M_{ij} = \frac{1}{2}(M_{a+b+c} + M_b - M_a - M_c) \tag{7a}$$

$$M_{ij} = \frac{1}{2}(M_{a+b} + M_{b+c} - M_a - M_c) \tag{7b}$$

$$M_{ij} = \frac{1}{2}(M_{a+b+c} + M_b - M_{a+b} - M_{b+c}). \tag{7c}$$

A. Evaluation of RDL1/RDL2's Mutual Coupling

To simplify the inductor schematic, its top view is given in Fig. 6. Equation (4) can be used to estimate the mutual coupling between the pillars. We name the mutual-inductance as $M_{\mathrm{pillar}+}$ and $M_{\mathrm{pillar}-}$ for the pillar-pair in the same side and the opposite side, respectively.

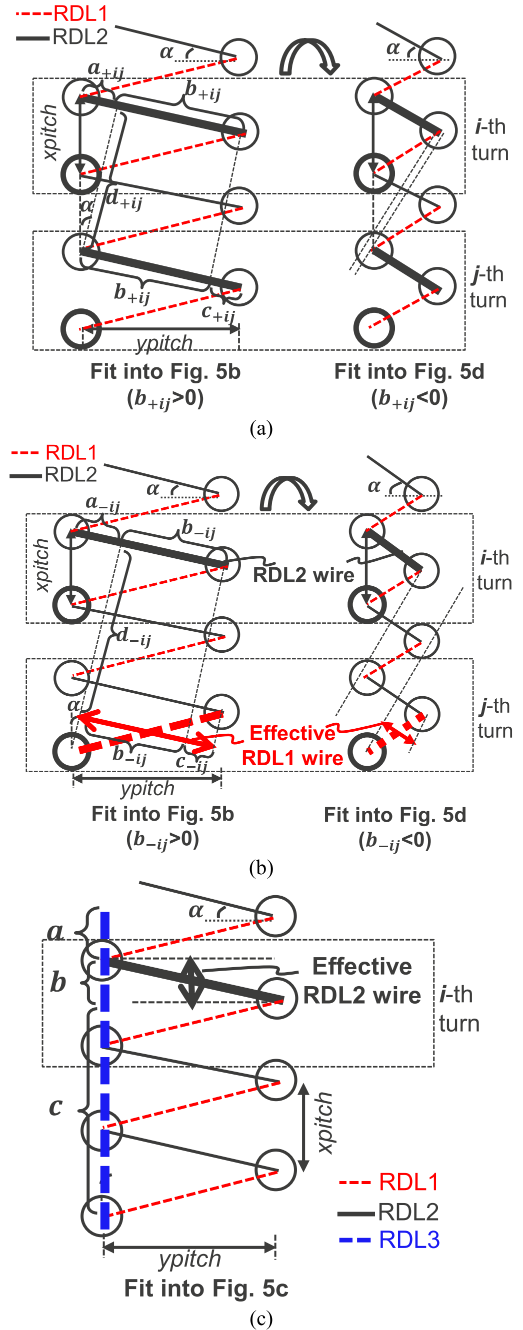

Fig. 6. In inductor design, relative position of (a) RDL wire segments in the same layer, (b) RDL segments in different layers, and (c) PDN (simplified with RDL3) and RDL2 wire segments.

For the mutual coupling in RDL wires, we need to count in the wire pairs that are in the same side ($M_{\mathrm{RDL}+} : 2n^2 - 2n$ terms) and that are in opposite layers ($M_{\mathrm{RDL}-} : 2n^2$ terms). The relative position of each pair of RDL wires is quite random. We need to figure out which case in Fig. 5 does it belong to.

To deal with this difficulty, we use Algorithm 1 to determine the required calculation rule. In Algorithm 1 and Fig. 6, if two wire segments fit into Fig. 5(b)'s description, we give $a_{+ij}, b_{+ij}, c_{+ij}$ and d_{+ij} to present the relative positions of two segments in the same RDL layer, and $a_{-ij}, b_{-ij}, c_{-ij}$, and d_{-ij} are used to define the relative positions of two segments

Authorized licensed use limited to: IMEC. Downloaded on August 10,2022 at 08:46:26 UTC from IEEE Xplore. Restrictions apply.

in the opposite RDL layers. When we detect that b_{+ij} (or b_{-ij}) < 0, they move to Fig. 5(d)'s description. Finally, $M_{\text{RDL}+}$ and $M_{\text{RDL}-}$ can be solved from steps 2–4 and steps 5–8, respectively. We need to mention that $M_{\text{RDL}-}$ would become positive when RDL angle $\alpha > 45°$.

Algorithm 1 Evaluation of RDL's Mutual Coupling

Input: inductor dimension n, xpitch, ypitch, w_{RDL}, t_{RDL}, RDL angle α;
Output: RDLs' mutual-inductance M_{RDL+} and M_{RDL-};
1: Initialize $M_{RDL+} = M_{RDL-} = 0$;
2: for i = 1:(n-1)
  for $j = (i+1)$:n
   $a_{+ij} = c_{+ij} = xpitch \cdot sin\alpha \cdot (j-i)$;
   $b_{+ij} = ypitch/cos\alpha - a_{+ij}$;
   $d_{+ij} = xpitch \cdot cos\alpha \cdot (j-i)$;
3:   if $b_{+ij} < 0 M_{ij}$ follows case in Fig. 3d & Eq. (7d)
   else M_{ij} follows case in Fig. 3b & Eq. (7b)
4:   $M_{RDL+} \leftarrow M_{RDL+} + 4M_{ij}$
  end
 end
5: for i = 1:n
  for j = 1:n
   $d_{-ij} = sqrt(h_p'^2 + (xpitch \cdot cos\alpha \cdot (i-j-0.5))^2)$;
6:   if $\alpha > 45^o$
    $b_{-ij} = xpitch \cdot sin\alpha \cdot ((i-j-1)\cdot(i>j) + (j-i)\cdot(i \le j))$; $a_{-ij} = ypitch/cos\alpha$; $c_{-ij} = xpitch \cdot sin\alpha - a_{-ij}$;
    M_{ij} is positive, and follows case in Fig. 3d & Eq. (7d)
7:   elseif $\alpha \le 45^o$
    $c_{-ij} = xpitch \cdot sin\alpha \cdot ((i-j-1)\cdot(i>j) + (j-i)\cdot(i \le j))$; $b_{-ij} = ypitch/cos\alpha \cdot cos2\alpha - c_{-ij}$; $a_{-ij} = ypitch/cos\alpha - b_{-ij}$;
    if $b_{-ij} < 0$ M_{ij}(neg.) follows case in Fig. 3d & Eq. (7d)
    else M_{ij} (neg.) follows case in Fig. 3b & Eq. (7b)
    end
   end
8:   $M_{RDL-} \leftarrow M_{RDL-} + 2M_{ij}$
  end
 end

B. Mutual Coupling of RDL3 (Represent for First-PDN-Layer) and RDL1/RDL2

In our technology, we have the RDL3 layer to serve as the first metal layer in the PDN, it is spaced 10 μm vertically to RDL2 (inductor's top winding layer). As is mentioned in Fig. 4(a), the 3-D inductor together with the PDN, resistive loads, and the low-side power switches M_{N1}/M_{N2} form the close-loop current flow. The RDL3 wire, serving as the simplified PDN structure, is used to compute the PDN coupling to the 3-D inductor and have a better evaluation of the whole inductance. For different architectures of the processor cores, the PDNs could be quite different, leading to different resistive power loss. However, the PDN resistive loss is out of our scope here. As the inductor, the PDN load and the low-side switches still form the close-loop current flow, we can use the simplified RDL3 wire to calibrate the whole inductance.

In the model of RDL3's self-inductance, $x$pitch or $y$pitch can be used as the width of RDL3 wire to simplify the calculation (we use $y$pitch here)

$$L_{\text{selfPDN}} = L_{\text{self}}(n \cdot x\text{pitch}, y\text{pitch}, t_{\text{RDL}}). \tag{8}$$

The mutual coupling of the RDL3 layer to RDL1/RDL2 is the same as the case shown in Fig. 5(c). For example, we give the relative position of RDL3 and RDL2 (simplified) in Fig. 6(c). Due to the vertical placement of three RDL

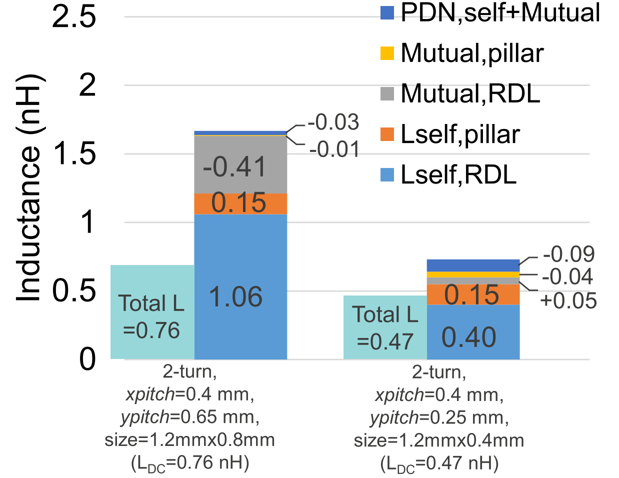

Fig. 7. Detailed inductance breakdown (winding $n = 2$).

layers, parameter w in Fig. 5(c) is equal to t_{RDL} here. Thus, $M_{\text{PDN,RDL}}$ can be deducted from (7c). Summing the self-inductance contributed by each inductor segment the PDN, together with the mutual-inductance between every pair of segments discussed above, the total inductance for 3-D air-core inductor is obtained.

The coupling of the RDL3 wire to the inductor can be important when the angle α is quite large (narrow $y$pitch). Fig. 7 provides the inductance breakdown of this 3-D inductor with winding $n = 2$. For an inductor with a size = 1.2 mm × 0.8 mm (small angle α), the RDL3 wire (mimicking the PDN) has a small impact on the whole inductance (only 4%). When the 3-D inductor shrinks and has a smaller inductance and a larger α (size = 1.2 mm × 0.4 mm), the mutual coupling of the RDL3 wire becomes important, leading to a larger contribution to the whole inductance computation.

C. Modeling of AC ESR

In the meanwhile, we need to compute the copper loss, and it is related to the inductor's ESR. The dc resistance, which includes the pillars, vias, and RDLs, is shown in (9). Here, l_{RDL}, w_{RDL}, t_{RDL}, h_p, D_p, h_{via}, and D_{via} are the dimensions of each segment and they are shown in Table I. Taking the skin effect into consideration, the ac resistance at kth switching frequency harmonic–$R_{\text{ac},k}$ can be solved with [27]. In (10), zeros, poles (z_i, p_i) and lump (number of zero-pole pairs) are used to define the behavior of the ac impedance

$$R_{\text{dc}} = 2n \cdot \left(\rho_{\text{Cu}} \frac{l_{\text{RDL}}}{t_{\text{RDL}} \cdot w_{\text{RDL}}} + \rho_{\text{Cu}} \frac{4h_{\text{via}}}{\pi D_{\text{via}}^2} + \rho_{\text{Cu}} \frac{4h_p}{\pi D_p^2}\right) \tag{9}$$

$$R_{\text{ac},k} = \text{real}\left(R_{\text{dc}} \frac{\prod_{i=1}^{\text{lump}}(1 - j2\pi f_k/z_i)}{\prod_{i=1}^{\text{lump}}(1 - j2\pi f_k/p_i)}\right) = \alpha_k \cdot R_{\text{dc}}. \tag{10}$$

D. Comparison: Modeling Versus Simulation Results

In order to prove the effectiveness of our method, we compare its calculated result with the simulation result from 3-D Electro-Magnetics High-Frequency Structure Simulator (HFSS) based on the finite element method (FEM) (simulated

Authorized licensed use limited to: IMEC. Downloaded on August 10,2022 at 08:46:26 UTC from IEEE Xplore. Restrictions apply.

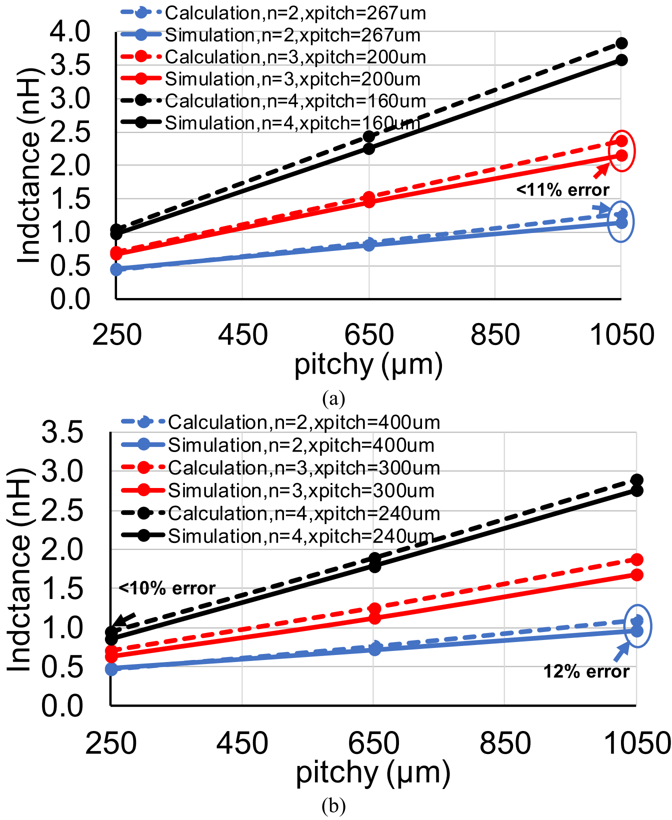

Fig. 8. With the inductor length along x-direction equals to (a) 0.8 mm and (b) 1.2 mm, the inductance comparison between theoretical calculation and HFSS simulation results at 200–300 MHz.

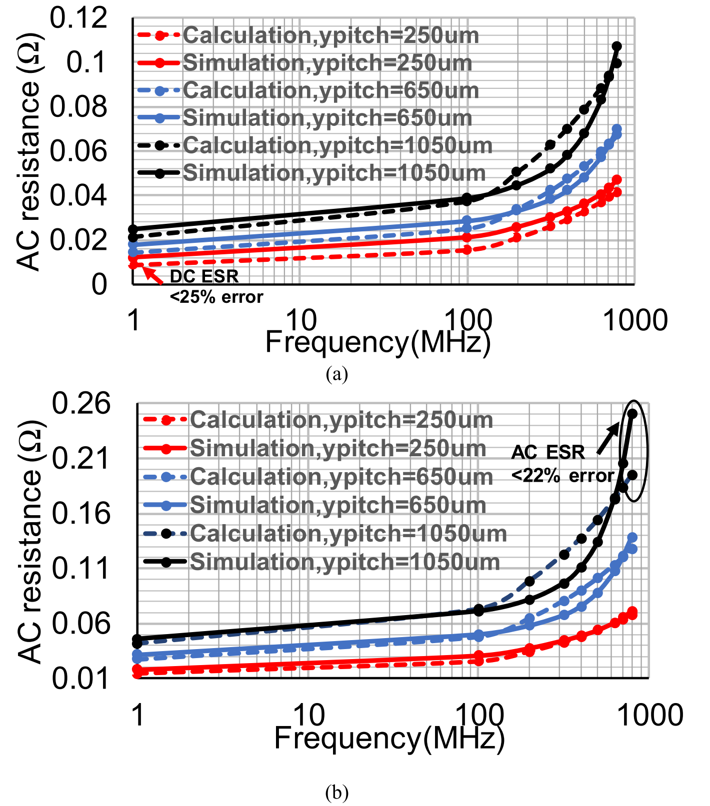

Fig. 9. Results of ac resistance for the inductor with (a) $n = 2$, $x$pitch $= 400$ μm and (b) $n = 3$, $x$pitch $= 300$ μm.

TABLE II

COMPARISON OF DC AND AC COPPER LOSS

D	$R_{AC,1}$	$R_{AC,2}$	$R_{AC,3}$	$I_{DD}^2 R_{DC}$	$I_1^2 R_{AC,1}/2$	$I_2^2 R_{AC,2}/2$	$I_3^2 R_{AC,3}/2$
0.5					0.94	0.00	0.02
0.33	2.9	4.0	5.0	1.0	0.90	0.08	0.00
0.25					0.84	0.15	0.02

*R_{DC} and I_{DD} are both normalized to 1, and the fundamental f=300 MHz, r=2.

inductance at 200–300 MHz) [28]. The proposed buck converter has 0.4–2 nH inductance and operates within 300 MHz (see Section IV, $V_{\mathrm{OUT}} = 0.7$–0.9 V). Thus, we provide the theoretical data within this range, and they fit simulation results well. From Fig. 8, we can find that our method behaves simpler, and its computation error is within 12% for inductor design with 2–4 turns.

In Fig. 9, we can see that the estimated ac ESR has a maximum error of 25% for a wide range of $f < 800$ MHz. As will be shown in Section IV, this large error for ac ESR at the high frequency has limited impact on loss calculation of the converter.

IV. Modeling and Optimization of a Fully-Integrated Buck Converter

First, we want to analyze the inductor's copper loss. According to [29], if we assume the slope of inductor current as constant (I_{DD} as its dc component), the inductor current amplitude I_k at the kth switching frequency harmonics, and the total copper loss is shown in the following equations:

$$I_k \approx \frac{r \cdot I_{\mathrm{DD}} \cdot \sin(D\pi k)}{(\pi k)^2 \cdot D \cdot (1-D)} \tag{11}$$

$$P_{\mathrm{ESR}} = R_{\mathrm{dc}} I_{\mathrm{DD}}^2 + \sum_{k=1}^{k_{\max}} R_{\mathrm{ac},k} I_k^2/2 \tag{12}$$

where r is the ratio of inductor's current ripple to output current I_{DD}. From Table II, we find that: if the fundamental frequency $f = 300$ MHz, the third switching frequency harmonics only contributes ~2% of ac copper loss. Thus, only the first and second switching frequency harmonics are taken into the calculation of ac copper loss to simplify the calculation.

Next, we will discuss about the power switches in the buck converter. The power losses in the switches and 3-D inductors should be combined to evaluate the overall efficiency. If only the inductor's efficiency is evaluated, it has $\eta > 98\%$ in high-frequency operation, while the resulted switching loss would destroy the whole performance [29]. For the gate driver shown in Fig. 4(a), generally the power losses in the switches consist of: 1) conduction loss; 2) gate-charging loss; 3) switching loss; 4) output capacitance loss in switches; 5) reverse recovery loss in the body diode; and 6) deadtime loss. In [20], only the first two losses are included into the analysis, which underestimates the total power losses. We refer to [30] to obtain more accurate power losses in the power switches. The total losses in the power switches (P_{SW}) can be deducted from [30], which is related to the switch sizes. We define W_P and W_N as the widths of high-side and low-side power switches, respectively, and the minimum channel length is used by default.

Authorized licensed use limited to: IMEC. Downloaded on August 10,2022 at 08:46:26 UTC from IEEE Xplore. Restrictions apply.

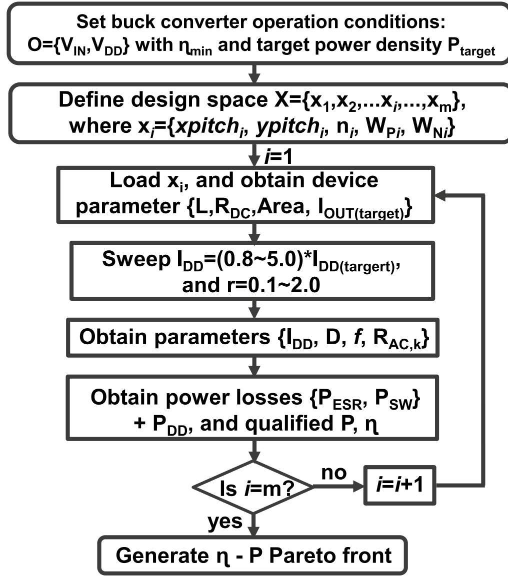

Fig. 10. Optimization flowchart of a buck converter with air-core inductor.

TABLE III

INDUCTOR DESIGNS

Inductor design	A	B	C	D	E
n	2	2	2	3	3
xpitch (mm)	0.4	0.4	0.4	0.3	0.3
ypitch (mm)	1.05	0.65	0.25	1.05	0.25
L (nH)	1.1	0.76	0.47	1.9	0.7
ESR (mΩ)	21.4	14.4	9	41.7	14.5
Area (mm^2)	1.2×1.2	1.2×0.8	1.2×0.4	1.2×1.2	1.2×0.4

Combing the total power losses in the 3-D inductor in (12), we use the flowchart in Fig. 10 to optimize the system efficiency. First, we sweep the inductor key parameters ($x$pitch$_i$, $y$pitch$_i$, n_i) and the power switches' widths (W_{Pi}, W_{Ni}). For each inductor design, we use the inductor model in Section III to solve the inductance L and the resistance R_{dc}. Following the link between the inductor device (with value L) and the power switches (with switching frequency f), which is shown in (13), we find out the optimized power loss by sweeping the parameter f or r:

$$L \cdot r I_{\text{DD}} = \frac{V_{\text{DD}}(1-D)}{f}. \tag{13}$$

Following the design methodology given above, the optimized parameters ($x$pitch, $y$pitch, n, W_P, and W_N) can be deducted for a fixed design with target power density, V_{IN} and V_{OUT}. When the output load is lower, the switch size (W_P, W_N) should be smaller to reduce the related losses for better system efficiency [31]. A larger input voltage V_{IN} means a larger gate-drive voltage $|V_{\text{GS}}| = V_{\text{IN}}/2$ for the switches, which allows a smaller switch size for the equivalent ON-resistance. This is shown in Fig. 11 with an example of a 0.5 ratio buck converter with a three turn, 1.2 mm × 0.8 mm-size inductor and 28 nm CMOS.

In Table III, we list the inductor designs identified on the Pareto front based on the optimization method above. The results in Figs. 12–14 are based on those inductor designs.

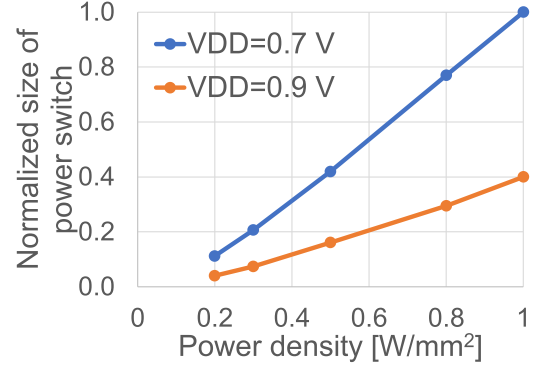

Fig. 11. Normalized switch size for different power density and the output V_{DD} (normalized by the case with 1 W/mm^2 power density and $V_{\text{DD}} = 0.7$ V).

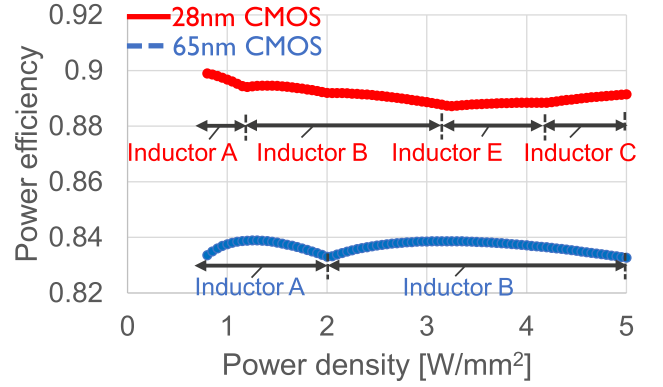

Fig. 12. Optimized η-P performance for a 0.5 ratio buck converter with $V_{\text{DD}} = 0.9$ V based on 65/28 nm CMOS.

A. Dependency on CMOS Technology

Fig. 12 gives the optimized results for a converter with $V_{\text{IN}} = 1.8$ V and $V_{\text{OUT}} = 0.9$ V (VCR = 0.5). We find that inductor designs with $n = 2$, 3 are preferred. To optimize η at a particular power density ranging from 1 to 5 W/mm^2, a 0.5 ratio buck converter can have $\eta = 88.5\%$ and 83% based on 28 nm CMOS and 65 nm CMOS, respectively. As the converter always operates in $f = 50$–300 MHz, the Q-factor for inductor (e.g., inductor B) reaches 35 at 300 MHz.

For buck converter's dependency on CMOS devices, we find that: less advanced CMOS technology (65 nm) requires larger inductance value to allow the converter to operate at a lower frequency range. For instance, for a given power density = 1.5 W/mm^2 with a less advantage CMOS (65 nm), the optimized circuit frequency is 90 MHz (2× times lower), and inductor A with a higher inductance is required. This optimizes the power efficiency with a mitigated power loss in the switches.

B. Loss Breakdown

Fig. 13 shows the loss breakdown based on some particular inductor designs at a 1 W/mm^2 power delivery (its operation f is optimized automatically). Both inductors A and B are good designs for the buck converter. We find that the total power losses in the inductor and the switches need to be balanced to optimize the overall efficiency, otherwise it would ruin the whole system efficiency (inductor design C in Fig. 13 for

Authorized licensed use limited to: IMEC. Downloaded on August 10,2022 at 08:46:26 UTC from IEEE Xplore. Restrictions apply.

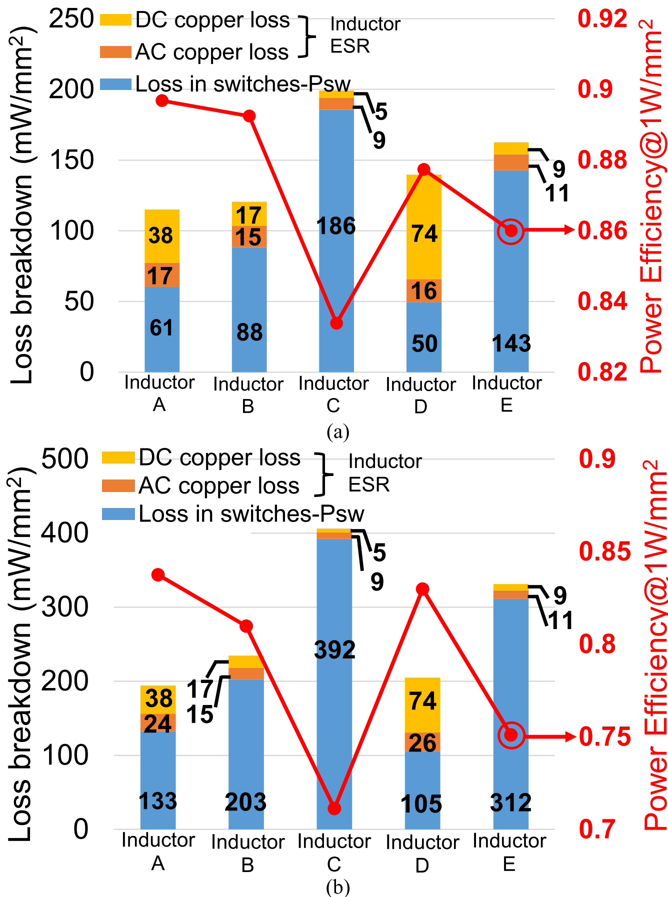

Fig. 13. With 1 W/mm^2 power density, the loss breakdown of a 0.5 ratio buck converter ($V_{DD} = 0.9$ V) based on (a) 28 nm and (b) 65 nm CMOS.

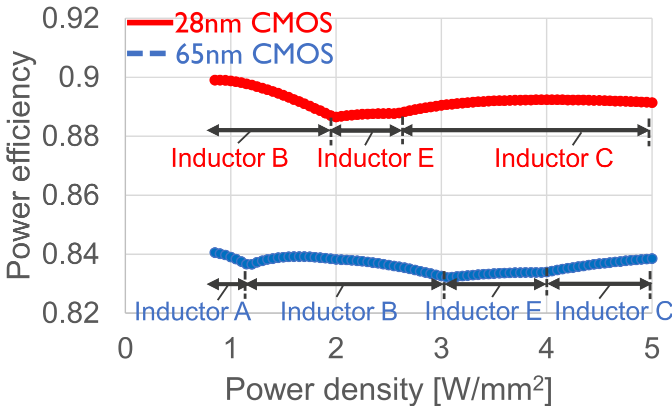

Fig. 14. Optimized η-P performance for a 0.5 ratio buck converter with $V_{DD} = 0.7$ V based on 65/28 nm CMOS.

instance). For inductance selection, it is quite related to the switching frequency and the winding ESR. The optimal value is close to 1 nH based on our design methodology.

C. Dependency on Output Voltage-V_{DD}

Next, the power efficiency at a lower $V_{DD} = 0.7$ V is investigated. From Fig. 14, the power efficiency of the buck converter keeps 88.5% and 83% based on 28 nm CMOS and 65 nm CMOS, respectively, and it is almost the same as the one with higher V_{DD} in Fig. 12. Compared with the condition with higher V_{DD} (0.9 V), it allows the use of smaller L. For example, if the converter operates at 1.5 W/mm^2 based on 65 nm CMOS, inductor A ($L = 1.1$ nH) is required when $V_{DD} = 0.9$ V. However, it is suggested to use inductor B (0.76 nH) when V_{DD} scales to 0.7 V. It can also be predicted from (13) that a lower L can be designed for a lower output voltage V_{DD}.

V. Conclusion

In this work, we propose an analytical model to optimize the integrated buck converters using 3-D in-package air-core inductor. For this integrated inductor with pillar height $h_p = 120$ μm and a minimum pillar pitch of 150 μm, its Q-factor can achieve 35 at 300 MHz. Based on our design methodology, the overall efficiency of a buck converter is optimized. This provides the optimized design parameters for both the inductor device and the circuit. Moreover, the converter's dependency on CMOS technology and output voltage V_{DD} is investigated. It shows that the output voltage has a limited effect on circuit performance, and a 0.5 ratio buck converter with 1–5 W/mm^2 of power density achieves an efficiency $\eta = 88.5\%$ and 83% based on 28 nm CMOS and 65 nm CMOS, respectively.

References

[1] S. Naffziger, "Integrated power conversion strategies across laptop, server and graphics products," in *Proc. Power SoC Conf.*, Oct. 2016. [Online]. Available: http://pwrsocevents.com/wp-content/uploads/2016-presentations/live/0_PRES_Naffziger.pdf

[2] L. T. Su, S. Naffziger, and M. Papermaster, "Multi-chip technologies to unleash computing performance gains over the next decade," in *IEDM Tech. Dig.*, Dec. 2017, pp. 1.1.1–1.1.8.

[3] M. Horowitz, "1.1 Computing's energy problem (and what we can do about it)," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 10–14.

[4] W. J. Lambert, M. J. Hill, K. Radhakrishnan, L. Wojewoda, and A. E. Augustine, "Package inductors for Intel fully integrated voltage regulators," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 6, no. 1, pp. 3–11, Jan. 2016.

[5] H. Lin *et al.*, "91.5%-efficiency fully integrated voltage regulator with 86 fF/μm^2-high-density 2.5D MIM capacitor," in *Proc. Symp. VLSI Technol.*, Jun. 2021.

[6] N. Butzen and M. Steyaert, "10.1 A 1.1W/mm^2-power-density 82%-efficiency fully integrated 3:1 switched-capacitor DC-DC converter in baseline 28 nm CMOS using stage outphasing and multiphase soft-charging," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 178–179.

[7] H. Krishnamurthy *et al.*, "A 500 MHz, 68% efficient, fully on-die digitally controlled buck voltage regulator on 22 nm tri-gate CMOS," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2014, pp. 1–2.

[8] T. Jia and J. Gu, "A fully integrated buck regulator with 2-GHz resonant switching for low-power applications," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2663–2674, Sep. 2018.

[9] N. Tang, B. Nguyen, Y. Tang, W. Hong, Z. Zhou, and D. Heo, "8.4 fully integrated buck converter with 78% efficiency at 365 mW output power enabled by switched-inductor capacitor topology and inductor current reduction technique," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 152–153.

[10] P. Hazucha *et al.*, "A 233-MHz 80%-87% efficient four-phase DC-DC converter utilizing air-core inductors on package," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 838–845, Apr. 2005.

[11] N. Sturcken *et al.*, "A switched-inductor integrated voltage regulator with nonlinear feedback and network-on-chip load in 45 nm SOI," *IEEE J. Solid-State Circuits*, vol. 47, no. 8, pp. 1935–1945, Aug. 2012.

[12] E. A. Burton *et al.*, "FIVR—Fully integrated voltage regulators on 4th generation Intel Core SoCs," in *Proc. 29th Annu. IEEE Appl. Power Electron. Spec. Conf. Expo.*, Mar. 2014, pp. 432–439.

Authorized licensed use limited to: IMEC. Downloaded on August 10,2022 at 08:46:26 UTC from IEEE Xplore. Restrictions apply.

[13] C. Schaef *et al.*, "8.5 A fully integrated voltage regulator in 14 nm CMOS with package-embedded air-core inductor featuring self-trimmed, digitally controlled variable on-time discontinuous conduction mode operation," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 154–155.

[14] N. Sturcken *et al.*, "A 2.5D integrated voltage regulator using coupled-magnetic-core inductors on silicon interposer," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 244–254, Jan. 2013.

[15] K. Tien *et al.*, "An 82%-efficient multiphase voltage-regulator 3D interposer with on-chip magnetic inductors," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2015, pp. 192–193.

[16] H. K. Krishnamurthy *et al.*, "A digitally controlled fully integrated voltage regulator with on-die solenoid inductor with planar magnetic core in 14 nm tri-gate CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 336–337.

[17] H. K. Krishnamurthy *et al.*, "A digitally controlled fully integrated voltage regulator with 3D-TSV based on-die solenoid inductor with backside planar magnetic core in 14 nm tri-gate CMOS," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2017, pp. C148–C149.

[18] X. Sun *et al.*, "3D heterogeneous package integration of air/magnetic core inductor: 89%-efficiency buck converter with backside power delivery network," in *Proc. Symp. VLSI Technol.*, Jun. 2020, pp. 1–2.

[19] H. Lin *et al.*, "Backside power delivery with a direct 14:1/19:1 high-ratio point-of-load power converter for servers and datacenters," in *Proc. Symp. VLSI Technol.*, Jun. 2021, pp. 1–2.

[20] H. Lin *et al.*, "Modeling of buck converter with 3D air-core inductor," in *Proc. ESTC*, Sep. 2020, pp. 1–6.

[21] M. O. Hossen *et al.*, "Power delivery network (PDN) modeling for backside-PDN configurations with buried power rails and μTSVs," *IEEE Trans. Electron. Devices*, vol. 67, no. 1, pp. 11–17, Jan. 2020.

[22] D. Prasad *et al.*, "Buried power rails and back-side power grids: Arm CPU power delivery network design beyond 5 nm," in *IEDM Tech. Dig.*, Dec. 2019, pp. 19.1.1–19.1.4.

[23] B. Chava *et al.*, "Backside power delivery as a scaling knob for future systems," *Proc. SPIE*, vol. 10962, Mar. 2019, Art. no. 1096205.

[24] F. W. Grover, *Inductance Calculations*. New York, NY, USA: Van Nostrand, 1962.

[25] H. M. Greenhouse, "Design of planar rectangular microelectronic inductors," *IEEE Trans. Parts, Hybrids, Packag.*, vol. PHP-10, no. 2, pp. 101–109, Jun. 1974.

[26] C. P. Yue and S. S. Wong, "Physical modeling of spiral inductors on silicon," *IEEE Trans. Electron Devices*, vol. 47, no. 3, pp. 560–568, Mar. 2000.

[27] K. Kundert, *Modeling Skin Effect in Inductors*. Melbourne, VIC, Australia: Designer's Guide Consulting, May 2006. [Online]. Available: https://www.designers-guide.org/Modeling

[28] Ansys. *ANSYS HFSS*. Accessed: 2018. [Online]. Available: https://www.ansys.com/products/electronics/ansys-hfss

[29] T. M. Andersen, C. M. Zingerli, F. Krismer, J. W. Kolar, N. Wang, and C. Mathuna, "Modeling and Pareto optimization of microfabricated inductors for power supply on chip," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4422–4430, Sep. 2013.

[30] (2016). *Rohm Semiconductor, Switching Regulator IC Series: Efficiency of Buck Converter, Application Note*. [Online]. Available: https://fscdn.rohm.com/en/products/databook/applinote/ic/power/switching_regulator/buck_converter_efficiency_app-e.pdf

[31] C. Huang and P. K. T. Mok, "A 100 MHz 82.4% efficiency package-bondwire based four-phase fully-integrated buck converter with flying capacitor for area reduction," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 2977–2988, Dec. 2013.

Hesheng Lin (Graduate Student Member, IEEE) received the M.S. (Hons.) degree from the School of Electronic and Computer Engineering, Peking University, Beijing, China, in 2016. He is currently pursuing the Ph.D. degree with KU Leuven, Leuven, Belgium, continuing his study on power delivery network designs for computing systems and the related integrated power management integrated circuits (ICs).

He held an Internship (or Research Assistant) positions with Solomon Systech Ltd., Shenzhen, China, from 2014 to 2016, SKL-AMSV, University of Macau, Macau, China, from 2016 to 2017, and Peking University, Shenzhen, 2017 fall. He is with imec, Leuven.

Geert Van der Plas (Member, IEEE) received the Ph.D. degree from Katholieke Universiteit Leuven, Leuven, Belgium, in 2001.

He joined imec, Leuven, Belgium, in 2003. He has been working on energy-efficient data converter, power/signal integrity, and 3-D integration technologies. He is currently a Program Manager in the 3-D program addressing system scaling using advanced 3-D (TSV) and packaging (FO-WLP) technology for high performance, mobile, and Internet of Things (IoT) applications. His research interests are in characterization, modeling, system exploration, and design enablement of 3-D integration technologies.

Xiao Sun (Member, IEEE) received the Ph.D. degree in electrical engineering from Université Grenoble Alpes, Grenoble, France, in 2001.

She is currently a Principal Member of Technical Staff with imec, Leuven, Belgium. She has authored or coauthored more than 70 peer-reviewed journal articles and conference papers and one book chapter. Her research interests include RF design, modeling, and characterization for 3-D interconnects and their impact on 3-D integrated circuits (ICs), heterogeneous integration, and packaging for RF and 5G applications.

Dr. Sun was a recipient of the prestigious Outstanding Session Paper Award from the IEEE Electronic Components and Technology Conference (ECTC) 2015.

Dimitrios Velenis (Member, IEEE) received the M.Sc. and Ph.D. degrees from the University of Rochester, Rochester, NY, USA, in 2000 and 2003, respectively.

He worked as an Assistant Professor with the Department of Electronics and Communications Engineering, Illinois Institute of Technology, Chicago, IL, USA, and a Research Associate with the University of Rochester. In April 2008, he joined imec, Leuven, Belgium, where he worked on cost modeling and benchmarking activities for integration flows in 3-D and silicon photonics interconnects. Since 2015, he has been the Leader of the 3-D System Design and Signal Analysis Team, imec. He has authored or coauthored more than 60 articles in journals and conference proceedings.

Eric Beyne, photograph and biography not available at the time of publication.

Rudy Lauwereins (Fellow, IEEE) is the Vice President with imec, Leuven, Belgium, responsible for the digital and user-centric solutions unit, which focuses on security, connectivity, image processing, sensor fusion, artificial intelligence, machine learning, data analytics, and on making technology society proof. He is the Director of the imec academy, coordinating external and internal technical training curricula. He is a part-time Full Professor with Katholieke Universiteit Leuven, Leuven. He has authored or coauthored more than 500 peer reviewed publications in international journals, books, and conference proceedings.

Authorized licensed use limited to: IMEC. Downloaded on August 10,2022 at 08:46:26 UTC from IEEE Xplore. Restrictions apply.