Linking Room- and Low-Temperature Electrical Performance of MOS Gate Stacks for Cryogenic Applications

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***Abstract* — As the MOS structure plays an essential role in both MOSFET and Si qubit devices, it is desirable to have deeper understanding of MOS material properties and identify limiting factors for cryogenic applications. In this work, based on MOSFETs with four different gate stacks, we extract the oxide trap density and transconductance from the low frequency noise and DC transfer characteristics at room temperature, respectively. With the same gate stacks, Hall mobility as a function of carrier density is measured at 10 K and 10 mK, and the critical density is extracted at 10 mK. These physical quantities are analyzed and correlated explicitly, offering a method to qualitatively compare the quality of the four gate stacks for cryogenic MOS devices, and providing further insight into the material physics at cryogenic temperatures.**

***Index Terms* — high performance computing, quantum computing, cryogenic MOSFET, low frequency noise, transconductance, Hall mobility, critical density.**

I. Introduction

With the development of cryogenic applications, such as high performance computing and quantum computing, cryogenic semiconductor electronics has become one of the vital research topics [1]. Generally, the MOS structure plays a critical role in both CMOS and Si qubits working at cryogenic temperatures. Compared to operation at 300 K, however, the CMOS devices show significantly larger variability and nonnegligible reliability issue associated with disorder and traps of the gate stack at cryogenic temperatures (*T*) [2-3].

The Si qubit devices have been recognized as one of the most promising platforms for implementing large scale quantum computation, thanks to their long coherence times and compatibility with standard CMOS technology [4-5]. However, the gate dielectric and the Si/SiO_2 interface disorder could induce spurious quantum dots, limiting quantum dot formation and control [6]. In addition, dielectric defects lead to charge noise, thereby reducing the qubit coherence [7-8]. Both effects originate from the MOS gate stack and hinder development of large-scale quantum processors.

To evaluate the gate stack quality for cryogenic applications, cryogenic Hall mobility and critical density are commonly used as 2DEG performance metrics [9]. However, they can only provide limited insights into the density or origin of the defects present in the dielectric layers of the gate stack. Though statistical 300-K threshold voltage analysis provides quick assessment of electrostatic disorder, it has not been linked to low-*T* device performance metrics [10]. The low temperature measurement process is also slow and not suitable for statistical and systematic studies, which are essential to investigate cryogenic material properties and subsequent process optimization. Therefore, the correlation of electrical results between room and low temperatures allow insights into the material properties that affect the cryogenic performance [11].

Among the electrical characterization techniques, low frequency noise (LFN) analysis has been recognized as a sensitive, non-destructive and diagnostic tool, which can be used to evaluate the material quality of MOS devices. More specifically, LFN can be used to study the origin of the noise and quantify the trap density in a gate stack [12-14]. Typically, devices show $1/f$ noise originating from carrier number or mobility fluctuations. The former has been shown to be the dominant mechanism in nMOSFETs [15-18]. For this case, according to the McWorther model, a trap density (N_{OT} profile) along the oxide depth *z* can be obtained by converting the $1/f$ noise spectrum [19-24].

In this work, we perform electrical characterization on MOS structures fabricated in a 300 mm integrated process, at the same time with the qubit devices [25]. We measured the LFN on nMOS transistors at room temperature (RT ~ 300 K) and Hall mobility on Hall bar devices at cryogenic temperatures (10 K and 10 mK). We identify a direct correlation between the transistor transconductance, the trap density and the Hall mobility for the four gate stacks used in this study. The method and results presented in this work allow better understanding of cryogenic MOS material properties and identify limiting factors for cryogenic applications.

II. Experiment

A. Device fabrication

The MOS structures are fabricated in a 300 mm Si integration process optimized for qubit devices with multi-level gate stacks [25]. The gate stack starts with an 8 nm in-situ steam generated SiO_2, followed by gate layer 1 (GL1), which is heavily doped 30 nm poly Si (PS) or 20 nm TiN. Subsequently, GL1 is patterned by electron beam lithography and dry etching. Then 5 nm ALD-based SiO_2 is deposited as the insulation layer. Similarly, gate layer 2 (GL2) is formed by 30 nm PS or 30 nm TiN deposition and subsequent patterning process. The

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schematic of the gate stacks for GL1 and GL2 is shown in the inset of Fig. 1(a).

B. *Electrical measurement*

The electrical measurements for transfer characteristics and LFN are performed at RT on a TS 3000-SE probe station with the A-LFNA E4727A Keysight system. In these measurements, the drain-to-source bias V_{DS} is fixed at 20 mV and hence the MOSFETs operate in the linear region. The whole transfer characteristics of MOSFETs with different gate workfunction and equivalent oxide thickness is obtained by applying a wide range of gate-to-source bias V_{GS}, as shown in Fig. 1(a). For the LFN analysis, the input-referred gate noise (S_{VG}) is calculated by dividing the drain current noise (S_{ID}) by the square of the measured transconductance (g_m) at each gate bias point. Noise results are shown in Figs. 2-4.

The transfer characteristics of MOSFETs (Fig. 1(b)) is obtained by a Lakeshore CPX cryogenic probe station at different temperatures. The Hall mobilities are measured at T = 10 mK in a Bluefors LD250 dilution refrigerator and at 10 K in a Lakeshore CRX-VF cryogenic probe station. Hall mobility is measured at $T \leqq 10$ K), considering the temperature requirements of the superconducting magnet in the cryostat. The Hall bar structure is shown in the inset of Fig. 5(b). Using standard lock-in techniques, the electron density is extracted from the transverse Hall voltage V_{xy} and the sheet conductance is extracted from the longitudinal voltage V_{xx} [9]. Combining both, we can extract the mobility at different electron densities n, as shown in Fig. 5. Though Hall measurement is performed only at two temperatures in this work, the mobility and percolation density exhibits almost linear relations [26].

III. Result and Discussion

Fig. 1(a) shows the transfer characteristics and corresponding g_m of MOSFETs with the four different gate stacks at RT. With a given gate oxide thickness, the TiN devices (red) exhibit worse performance than their PS counterparts (black) reflected in lower on-currents I_{on} and maximum g_m ($g_{m,max}$). This can be attributed to remote scattering mechanisms induced by the metal gate [27-28]. Fig. 1(b) exhibits the transfer characteristics of the MOSFET with GL1 & PS measured at different temperatures. The measured devices are large planar MOSFETs with 5 and 1 μm in channel length and width, respectively [14,25,29].

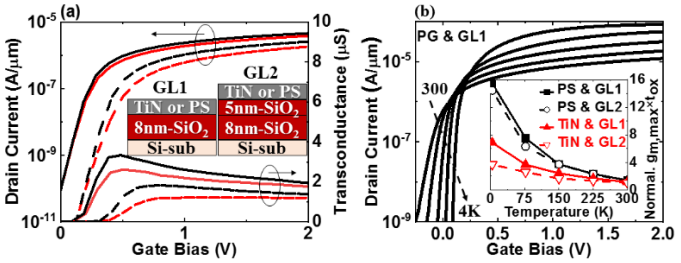

Fig. 1. (a) Transfer characteristics and corresponding g_m of nMOSFETs with four different gate stacks at RT. Note that the four black curves with PS have been shifted to the right so as to have the same off-currents (at 10^{-10} and 10^{-11} A/μm) with their TiN-counterparts at the same gate bias (black/red: PS/TiN and solid/dashed: GL1/GL2). (b) Typical transfer characteristics of the nMOSFET with PS & GL1 measured at 300, 225, 150, 77 and 4 K. The inset shows the products of $g_{m,max}$ and gate oxide thickness t_{ox} at different T, which are normalized to the smallest value of TiN & GL1. Compared to other three, the $g_{m,max}\times t_{ox}$ values of PS & GL1 are greatest at all temperatures. V_{DS} = 20 mV.

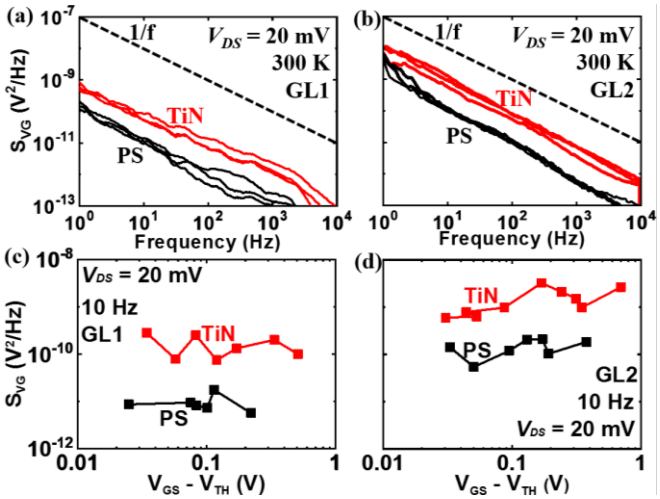

Fig. 2. Input-referred gate noise (S_{VG}) spectra of the nMOSFETs with TiN and PS for (a) GL1 and (b) GL2 devices. For a given gate stack, three traces with the same colour are obtained at three different drain current levels (0.5, 1 and 2 μA/μm) from weak to strong inversion at RT. The measurements have a frequency exponent close to 1 (dashed lines). S_{VG} at 10 Hz versus gate voltage overdrive beyond the threshold voltage ($V_{GS} - V_{TH}$) for (c) GL1 and (d) GL2. For a given gate level TiN devices generally show higher S_{VG} than the PS ones.

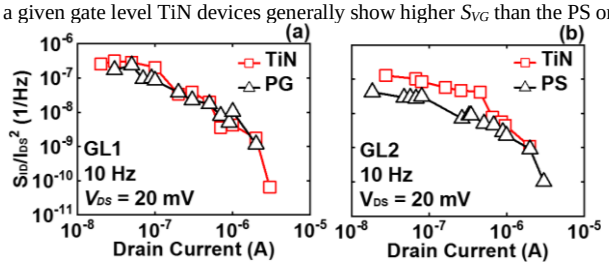

Fig. 3. Normalized drain current noise (S_{ID}/I_{DS}^2) at 10 Hz versus drain current for (a) GL1 and (b) GL2 gate stacks.

S_{VG} versus frequency (a-b) and the corresponding values at 10 Hz with different gate overdrive (c-d) are shown in Fig. 2 for different gate stacks. The normalized drain current noise at 10 Hz as a function of the drain current is displayed in Fig. 3. The normalized drain current noise tends to saturate at lower drain currents, suggesting that carrier number fluctuation is the dominant noise mechanism in the four devices [13, 30]. This is consistent with prior experimental results, showing that noise of nMOSFETs can be explained better by carrier number fluctuation [15-18]. As a result, the frequency exponent $\gamma \approx 1$ (Fig. 2(a-b)) and the nearly gate-independent S_{VG} (Fig. 2(c-d)) implies a uniform trap density in the oxide depth and as well as in energy, located near the Si conduction band edge.

According to the McWorther model, we can extract the oxide trap density distribution from Fig. 2(a) and (b) and the results are depicted in Fig. 4. The distribution of oxide trap density seems fairly uniform in oxide depth (2.1 ~ 1.3 nm from the channel interface). Note that the probing depth of this method is limited by the minimal frequency of the hardware and the background noise of the devices [13]. Because the three traces for a given gate stack are not significantly affected by the drain currents, the oxide trap density seems not to vary significantly with the gate potential around the Si conduction band edge. These outcomes are consistent with the implications by Fig. 2. For a given gate level, the TiN devices show worse oxide quality compared to the PS devices. It may be attributed to the traps induced by atomic diffusion from the metal gate [28,31]. GL2 devices show higher trap density than GL1, which

is believed to be induced by additional plasma damage of the exposed gate stack during the subtractive patterning of GL1 [32-33]. On average, the two PS devices show lower N_{OT} compared to their TiN counterparts (Fig. 4(b)).

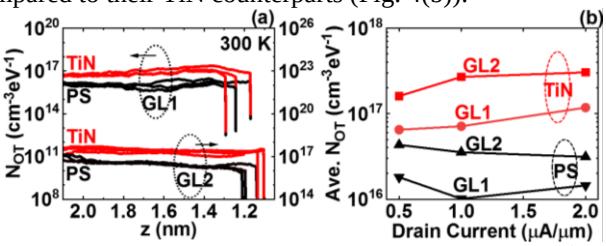

Fig. 4. (a) Oxide trap density (N_{OT}) along the oxide depth z measured from the channel/oxide interface (z = 0 nm) with different gate stacks (TiN in red and PS in black) for GL1 and GL2. The sudden drop around z = 2.1 ~ 1.3 nm is due to the frequency cut-off in the original S_{VG} spectra. For a given gate stack, three traces with the same colour are obtained at three different drain current levels (0.5, 1 and 2 μA/μm) from weak to strong inversion. From each trace, an average N_{OT} value can be determined. Hence, twelve N_{OT} values are plotted versus the drain current in (b).

When a MOSFET is operated in the linear region (V_{DS} = 20 mV), g_m is approximately proportional to the product of gate oxide capacitance C_{ox} and carrier mobility μ [34]. Because C_{ox} is given by the oxide dielectric constant (ε_{ox}) and the gate oxide thickness (t_{ox}), a simple relation can be written as

$$g_m \cdot t_{ox} \propto \varepsilon_{ox} \cdot V_{DS} \cdot \mu \propto \mu. \qquad (1)$$

The four gate stacks of this study are composed of the same insulator (SiO_2) but with different thicknesses (8 and 13 nm for GL1 and GL2, respectively, see Fig. 1(a)). To fairly compare g_m and μ between the four gate stacks, the former needs to be multiplied by t_{ox}. With $g_{m,max}$ from Fig. 1(a), the average N_{OT} from Fig. 4(b) is plotted against $g_{m,max}\times t_{ox}$ in Fig. 6(a). One can see that N_{OT} is higher for lower values of $g_{m,max}\times t_{ox}$ and vice versa. It may be attributed to the fact that the charged oxide traps can degrade carrier mobility through remote Coulomb scattering [27-28]. This correlation remains valid at different current levels as depicted in Fig. 6(a). Note that the similar trend has been observed with different gate stacks and channel materials in our prior work [20-23].

Although N_{OT} is extracted in the oxide between z = 2.1 ~ 1.3 nm (Fig. 4(a)) and it is only a small fraction among the total oxide thickness (see the inset of Fig. 1(a)), it still dominates device performances in terms of mobility [20-23]. This is because that it is closer to the channel interface with stronger influence via electrostatic potential.

So far, merely LFN results obtained at RT have been discussed. By performing Hall bar measurements on the MOS devices with the different gate stacks, Hall mobility at 10 and 10 mK from Fig. 5 is extracted and plotted in Fig. 6(b) as well. Similar to the results derived from LFN measurements, gate stacks with GL1 (GL2) and poly (TiN) gate show the best (worst) material quality in terms of the highest (lowest) Hall mobility and smallest (largest) critical density. Based on this clear correlation between the results at room and cryogenic temperatures, we conclude that a screening of different MOS devices at RT based on LFN analysis and DC characteristics can be a valuable tool to also predict the performance of the same stacks at cryogenic temperatures.

Though the overall correlation between room and low temperatures is clear in Fig. 6, caution should be taken when comparing "TiN & GL1" to "PS & GL2". Especially they show similar Hall mobilities and critical densities at 10 mK in (b). Three distinct factors could affect the gate stack quality. With TiN gate material, oxygen scavenging [35] and the nitrogen diffusing from TiN [31] during thermal annealing could become trap sites, whereas extra processing steps in GL2 could also damage the gate stack quality [32-33]. Defects incurred by these three mechanisms may have different temperature responses, and further act together or compensate with each other. In addition, the lack of understanding at the deep cryogenic temperature further hinders the direct comparison of "TiN & GL1" and "PS & GL2" at 10 mK. However, they and the other two gate stacks ("TiN & GL2" and "PS & GL1") evidently show the expected tendency at 10 K and 10 mK in (b), respectively. Together with the 300 K data in (a), these results show the electrical correlation of the MOS devices between room and cryogenic temperatures.

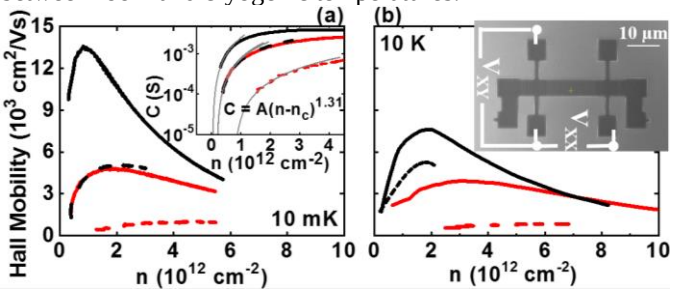

Fig. 5. (a) Hall mobility and conductance C (inset, with thin fitting curves by the function with prefactor A and critical density n_c [36]) measured as a function of carrier density n at 10 mK. (b) Mobility measured at 10 K. The inset in (b) is an image of the device (black/red: PS/TiN and solid/dashed: GL1/GL2).

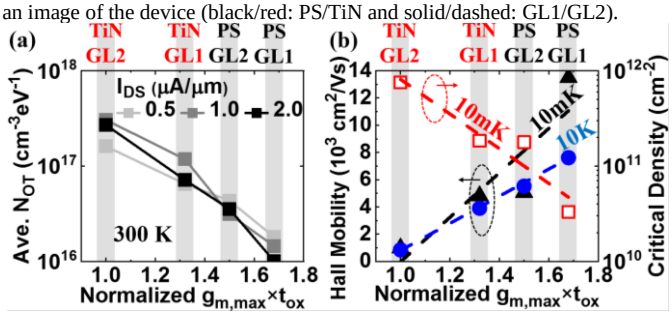

Fig. 6. Electrical correlation of different device metrics at 300 K, 10 K and 10 mK. (a) Average N_{OT} vs normalized $g_{m,max}\times t_{ox}$, (b) Maximal Hall mobility and critical density vs $g_{m,max}\times t_{ox}$. Note that the average N_{OT} and $g_{m,max}\times t_{ox}$ extracted from data measured at 300 K are adopted from Figs. 4(b) and 1(a), respectively. Hall mobility and critical density obtained are taken from Fig. 5.

IV. Conclusion

Based on MOS devices with four different gate stacks, we have extracted the oxide trap density, transconductance, Hall mobility and critical density through low frequency noise (LFN) analysis, DC electrical characterization and Hall measurements, respectively. A clear correlation of these electrical results has been found between 300 K, 10 K and 10 mK for the four gate stacks used in this work. Hall mobility at 10 K and 10 mK (critical density at 10 mK) is found to be clearly correlated to the normalized transconductance obtained at 300 K. As DC and LFN characterization can be performed on full wafers, this correlation may offer a useful method to qualitatively predict the gate stack quality of Si MOS devices based on room-temperature characterization with physical insights and expedite technology development for cryogenic applications.

REFERENCES

[1] IEEE, "Cryogenic Electronics and Quantum Information Processing", *International roadmap for Device and Systems (IRDS)*, 2021.

[2] A. Grill, E. Bury, J. Michl, S. Tyaginov, D. Linten, T. Grasser, B. Parvais, B. Kaczer, M. Waltl and I. Radu, "Reliability and Variability of Advanced CMOS Devices at Cryogenic Temperatures", *IEEE, IRPS*, 2020. 10.1109/IRPS45951.2020.9128316

[3] J. Michl, A. Grill, D. Claes, G. Rzepa, B. Kaczer, D. Linten, I. Radu, T. Grasser and M. Waltl, "Quantum Mechanical Charge Trap Modeling to Explain BTI at Cryogenic Temperatures", *IEEE, IRPS*, 2020. 10.1109/IRPS45951.2020.9128349

[4] L. M. K. Vandersypen, H. Bluhm, J. S. Clarke, A. S. Dzurak, R. Ishihara, A. Morello, D. J. Reilly, L. R. Schreiber and M. Veldhorst, "Interfacing spin qubits in quantum dots and donors-hot, dense, and coherent", *npj Quantum inf*, 3, 34, 2017. https://doi.org/10.1038/s41534-017-0038-y

[5] L. Hutin, "From Silicon CMOS Technology to Spin Qubits", *IMW*, 1-71, 2019. 10.1109/IMW.2019.8739657

[6] A.M.J. Zwerver, T. Krähenmann, T.F. Watson, L. Lampert, H.C. George, R. Pillarisetty, S.A. Bojarski, P. Amin, S.V. Amitonov, J.M. Boter, R. Caudillo, D. Corras-Serrano, J.P. Dehollain, G. Droulers, E.M. Henry, R. Kotlyar, M. Lodari, F. Luthi, D.J. Michalak, B.K. Mueller, S. Neyens, J. Roberts, N. Samkharadze, G. Zheng, O.K. Zietz, G. Scappucci, M. Veldhorst, L.M.K. Vandersypen and J.S. Clarke, "Qubits made by advanced semiconductor manufacturing", arXiv:2101.12650

[7] J. Yoneda, K. Takeda, T. Otsuka, T. Nakajima, M. R. Delbecq, G. Allison, T. Honda, T. Kodera, S. Oda, Y. Hoshi, N. Usami, K. M. Itoh and S. Tarucha, "A quantum-dot spin qubit with coherence limited by charge noise and fidelity higher than 99.9%", *Nat. Nanotech.*, 13, 102, 2018. https://doi.org/10.1038/s41565-017-0014-x

[8] T. Wu and J. Guo, "Variability and Fidelity Limits of Silicon Quantum Gates Due to Random Interface Charge Traps", *IEEE Electron Device Lett.*, 41, 1078, 2020. 10.1109/LED.2020.2997009

[9] D. Sabbagh, N. Thomas, J. Torres, R. Pillarisetty, P. Amin, H. C. George, K. Singh, A. Budrevich, M. Robinson, D. Merrill, L. Ross, J. Roberts, L. Lampert, L. Massa, S.V. Amitonov, J.M. Boter, G. Droulers, H.G.J. Eenink, M. van Hezel, D. Donelson, M. Veldhorst, L.M.K. Vandersypen, J.S. Clarke and G. Scappucci, "Quantum transport properties of industrial $^{28}Si/^{28}SiO_2$", *Phys. Rev. Appl.*, 12, 014013, 2019. https://doi.org/10.1103/PhysRevApplied.12.014013

[10] R. Pillarisetty, N. Thomas, H. C. George, K. Singh, J. Roberts, L. Lampert, P. Amin, T. F. Watson, G. Zheng, J. Torres, M. Metz, R. Kotlyar, P. Keys, J. M. Boter, J. P. Dehollain, G. Droulers, G. Eenink, R. Li, L. Massa, D. Sabbagh, N. Samkharadze, C. Volk, B. P. Wuetz, A. M. Zwerver, M. Veldhorst, G. Scappucci, L. M. K. Vandersypen and J. S. Clarke, "Qubit Device Integration Using Advanced Semiconductor Manufacturing Process Technology" *IEEE IEDM Tech. Dig.*, 6.3.1, 2018. 10.1109/IEDM.2018.8614624

[11] R. Pillarisetty, H.C. George, T.F. Watson, L. Lampert, N. Thomas, S. Bojarski, P. Amin, R. Caudillo, E. Henry, N. Kashani, P. Keys, R. Kotlyar, F. Luthi, D. Michalak, K. Millard, J. Roberts, J. Torres, O. Zietz, T. Krähenmann*, A.-M. Zwerver, M. Veldhorst, G. Scappucci, L.M.K. Vandersypen and J.S. Clarke, "High volume electrical characterization of semiconductor qubits", *IEEE IEDM Tech. Dig.*, 31.5.1, 2019. 10.1109/IEDM19573.2019.8993587

[12] D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed., IEEE Press, 2006.

[13] M. von Haartman and M Östling, *Low-Frequency Noise in Advanced MOS Devices*, Springer, 2007.

[14] E. Simoen and C. Claeys, *Random Telegraph Signals in Semiconductor Devices*, IOP Publishing, 2016.

[15] R. Jayaraman and C. G. Sodini, "A 1/*f* noise technique to extract the oxide trap density near the conduction band edge of silicon", *IEEE Trans. Electron Devices*, 36, 1773, 1989. 10.1109/16.34242

[16] E. Simoen and C. Claeys, "On the flicker noise in submicron silicon MOSFETs", *Solid-State Electron.*, 43, 865, 1999. https://doi.org/10.1016/S0038-1101(98)00322-0

[17] G. Ghibaudo and T. Boutchacha, "Electrical noise and RTS fluctuations in advanced CMOS devices", *Microelectron. Reliab.*, 42, 573, 2002. https://doi.org/10.1016/S0026-2714(02)00025-2

[18] N. Lukyanchikova, M. Petrichuk, N. Garbar, E. Simoen, A. Mercha, C. Claeys, H. van Meer, and K. De Meyer, "The $1/f^{1.7}$ noise in submicron SOI MOSFETs with 2.5 nm nitrided gate oxide", *IEEE Trans. Electron Devices*, 49, 2367, 2002. 10.1109/TED.2002.807448

[19] A. L. McWorther, *Semiconductor surface physics*, University of Pennsylvania Press, 1957.

[20] W. Guo, G. Nicholas, B. Kaczer, R. M. Todi, B. De Jaeger, C. Claeys, A. Mercha, E. Simoen, B. Cretu, J.-M. Routoure and R. Carin, "Low-frequency noise assessment of silicon passivated Ge pMOSFETs with TiN/TaN/HfO_2 gate stack", *IEEE Electron Device Lett.*, 28, 288, 2007. 10.1109/LED.2007.891797

[21] E. Simoen, R. Ritzenthaler, M.-J. Cho, T. Schram, N. Horiguchi, M. Aoulaiche, A. Spessot, P. Fazan and C. Claeys, "Low-frequency noise assessment of the oxide trap density in thick-oxide input-output transistors for DRAM applications", *ECS J. Solid State Sci. Technol.*, 5, N27, 2016. https://iopscience.iop.org/article/10.1149/2.0051606jss

[22] C. Claeys, R. Ritzenthaler, T. Schram, H. Arimura, N. Horiguchi and E. Simoen, "Low-frequency noise assessment of work function engineering cap layers in high-k gate stacks", *ECS J. Solid State Sci. Technol.*, 8, N25, 2019. https://iopscience.iop.org/article/10.1149/2.0221902jss

[23] D. Xie, E. Simoen, F. Chen, H. Arimura and N Horiguchi, "Impact of dummy gate removal and a silicon cap on the low-frequency noise performance of germanium nFinFETs", *IEEE Trans. Electron Devices*, 67, 4713, 2020. 10.1109/TED.2020.3019366

[24] K. Takakura, V. Putcha, E. Simoen, A. R. Alian, U. Peralagu, N. Waldron, B. Parvais and N. Collaert, "Low-Frequency Noise Investigation of GaN/AlGaN Metal–Oxide–Semiconductor High-Electron-Mobility Field-Effect Transistor With Different Gate Length and Orientation", *IEEE Trans. Electron Devices*, 67, 3062, 2020. 10.1109/TED.2020.3002732

[25] R. Li, *et al.*, "A flexible 300 mm integrated Si MOS platform for electron- and hole-spin qubits exploration", *IEEE IEDM Tech. Dig.*, 38.3.1, 2020. 10.1109/IEDM13553.2020.9371956

[26] T. N. Camenzind, A. Elsayed, F. A. Mohiyaddin, R. Li, S. Kubicek, J. Jussot, P. Van Dorpe, B. Govoreanu, I. Radu and D. M. Zumbuhl, "High mobility SiMOSFETs fabricated in a full 300 mm CMOS process", *Mater. Quantum. Technol.*, 1, 041001, 2021. https://iopscience.iop.org/article/10.1088/2633-4356/ac40f4

[27] S. Saito, D. Hisamoto, S. Kimura and M. Hiratani, "Unified mobility model for high-κ gate stacks", *IEEE IEDM Tech. Dig.*, 33.3.1, 2003. 10.1109/IEDM.2003.1269400

[28] K. Maitra, M. M. Frank, V. Narayanan, V. Misra and E. A. Cartier, "Impact of metal gates on remote phonon scattering in titanium nitride/hafnium dioxide n-channel metal-oxide-semiconductor field effect transistors-low temperature electron mobility study", *J. Appl. Phys.*, 102, 114507, 2007. https://doi.org/10.1063/1.2821712

[29] M. Fadlallah, G. Ghibaudo, J. Jomaah, M. Zoaeter and G. Guegan, "Static and low frequency noise characterization of surface- and buried-mode 0.1 µm P and NMOSFETS", *Microelectron. Reliab.* 42, 41, 2002. https://doi.org/10.1016/S0026-2714(01)00232-3

[30] E. Simoen, R. Ritzenthaler, T. Schram, A. Spessot, M. Aoulaiche, P. Fazan, H.-J. Na, S.-G. Lee, Y. Son, K. B. Noh, N. Horiguchi, A. Thean and C. Claeys, "Impact of thermal budget on the low-frequency noise of DRAM peripheral NMOSFETs", *CSTIC*, 2015. 10.1109/CSTIC.2015.7153430

[31] B. J. O'Sullivan, R. Ritzenthaler, E. D. Litta, E. Simoen, V. Machkaoutsan, P. Fazan, Y.-H. Ji, C. Kim, A. Spessot, D. Linten and N. Horiguchi, "Overview of Bias Temperature Instability in Scaled DRAM Logic for Memory Transistors", *IEEE Trans. Device and Materials Reliability*, 20, 258, 2020. 10.1109/TDMR.2020.2982660

[32] L. J. Klein, K. L. M. Lewis, K. A. Slinker, S. Goswami, D. W. van der Weide, R. H. Blick, P. M. Mooney, J. O. Chu, S. N. Coppersmith, M. Friesen and M. A. Eriksson, "Quantum dots and etch-induced depletion of a silicon two-dimensional electron gas", *J. Appl. Phys.*, 99, 023509, 2006. https://doi.org/10.1063/1.2159074

[33] R. Ding, L. J. Klein, M. G. Friesen, M. A. Eriksson and A. E. Wendt, "Sidewall damage in plasma etching of Si/SiGe heterostructures", *J. Vac. Sci. Technol.*, A 27, 836, 2009. https://doi.org/10.1116/1.3097858

[34] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. New York, NY, USA: Wiley, 2007.

[35] E. O. Filatova, S. S. Sakhonenkov, A. S. Konashuk, S. A. Kasaikov and V. Afanasev, "Inhibition of Oxygen Scavenging by TiN at the TiN/SiO_2 Interface by Atomic-Layer-Deposited Al_2O_3 Protective Interlayer", *J. Phys. Chem. C*, 123, 36, 22335, 2019. https://doi.org/10.1021/acs.jpcc.9b05800

[36] L. A. Tracy, E. H. Hwang, K. Eng, G. A. Ten Eyck, E. P. Nordberg, K. Childs, M. S. Carroll, M. P. Lilly and S. Das Sarma, "Observation of percolation-induced two-dimensional metal-insulator transition in a Si MOSFET", *Phys. Rev. B.*, 79, 235307, 2009. https://doi.org/10.1103/PhysRevB.79.235307