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Transport properties of chemically synthesized MoS$_2$ – Dielectric effects and defects scattering

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We report on the electrical characterization of synthetic, large-area MoS$_2$ layers obtained by the sulfurization technique. The effects of dielectric encapsulation and localized defect states on the intrinsic transport properties are explored with the aid of temperature-dependent measurements. We study the effect of dielectric environment by transferring as-grown MoS$_2$ films into different dielectrics such as SiO$_2$, Al$_2$O$_3$, HfO$_2$, and ZrO$_2$ with increasing dielectric permittivity. Electrical data are collected on a statistically-relevant device ensemble and allow to assess device performances on a large scale assembly. Our devices show relative in-sensitiveness of mobility with respect to dielectric encapsulation. We conclude that the device behavior is strongly affected by several scattering mechanisms of different origin that can completely mask any effect related to dielectric mismatch. At low temperatures, conductivity of the devices is thermally activated, a clear footprint of the existence of a mobility edge separating extended states in the conduction band from impurity states in the band-gap. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4971775]

Semiconductor compounds based on the ultra-thin membranes of transition-metal-dichalcogenides (TMDs) are showing great promise as future nanoscale building-block devices. In particular, they are foreseen to play a major role in nanoelectronic applications targeting low-power and high-performance switching devices.[1–3] A key ingredient for the exploitation of their characteristics resides in the correct determination of the limiting factors, which can adversely affect the electronic transport. If the extremely thin body, the relatively large effective mass and dielectric constant can potentially ensure immunity to short-channel effects, a strong effort is still required in order to boost carrier mobility, as high-drive currents are needed for increasing device speed. To this end, it is mandatory not only to accurately control the overall defect density of the as-grown TMD layer but also to wisely choose suitable materials for contacts and gate stack,[4] as they will ultimately control the efficiency of charge injection and the device electrostatics. A vast literature in the recent years have been produced in order to model and interpret the transport properties of TMD based devices with particular attention to the effect of dielectric environment and the role of defects.[5–12] However, fewer reports[13–15] focus on large-area synthetic compounds, more relevant for applications. A full performance characterization of technologically-relevant materials, prone to large-scale integration in logic circuits,[16] is thus lacking. In fact, most of the reported electrical data are limited on devices obtained by the micro-mechanical cleavage technique, which offers the possibility to isolate high-quality single crystals from naturally-occurring bulk materials. Here, we collect electrical data on a large assembly of devices, thus assessing their electrical characteristics on a scale relevant for CMOS integration.

Several theoretical models have been proposed in order to describe charge transport in the single layer devices with a strong effort in the correct understanding of the role that phonons, charged impurities, dielectric interfaces and contacts have on the electronic transport.[17–23] The semiconducting material being few nanometer-thick makes this system particularly dependent on the local electrostatic landscape provided by charges, and in close proximity, to the semiconductor-dielectric interface. Purposely, we have fabricated and characterized field-effect devices from synthetic MoS$_2$, on different dielectric substrates in order to explore the effect of dielectric environment on device characteristics, using the field-effect mobility as a principal metric for device performance.

Large-area TMD layers are grown on c-sapphire substrates following a sulfurization procedure described elsewhere.[24] Briefly, a pre-deposited Mo layer, few Angstrom thick, is thermally annealed into a lamp-based annealing system at temperatures ranging between 800 °C and 1000 °C in an H$_2$S atmosphere. The exposed Mo layer is then converted into few ($\approx$4) layers of MoS$_2$ film, as evidenced by the typical Raman signatures at 408 and 383 cm^{-1}, corresponding to the A1g and E2g vibrational modes in Fig. 1(b). The resulting microscopic structure consists of randomly-oriented poly-crystalline domains interconnected through highly defective grain-boundary regions, as shown by the AFM map in Fig. 1(a).

The as-grown MoS$_2$ layer is subsequently transferred for device processing into different dielectric substrates (see the inset of Fig. 1(b)) via a water-assisted transfer technique.[25,26] After transfer, the stripes of different widths are etched into the MoS$_2$ film through conventional optical lithography and Ar-plasma milling. Contacts to the stripes are subsequently processed via an additional lithographic step followed by the thermal evaporation of Ni and lift-off.

Fig. 2 shows the I$_{ds}$-V$_{GS}$ transfer characteristic (black trace) of a high-mobility field-effect device transferred to a 90 nm-thick SiO$_2$ substrate used as a global back-gate electrode.

FIG. 2. Back-gate transfer characteristics (black trace) taken at $V_{ds} = 1$ V and field-effect mobility (blue trace) as a function of gate voltage for an MoS$_2$ field-effect device on 90 nm SiO$_2$ substrate capped by 20 nm SiO$_2$ followed by 30 nm Al$_2$O$_3$ ALD top-dielectric.
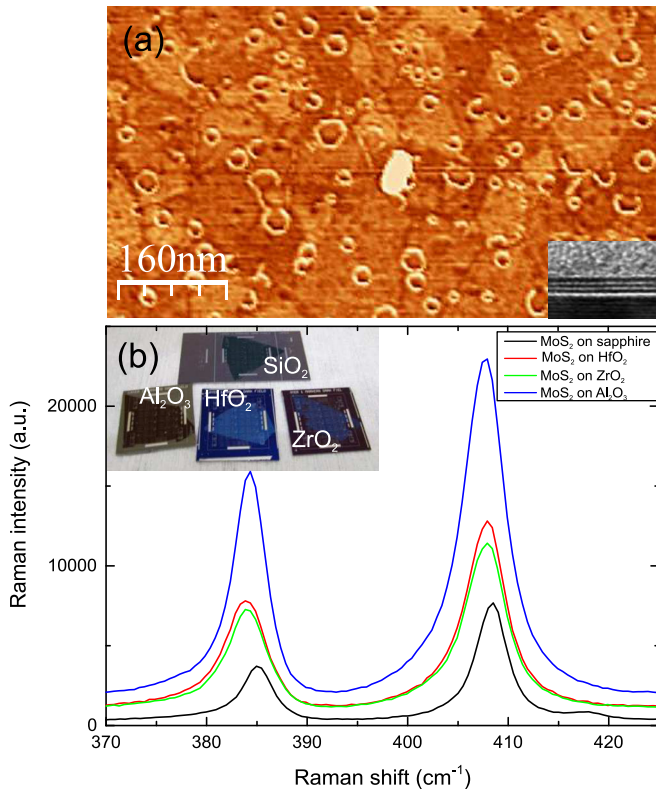
FIG. 1. (a) Atomic force microscopy of the MoS$_2$ layer revealing a non-uniform poly-crystalline structure. The inner layers consist of crystalline domains of lateral size in the range of a few hundreds of nanometers, whereas small unconnected islands of 20 nm lie on the top. (Inset) TEM cross-section of the MoS$_2$ film (b) Raman spectra of the MoS$_2$ layer transferred to different dielectrics. Inset: Optical image of the MoS$_2$ transferred to the ZrO$_2$, HfO$_2$, Al$_2$O$_3$, and SiO$_2$ substrates.

The device is encapsulated with an SiO$_2$ capping layer deposited by chemical vapour deposition. It presents an Ion/Ioff $\approx 10^6$ and on-state resistance of about 5 kΩ/μm. From the transfer characteristics, it is possible to extract a two-terminal field-effect mobility (for $V_{ds} \ll V_{GS} - V_{th}$, where V$_{th}$ is the threshold voltage) of 12 cm^2 V^{-1} s^{-1} calculated using the expression $\mu = dI_{ds}/dV_{GS} \times L/(WC_g V_{ds})$, where L = 2 μm is the channel length, W = 5 μm is the channel width and

$C_g = 3.9 \times 10^{-4}$ F/m^2 is the back-gate capacitance per unit area. The carrier mobility has been extracted by a linear fit of the $I_{ds} - V_{GS}$ characteristics and has to be considered as an "average" value in the gate-voltage range between 15 and 30 V. The estimation of the field-effect mobility contains contributions from the unknown contact resistances, and, as such, it has to be considered as a lower limit.

Dielectric capping has generally the effect of removing adsorbants like water and oxygen that can trap electrons and modify the local electrostatic field.[27] This results in an overall increase in the device performances, as can be seen from the inset of Fig. 3(b). Dielectric capping enables the transconductance peak to be in a measurable voltage range, as opposed to the case of un-capped devices for which uncompensated charges on the surface or in close proximity to the channel have the effect of shifting the threshold voltage towards positive values.[28,29] To shed light on the effects of dielectric encapsulation on the device properties, we have fabricated several field-effect devices on different dielectric substrates with increasing dielectric constants. Subsequently, we have embedded the devices with a relatively thick
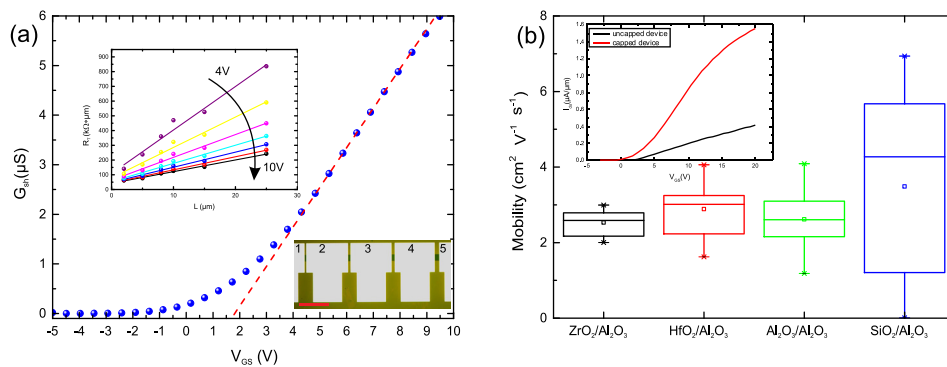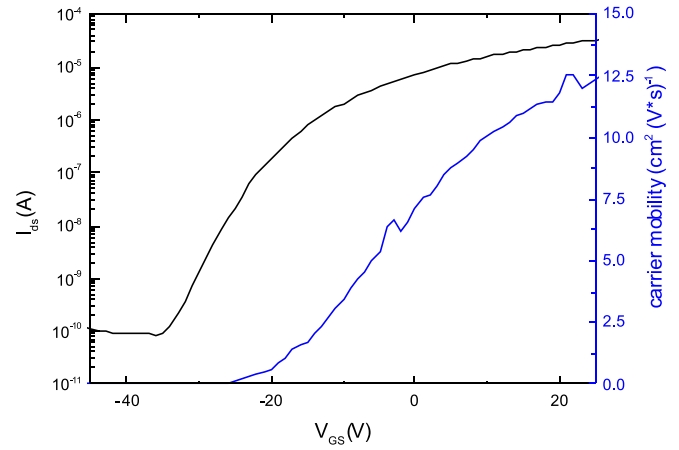

FIG. 3. (a) Sheet conductance G_{sh} as a function of gate voltage extracted following the TLM method. The device has been patterned on top of a ZrO$_2$ substrate and subsequently capped with 30 nm of Al$_2$O$_3$ deposited by ALD. The linear fit (red dashed line) calculated around the point of maximum slope for G_{sh} gives an estimation of the peak electron mobility. (Upper inset) Total 2-probes resistance as a function of channel length for different gate voltages (4–10 V top-to-bottom in step of 1 V). Linear fits give the sheet resistance of the MoS$_2$ layer. (Lower inset) Optical image of the TLM structures is used for parameter extraction. Transfer characteristics are taken between each couple of numbered contacts ($V_{ds} = 1$ V). Scale bar 100 μm (b) statistical distribution of the mobility values extracted following the procedure in (a). Mobility is extracted from an ensemble of 150 TLM structures for each dielectric combination. The dielectric constant of the back dielectrics is 22, 15, 9, and 4 for the ZrO$_2$, HfO$_2$, Al$_2$O$_3$, and SiO$_2$, respectively. (Inset) Transfer characteristics on a linear scale of a representative device fabricated on an Al$_2$O$_3$ substrate followed by 30 nm Al$_2$O$_3$ ALD top-dielectric showing the effect of dielectric encapsulation on the device performances.

($\approx$30 nm) Al_2O_3 top-oxide layer deposited by atomic layer deposition (ALD) to ensure a homogeneous and compact encapsulation of the MoS_2 layer. Prior to the ALD deposition, the samples are left at 150° in vacuum overnight in order to promote the thermal desorption of adsorbates.[30,31] In order to evaluate the intrinsic properties of our MoS_2 layers, we have adopted the transfer line method (TLM).[32–34] This method consists on patterning on top of MoS_2 stripes of widths W, a series of two-terminal devices with variable spacing L between the contacts. The total device resistance can be written as $R_{tot}(V_{GS}) = 2R_c(V_{GS}) + R_{sh}(V_{GS}) \times L/W$, where $R_c(V_{GS})$ is the contact resistance, $R_{sh}(V_{GS}) = \rho(V_{GS})/d$ is the sheet resistance with $\rho(V_{GS})$ being the resistivity and d is the layer thickness. For each gate voltage, we can extract the value of the sheet resistance and contact resistance through the linear fit of the total device resistance with respect to length L, as shown in the upper inset of Fig. 3(a). The mobility is calculated by fitting the $G_{sh} - V_{GS}$ curve (Fig. 3(a), main panel) following the relation $\mu = 1/C_g \times \partial G_{sh}/\partial V_{GS}$, where $G_{sh} = 1/R_{sh}$ is the sheet conductance of the MoS_2 layer. The TLM method thus allows to evaluate the intrinsic value of the mobility ruling out any effect from contact resistance, provided that the total gate capacitance can be well approximated by the geometric capacitance C_g.

Data are collected by semi-automatic probing (Karl Suss PA 300) on a set of 150 devices fabricated on each of the four substrates. Figure 3(b) shows the statistical distribution of the mobility values. Each data on the histogram plot represents the mobility extracted from the sheet conductance and, as such, it represents an averaged value over different sections of the MoS_2 strip. The electrical data collected demonstrate good homogeneity of the transport properties on centimeter scales, thus proving the good control over the growth conditions in large areas. As can be seen from Fig. 3(b), increasing the total dielectric constant of the bottom dielectric (from 4 to 22) does not have a strong impact on transport, with average mobility values almost constant for the four substrates evaluated. In order to elucidate the dominant scattering mechanisms, we have performed temperature-dependent measurement between 9 K and 450 K.

In all the measured devices, the mobility is always decreasing with temperature below T = 250 K,[35] irrespective of the dielectric encapsulation, as evidenced in Fig. 4(a) for a representative sample encapsulated in Al_2O_3. For the low-temperature regime ($T \leq 250°$), we ascribe this behavior to the onset of charge localization[36–39] triggered by disorder. In

this temperature regime, the conductivity extracted from the TLM method has an activated behavior and can be written as

$$\sigma(V_{GS}, T) = \sigma_0 \exp - \left(\frac{\Delta E(V_{GS})}{K_b T} \right),$$

where the K_b is the Boltzmann constant, T is the temperature, and σ_0 is a fitting parameter. $\Delta E(V_{GS}) = E_m - E_F$ represents the energy required to excite an electron from the Fermi energy E_F to an extended state in the conduction band just above the mobility edge E_m.[40] The activation energy over the mobility edge is extracted as a function of gate voltage and gives an estimation of the width of the band-tail generated by localized states in the forbidden gap. As it can be inferred from Fig. 4(b), the band tail is of the order of 100 meV[41,42] at zero gate bias. The activated behavior of the conductivity (Fig. 4(b), inset) is a hallmark of electronic transport in the disordered systems[43] and justifies the rather low values of the mobility seen for these materials.

The first-principles calculations[19] predict an upper limit for the phonon-limited mobility of MoS_2 monolayers of 410 cm^2 (V*s)$^{-1}$, but experimental mobility values are strongly sample-dependent and largely spread over a much lower range. In our synthetic MoS_2 devices, intrinsic phonon-scattering is not the main source of momentum relaxation, as can be evidenced by the relatively small mobility values between 1 and 20 cm^2 V^{-1} s^{-1}, irrespective of the particular dielectric encapsulation. In fact, carriers can interact in a complex way with charged impurities, defects, grain boundaries and phonon modes at the interface with the bottom/top dielectrics.

If charged impurities in the device channel are the main sources of scattering, embedding the material into a high-k environment should result, in a first approximation, into an enhancement of the total mobility compared to the uncapped case due to the damping of the long-range Coulomb interaction.[22,23] However, at high carrier densities, screening of the Coulomb potential can take place and the effect of dielectric mismatch is less important. In this context, low-k dielectrics might favor higher mobility values, thanks to the higher characteristic energy of the surface-optical phonon modes compared to the high-k dielectric case, as outlined by Ma and Jena[18] The strong dependency of the mobility with respect to the gate voltage (Fig. 4(a) (inset)) is, on the other hand, an indication that a charged-impurity scattering mechanism might be at work. Coulomb scatterers can originate from the highly defective intra-grain regions, background doping and/or charged defects introduced during process.
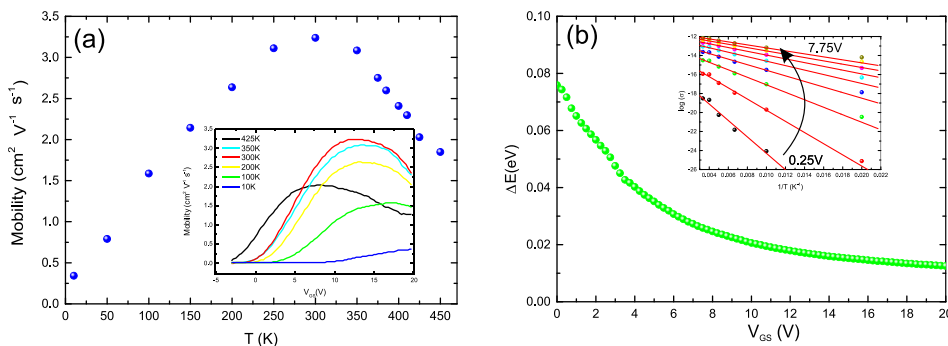

FIG. 4. (a) Mobility as a function of temperature extracted from a 5 μm width device encapsulated in Al_2O_3, following the same procedure outlined in Fig. 3. (Inset) Mobility vs. gate voltage at different temperatures for the same device. (b). Mobility edge (see text) as a function of gate voltage. (Inset) Arrhenius plot of the conductivity between 100 and 300 K extracted from the TLM method (V_{GS} from 0.25 V to 7.75 V in steps of 2.5 V, bottom to top).

Because of the presence of a mobility edge, Coulomb scattering and thermal trapping-release of electrons from trap states are present at the same time, thus preventing the isolation of a pure coulombic interaction between carriers and charged defects.

Our results suggest that a combined effect of different scattering mechanisms can completely mask any effect related to dielectric mismatch. The statistical distribution of the mobility values could be too large to evidence an effect of the dielectric. Vacancies,[8,44–46] anti-sites,[47] grain boundaries,[48,49] and defects originating by random potential fluctuations at the interfaces with dielectrics[9,17] might be responsible for the generation of the band-tail and demands for further improvement of material quality and suitable interface engineering. Further investigations are needed in order to evaluate and possibly mitigate, the effect that a finite density of defect states has on the Fermi level pinning in the contact and channel regions.

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