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Extreme contact shrink for BEOL connectivity

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For the past 50 years, the Moore's law has been well followed by the semiconductor industry. The scaling of transistors and interconnects has been enabled not only by various technological advancements, but also by novel patterning approaches. However, in order to keep up with the Moore's law, further shrinking at all levels of the integrated circuit is needed. Among them is the Back End Of Line (BEOL), where increasingly smaller metal pitches require tight specifications for vias connecting metal lines. In this paper, BEOL via shrink options are investigated, targeting the bottom Critical Dimension (CD) 10.5 nm in order to land on metal pitch 21 nm lines below, while maintaining low defectivity, as well as low Global and Local CD Uniformity (CDU and LCDU, respectively). Approaches to this shrink consist of modifications to the etch chemistry at different levels of the mask etch and liner-assisted shrink, either organic or inorganic. Numerical analysis of CD-Scanning Electron Microscopy (CDSEM) images quantitatively shows efficiency of different approaches to via shrink, together with associated CDU, LCDU and defectivity values. CDSEM results are supplemented by large-area Voltage Contrast (VC) defectivity and Transmission Electron Microscopy (TEM) datasets.

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I. INTRODUCTION

For the past few decades, keeping pace with the Moore's law[1] allowed a tremendous gain in terms of digital information processing speed and storage capacity. However, it is well understood that in order to continue, a perpetual development for new hardware and patterning concepts is needed[2]. One of the challenges is the need for tight-pitch metal lines in the Back End Of Line (BEOL) which, at the next[3] 3nm technology node is expected to be metal pitch 21 nm. Moreover, vias that need to connect such 10.5 nm Critical Dimension (CD) metal lines are currently impossible to print directly at this CD, even with the Extreme Ultraviolet (EUV) lithography. Therefore, such vias need to be printed much larger and a significant shrink is needed to enable landing on tight-pitch metal lines below, without touching neighboring lines. A recent report[4] shows how the shrink at the top of the patterning stack affects elongated features and contact holes of larger (18 nm) CD, corresponding to the 7 nm technology node. Another study[5] points to the resist curing/protection as the key for improvement of the via performance. Direct Self Assembly (DSA) approaches are also considered[6,7,8] but their performance is not yet mature. In this paper, we will focus on a few different industry-relevant approaches to the more advanced 3 nm technology node via shrink.

II. EXPERIMENTAL

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A. Stack and lithography

For this via shrink study, we use the V2 layer of IMEC's three-level, metal pitch 21nm BEOL vehicle[9,10]. In this test case, V2 is the only layer printed since the presence of M3 would significantly hamper inspections of the vias. Since no electrical measurements are possible without the M3 layer, bottom layers are also omitted and the 10.5nm M2 lines, on which V2 would normally land, are replaced with a blanket Cu layer. On top of this Cu, the standard V2 stack (without M3) is deposited, and the photoresist (PR) is exposed and developed (Fig. 1).

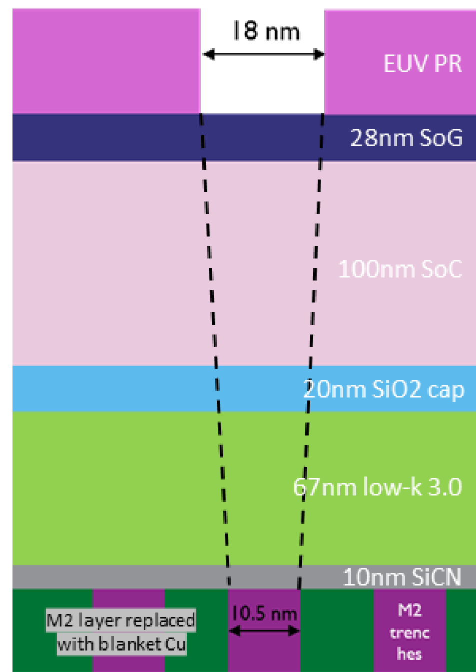

FIG. 1. V2 stack after EUV exposure. Note that for this study, the bottom 10.5 nm CD M2 layer is replaced by blanket Cu. The shown cut is across M2 lines, the shrink-critical y-direction, with the target via CD_y shrinking from 18 nm to 10.5 nm. Photoresist (PR), Spin-on-Glass (SoG) and Spin-on-Carbon (SoC) layers will be stripped at the end of the etch process and SiO_2 will remain the topmost layer of the stack.

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V2 is printed at ADI (after development inspection) CD_x 47nm and CD_y 18nm, as this is the optimum condition for the EUV lithography (Fig.2). During the etch, the target shrink in the y-direction is down to AEI (after etch inspection) 10.5nm in order to match CD of the pitch 21nm M2 lines below. The shrink in x is less critical as CD_x would be normally self-aligned to 18nm CD M3 TiN gratings, which would be the hard mask defining M3 metal lines. As a reminder, M3 lines are not present in this study, and we will not focus on CD_x. From now on, we will refer only to the CD_y.

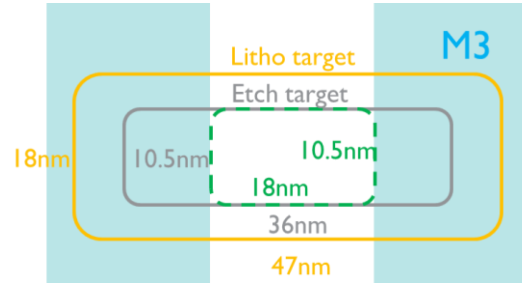

FIG. 2. CD targets of the V2 layer: ADI (yellow), AEI not aligned (grey) and AEI aligned (green) to the M3 hard mask. Note that M3 lines are not present in this study, therefore CD_x will not be self-aligned to it.

B. Etch experiments

1. Baseline etch

The baseline etch sequence of the via stack proceeds as follows: 1) N_2/H_2 cure and descum step which improves the stability of the resist and removes any post-exposure residues, 2) $CF_4/CHF_3/C_4F_8$ SoG etch, 3) $N_2/H_2/CH_4$ SoC opening. 4) CF_4-based SiO_2 cap opening called PV1, 5) low-κ dielectric etch called PV2 and 6) the final

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CO_2 strip of SoC. Steps 1-3 (the mask etch) are performed in a TEL SCCM^{TM} etch chamber, while steps 4-6 are performed in a TEL Vigus^{TM} etch chamber. Both 300 mm processing modules are connected to the same vacuum transport chamber, therefore the vacuum is not broken throughout the entire etch sequence.

Since only low-κ and SiO_2 layers remain at the end of the etch and we don't want to impact the final profile of the via, steps during which these two materials are etched (PV1 and PV2, respectively), and which are relatively straight, are excluded from our design of experiment. We will therefore focus on shrinking at the mask level, i.e. during SoG and SoC etch steps.

Typical CDSEM results showing performance of the baseline recipe are shown in Fig.3. A significant CD shrink of 7.3 nm occurs during the SoG/SoC etch, while the low-κ etch maintains a relatively straight profile with CD going delicately up by only 1.4 nm. This small expansion is attributed to a slight undercut in SoC, which is then transferred into low-κ. The resulting CD is 12.5 nm, therefore 2 nm above target. ADI CDU in the y-direction is well maintained throughout the etch process with CDU being 0.1 nm lower AEI with respect to ADI.

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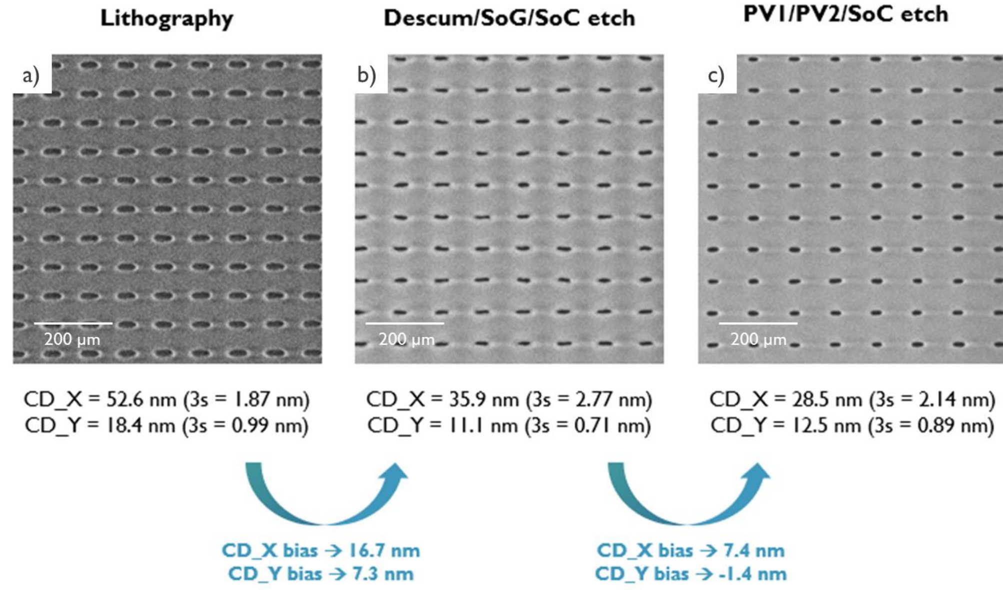

FIG. 3. Etch performance of the partitioned baseline etch recipe with CD_x and CD_y a) post lithography, b) post mask etch , and c) post low-κ etch with strip. CD shrink of both dimensions for each etch step is also noted below in blue.

2. *Fine-tuning of the etch chemistry*

Etch shrinkage has been attempted by modifying the etch chemistry either at the SoG or at the SoC level (Fig.4). Since both etch steps are polymer-heavy, the amount of the polymerization can be varied in two ways: 1) by altering the etch/passivation gas ratio or 2) by reducing the process temperature so that the passivation layer is more difficult to remove. Both approaches should result in an enhanced sidewall passivation, therefore more shrink. No modifications to SiO_2 or low-κ etch were done as doing so would affect the final via shape after the SoC strip.

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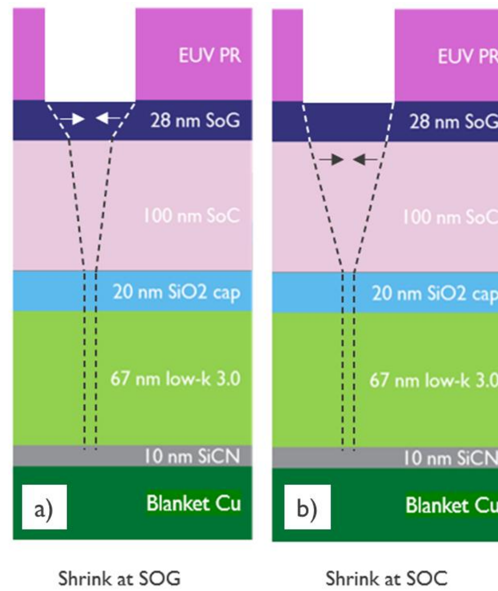

FIG. 4. Schematic etch profile resulting from shrinking either at the a) SoG or b) SoC level.

For the SoG etch, where the two main gases used are CF_4 and CHF_3, changes in -5/+5 sccm steps (less CF_4 / more CHF_3) have been attempted. Each -5/+5 sccm step will be denoted as “+1” SoG polymerizing condition. Similarly, for the SoC etch, increments by +5 sccm in the CH_4 flow have been tried. Each of such +5 sccm increments will be named “+1” SoC polymerizing condition. Similarly, temperature reduction by steps of 5° C for both SoG and SoC steps will be denoted as “-1” temperature condition.

3. *Liner-assisted shrink*

In addition to etch chemistry modifications, two different options of a liner-assisted shrink have been attempted (Fig.5). The first option is the organic liner deposited on PR directly after exposure and development. This liner is then opened with the standard

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N_2/H_2 descum step at the bottom of the contact hole while it remains on PR sidewalls, effectively providing extra shrink at the PR level. The other option is the SiO_2 liner deposited after SoG has been fully opened and SoC has been opened partially, just enough to remove PR from the wafer. The SiO_2 liner is then opened with a CF_4-based spacer etch step, similar to the SiO_2 etch performed further in this sequence. Deposition of the SiO_2 liner directly on PR has not been attempted due to the risk of collapsing liners at the PR sidewalls during the SoC etch, causing the PR to be removed.

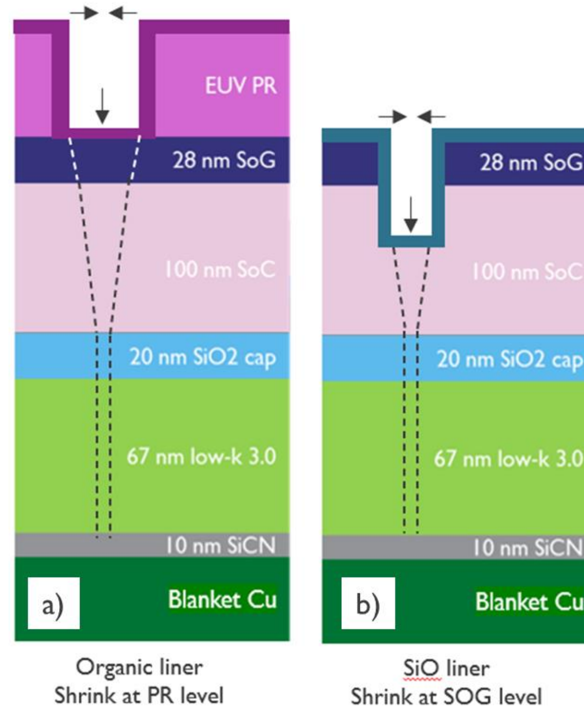

FIG. 5. Schematic showing the liner-assisted shrinkage, using the baseline etch recipe: a) organic liner deposited on PR directly after exposure and development, b) SiO_2 liner deposited on SoG, after partial etch into SoC has removed PR from the field.

4. Alternative etch of the mask (DCS)

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The final shrink option in this study has been to use the DCS (Direct Current Superposition) functionality during the mask etch. This feature allows for in-situ sputtering of Si atoms from the top electrode during the etch, which are then deposited on top of the photoresist, reducing its erosion. Moreover, electrons created during this process cure the resist simultaneously, further strengthening it. This functionality is known to improve the line edge roughness (LER) of lines or, as in the studied case, CDU of contact holes[11]. Since DCS is available in the TEL Vigus™ dielectric etch chamber and not in the TEL SCCM™ where the mask etch is normally done, the entire process had to be done in the TEL Vigus™ chamber. We will refer to it as to the 'alternative' etch, at two different process temperatures: the reference one, and the 5° C higher one, denoted as "Temp +1".

C. Metrology

All CDSEM measurements have been done on a Hitachi CG5000 tool. Two types of structures are investigated: Kelvin vias (KVA), with pitch x = 108 nm and y = 84 nm, as well as Fork-Fork structures (FF), with the same pitch in the x-direction but a two-times smaller pitch y, i.e. 42 nm (Fig.6).

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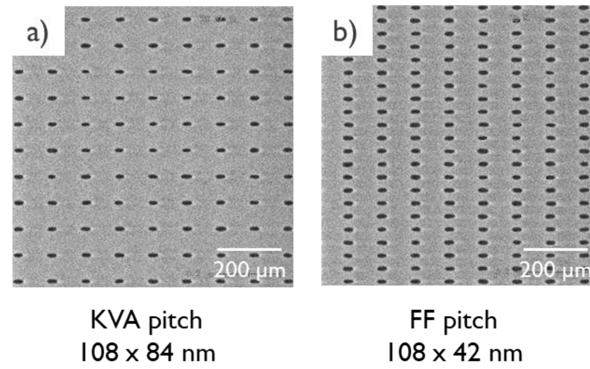

FIG.6 . Typical CDSEM pictures of both types of structures with different pitches studied in this paper: a) the KVA structure and b) the FF structure.

The total amount of KVA (FF) vias measured is 70 (140) per die, or 10500 (21000) per wafer, as the full wafer map of 150 dies is performed. Both structures serve different electrical purposes if connected to M2 and M3 lines, but for this study they will simply represent two different pitches. Investigation of both types of structures allows to assess any potential impact of semi-isolated vs dense loading on the etch performance. Numerical analysis with Fractilia MetroLER software is performed on the data, which allows to discard incorrectly measured features. Global and local CDU, as well as the fraction of missing vias will be also presented.

In addition to CDSEM data, large scale VC (Voltage Contrast) defectivity measurements have been performed on an HMI eP5 tool. During this inspection, the e-beam scans the wafer and creates secondary electrons of varying intensity, when the e-beam lands on a via or not. A via is classified as a 'defect' if its brightness is less than 70 % of a reference brightness (Fig.7). Since smaller vias may yield weaker VC signal even if they land on SiCN correctly, the result is treated mostly qualitatively and, in most cases, will be used to assess the spatial distribution of defects around the wafer and to

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supplement the fraction of missing vias calculated by Fractilia MetroLER. The total amount of KVA (FF) vias measured with the VC method is over 6000 (13000) per die, or over 900 k (1.9 M) per wafer.

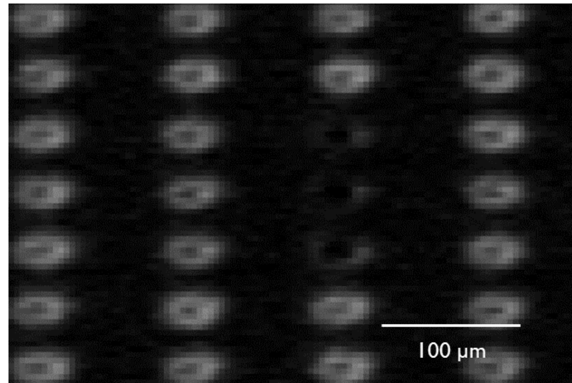

FIG. 7. Zoom of a typical VC picture of the FF array, showing three vias classified as defects due to the reduced signal intensity.

Finally, the study is complemented by Transmission Electron Microscopy (TEM) images. It is important to mention that during the TEM inspection, the low-κ material shrinks and deforms significantly by the e-beam (unlike the SiO_2 on top) which makes the CD measurement unreliable. Therefore, TEM images will be used to qualitatively confirm whether vias are correctly landing on the SiCN below, not for any CD or profile analysis. Such quantitative analysis can be done only if structures are filled with metal, which will be shown only for the fully integrated case at the end of this paper.

III. RESULTS AND DISCUSSION

A. Results and scorecard

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Table I summarizes all results of this study. Wafer 1 is the **process of reference (POR)**. Wafers 2 and 3 have been processed with the **SoG polymerizing conditions** +1 and +3. The SoG etch is the most straightforward parameter to tune[4], since the SoC layer below that would be potentially impacted by these modifications will be stripped afterwards anyway. The +1 condition shows a very small shrink and minimum impact on the defectivity. Due to this very small variation, the +2 condition has been skipped and the +3 condition has been applied next. This +3 condition shows the CD being close to the 10.5 nm target, but the CDU, LCDU and defectivity are significantly worse, with up to 0.2 % of vias missing. In all cases studied, we find that such defectivity occurs at the wafer edge due to excessive polymerization there (Fig.8).

TABLE I. CD, global CDU, LCDU, fraction of missing vias and VC defectivity study of both KVA and FF structures for all etch iterations performed in this study. The green-to-red scale represents values from best to worst for each specific parameter. White CD values represent CD below target or absence of results (wafer 15). VC values of *20000* denote saturation of the defect count and the real number may be much higher.

		MetroLER post etch								Defects	
		KVA				FF				KVA	FF
		CD nm	CDU nm	LCDU nm	miss %	CD nm	CDU nm	LCDU nm	miss %	defects VC ep5	
1	POR	13.1	2.87	2.51	0	13.5	2.67	2.47	0	416	821
2	SOG Polymer +1	12.7	2.78	2.49	0	13.3	2.73	2.49	0	510	1065
3	SOG Polymer +3	10.3	3.94	3.41	0.22	10.9	3.73	3.26	0.11	6867	8517
4	SOG Temp -1	12.5	2.66	2.44	0	13	2.64	2.42	0	451	2080
5	SOG Temp -2	10.9	3.08	2.72	0	11.4	2.97	2.61	0	1530	1949
6	SOG Temp -3	9.66	4.56	3.33	0.38	9.85	4.92	3.37	0.6	15386	*20000*
7	SOC Polymer +1	11.6	2.87	2.63	0	12	2.86	2.58	0	785	1138
8	SOC Polymer +2	10.1	2.9	2.64	0	10.5	3	2.65	0	6542	*8901*
9	SOC Temp -1	13.1	2.63	2.26	0	13.6	2.57	2.3	0	551	1614
10	SOC Temp -2	11.8	4.64	4.47	0.66	12.5	4.11	3.94	0.45	29240	*20000*

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11	1st org liner	11	3.1	2.8	0	11.7	2.86	2.51	0	2084	2027
12	2nd org liner	10.5	3.6	3.35	0.13	11.6	2.92	2.58	0	5957	2538
13	1st SiO liner 4nm	12.2	3.02	2.26	0	12.8	3.02	2.36	0	1019	2004
14	1st SiO liner 5nm	8.82	4.87	3.86	0.44	9.81	4.26	3.49	0.06	24543	*20000*
15	+50% liner etch	8.12	4.97	3.9	1.29	8.66	4.8	3.44	0.47		
16	2nd SiO liner 2nm	11.7	2.79	2.26	0	12.4	2.58	2.29	0	730	1943
17	2nd SiO liner 3nm	12.4	3.56	2.79	0	12.9	3.63	3.03	0	1026	2794
18	Alt. recipe	8.5	2.44	2.16	0.05	9.31	2.09	1.71	0.01	10098	7767
19	Alt. recipe Temp +1	10.2	2.13	1.97	0.01	10.9	1.86	1.63	0	1984	2700

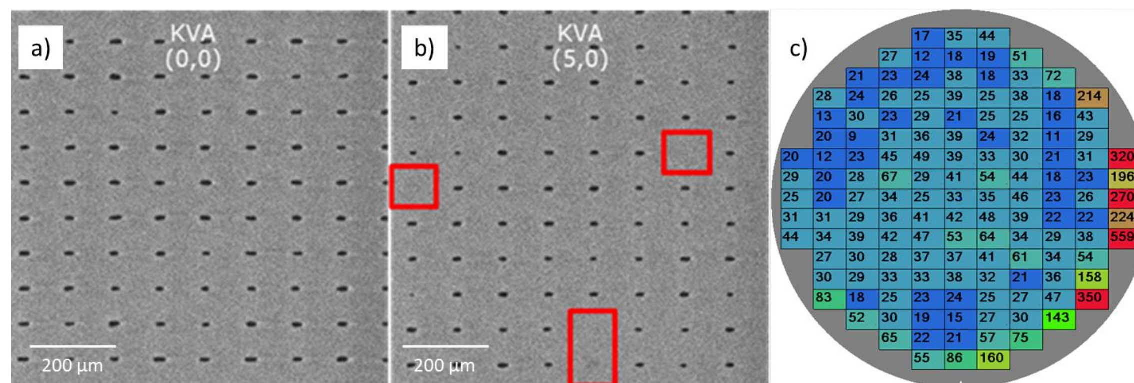

FIG. 8. KVA vias a) in the wafer center and b) at the edge, with missing vias highlighted in red. c) VC defectivity map of the wafer. This dataset corresponds to wafer 3, but this behavior is representative for the other cases with higher defectivity.

Since wafer 3 shows the CD on target, no further shrink has been attempted with the more polymerizing etch chemistry, and the **SoG temperature conditions** -1, -2 and -3 have been tried on wafers 4, 5 and 6. One can see that the -1 condition results in little shrink and a small improvement of CDU/LCDU. The -2 condition yields the CD almost on target and no missing vias, while the defectivity degrades by up to 0.3 nm. The -3 condition results in vias below target and very high defectivity. Nevertheless, for the SoG

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etch step, the temperature reduction results in less defectivity than the altered gas concentration.

Wafers 7 and 8 have been processed with the **SoC polymerizing conditions** +1 and +2. While the +1 condition already shows a significant shrink and small impact on defectivity, the +2 condition results in excellent etch performance: the CD being on target, no missing vias and low CDU, even better than the one obtained from wafer 5.

The **SoC temperature conditions** -1 and -2 have been tried on wafers 9 and 10. While the -1 condition shows reduced defectivity and no shrink, the -2 condition allows to shrink the features slightly, but at a very high defectivity cost. This approach for the SoC etch step is therefore significantly less effective than the altered gas concentration.

Table II is the expanded version of Table I for the experiment with **liner-based approaches**, in which the metrics after the liner deposition are shown in addition to final results. Two types of **organic liner** have been tried on wafers 11 and 12. Post-deposition results for these two wafers are almost identical, with a CD reduction of 3 nm and (except for KVA CDU) a reduction in CDU and LCDU. This is attributed to the smoothening properties of the liner deposited on the photoresist. After the etch, both options results in the CD very close to the 10.5nm target, especially for the KVA structure, which is printed around 1 nm smaller ADI. Both organic liner options show relatively small degradation after the etch, with results comparable to the best cases described beforehand, i.e. wafers 5 and 8.

TABLE II. The expanded version of Table I showing via metrics after liner deposition, i.e. before etch. The POR (process of reference) condition has no liner deposited and the

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values shown correspond to ADI, i.e. reference without any liner. Note that there is almost 1 nm ADI CD difference between KVA and FF structures, as seen for the POR wafer.

		MetroLER post deposition								MetroLER post etch							
		KVA				FF				KVA				FF			
		CD nm	CDU nm	LCDU nm	miss %	CD nm	CDU nm	LCDU nm	miss %	CD nm	CDU nm	LCDU nm	miss %	CD nm	CDU nm	LCDU nm	miss %
1	POR	20.3	2.18	2.1	0	21.1	2.06	2.04	0	13.1	2.87	2.51	0	13.5	2.67	2.47	0
11	1st org liner	17.1	2.24	2	0	18.7	2.01	1.93	0	11	3.1	2.8	0	11.7	2.86	2.51	0
12	2nd org liner	17.2	2.21	2	0	18.7	2.01	1.92	0	10.5	3.6	3.35	0.13	11.6	2.92	2.58	0
13	1st SiO liner 4nm	12.5	6.39	6.25	0.02	13.4	4.54	4.38	0.01	12.2	3.02	2.26	0	12.8	3.02	2.36	0
14	1st SiO liner 5nm	9.38	2.53	2.24	0	10.6	3.02	2.7	0	8.82	4.87	3.86	0.44	9.81	4.26	3.49	0.06
15	+50% liner etch									8.12	4.97	3.9	1.29	8.66	4.8	3.44	0.47
16	2nd SiO liner 2nm	11.8	2.12	2.04	0	12.7	2.39	2.29	0	11.7	2.79	2.26	0	12.4	2.58	2.29	0
17	2nd SiO liner 3nm	11.3	2.5	2.23	0	12.4	2.89	2.63	0	12.4	3.56	2.79	0	12.9	3.63	3.03	0

Unlike the organic liner, the **inorganic liner** deposited on top of SoG turned out to be more challenging. The first type of the SiO_2 liner, when deposited nominally 4 nm (wafer 13), has shown promising shrink and LCDU reduction after etch, despite apparent high defectivity after the deposition (possibly wafer contamination). However, increasing its thickness to 5 nm (wafer 14), resulted in many defects and CD below the 10.5 nm target, despite promising results after the deposition. To avoid the possibility that the liner opening was too short, a 50% longer liner etch has been tried on wafer 15. As seen from the table, there is no improvement with this approach.

The second type of the SiO_2 liner (2 nm on wafer 16), has shown improved CDU and LCDU despite the CD above target. However, when the 3 nm liner has been tried on wafer 17, all the metrics turned out to be worse, despite all vias still being open. Due to

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constraints on the experiment, the inorganic approach has been discontinued due to lack of promising results.

The final shrink option tested in this study is the **alternative etch**, incorporating the DCS functionality. Wafer 18 shows that while the initial process results in the CD well below target, the CDU and LCDU are significantly better than the POR process, which is attributed to both the resist cure and the Si deposition on top of it, thanks to the DCS functionality. The same process repeated at higher temperature of SoG and SoC steps on wafer 19 shows the result being on target and the best metrics among all wafers in this study. It is interesting to note that unlike in a recent study[5], the DCS functionality turned out to perform a bit worse than the liner-based approach.

B. TEM results and application on the fully integrated loop

Since CDSEM inspection probes the topmost layers of the wafer, it cannot guarantee that vias are correctly open at the bottom. Therefore, for the most promising conditions (wafers 5, 8, 11, 12, 18 and 19) TEM inspections have been performed. Fig. 9 shows that for all these cases vias indeed land correctly. Note that, unlike SiO_2, the lowk material is known to shrink significantly under the electron beam. Therefore, mid-height parts of lowk which are not held by stronger materials, (i.e., the SiO_2 above and SiCN below) are prone to shrinkage, which creates the impression of bulging. For the same reason, the shape is different at the SiO_2 level, and it is expected that it is also straight in lowk. However, the only way to definitely confirm the profile would be to fill the via with metal before the inspection. Unfortunately, this is not possible directly after via etch due to high aspect ratio of the structure.

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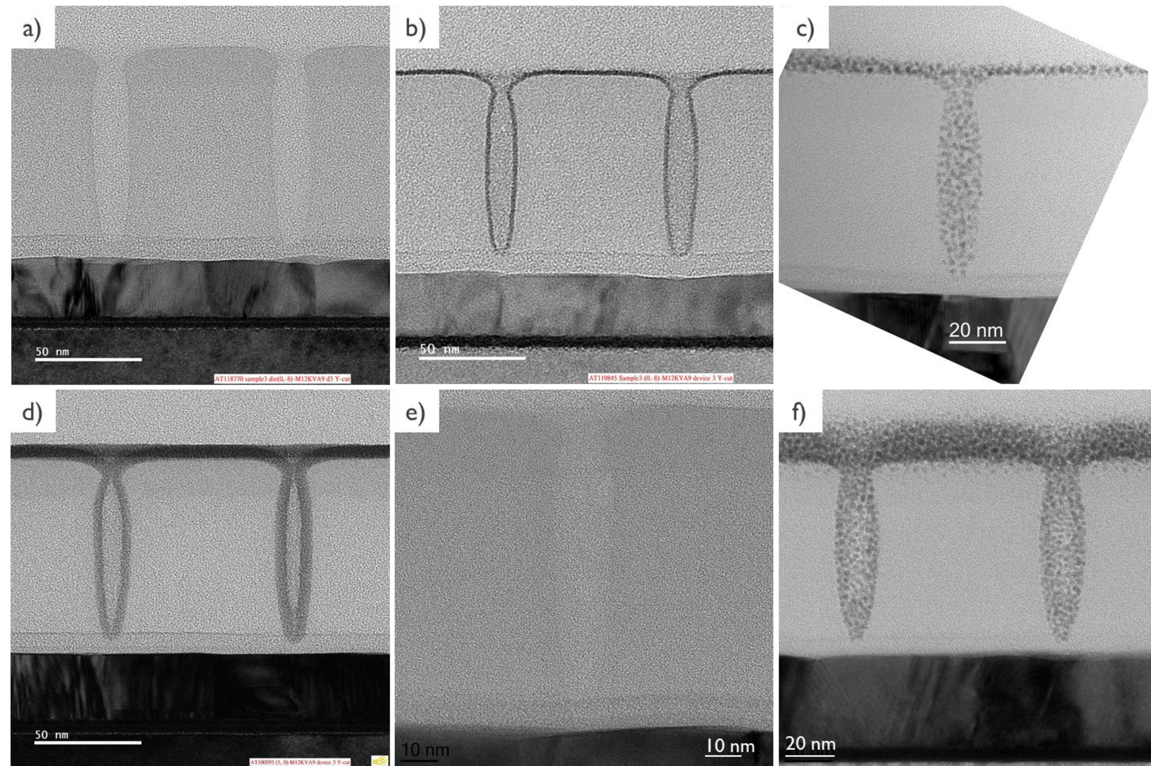

FIG. 9. TEM inspections of KVA structures for selected wafers: a) 5, b) 8, c) 11, d) 12, e) 18, f) 19. Only wafer edge locations are shown for clarity, but inspections in the wafer center are identical.

Since condition 19 is the most promising one, it is this one that has been selected to be applied on a fully integrated loop with M2, V2 and M3. Fig. 10 shows that this via etch condition works well if M3 TiN hard mask lines are present. If the final CD (after M3 trench etch, TiN removal and the dual damascene metallization) at the via bottom is compared to the POR process, we observe a significant 5 nm reduction with the new process. However, the final bottom CD of around 15 nm is ultimately higher than the 10.5 nm target. This is due to erosion of via corners during the M3 trench etch which results in chamfer and the sloped via profile. Moreover, some of the low-κ material is

consumed during the metallization process itself. These two issues are outside the scope of this study and will be addressed separately in the future. However, while the trench-first-via-last approach would certainly improve the chamfering issue, we observe that the impact on electrical measurements is significantly lower with the current approach[10], as trenches exposed to via patterning and cleans are not patterned yet. Moreover, while the excessive chamfer is obviously not desirable, a small chamfer allows to metallize the via more easily.

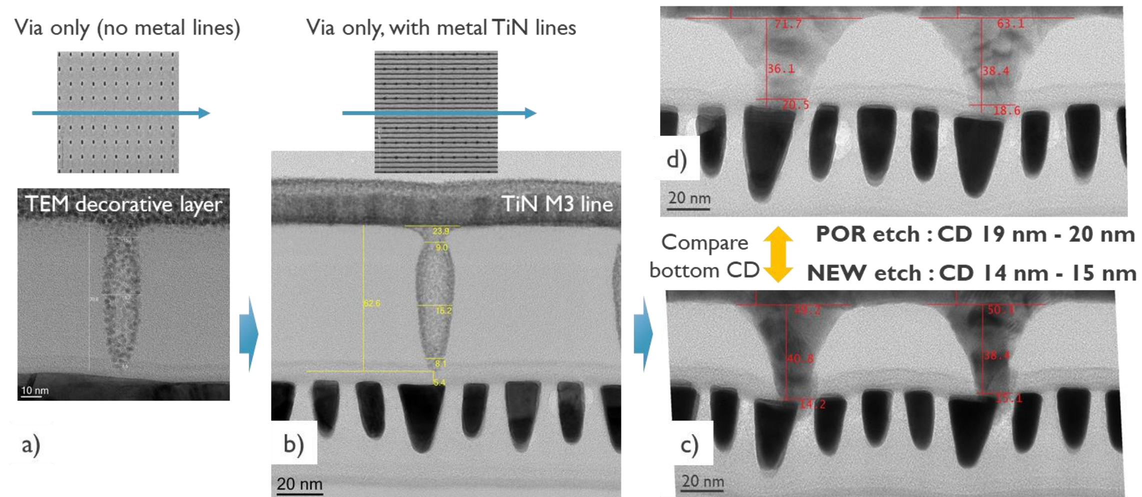

FIG. 10. a) TEM and CDSEM of the short loop wafer 19 (best condition), along with the direction of the TEM cut indicated. b) The same best etch condition applied on a full loop wafer, with M2 and M3 TiN lines patterned. c) The same full loop wafer after M3 trench etch, TiN strip and metal fill, compared to d) the POR process (same as wafer 1) at the same step.

The final comment is whether the Edge Placement Error (EPE) budget allows the presented Via-to-Metal connection to still yield. In this case, the 'yield' is defined by passing the Time Dependent Dielectric Breakdown (TDDB) electrical test. While

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experimental TDDB data is not available, our simulations[12] show that this distance is 6 nm, therefore three times higher than the CDU/LCDU obtained with the best method presented in the paper. With the CD increasing by 4 nm after the metal fill (2 nm on each side), EPE is reduced to 4 nm, still twice more than LCDU. Note that LCDU post metal fill cannot be measured, but it's expected to be lower due to larger CD.

IV. SUMMARY AND CONCLUSIONS

In summary, we have attempted to shrink contact holes down to CD_y 10.5 nm, while maintaining low CDU, LCDU and defectivity. Several attempts using gas ratio and temperature modifications to SoG and SoC etch steps have been tried, with two most promising conditions identified as the SoG step temperature reduction and the more polymerizing gas ratio for the SoC step. Organic liner deposition on top of the photoresist also turned out to be a good candidate, unlike a few SiO_2 liner options deposited on top of the SoG layer. Ultimately, it is the DCS functionality which, due to PR curing and protection capabilities, allowed to reach the target CD while further reducing CDU and LCDU, even below POR values. While all the promising candidates were screened with TEM to make sure that vias are correctly open at the bottom, it is the best DCS condition that has been tried on a full loop wafer. The final result, post dual damascene metallization, shows that the bottom CD at the interface with the metal below is significantly reduced with respect to the POR process. On the other hand, the final post-metallization CD is still larger than target, but this is attributed to consecutive processing steps in the flow.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon a reasonable request.

AUTHOR DECLARATIONS

The authors have no conflicts to disclose.

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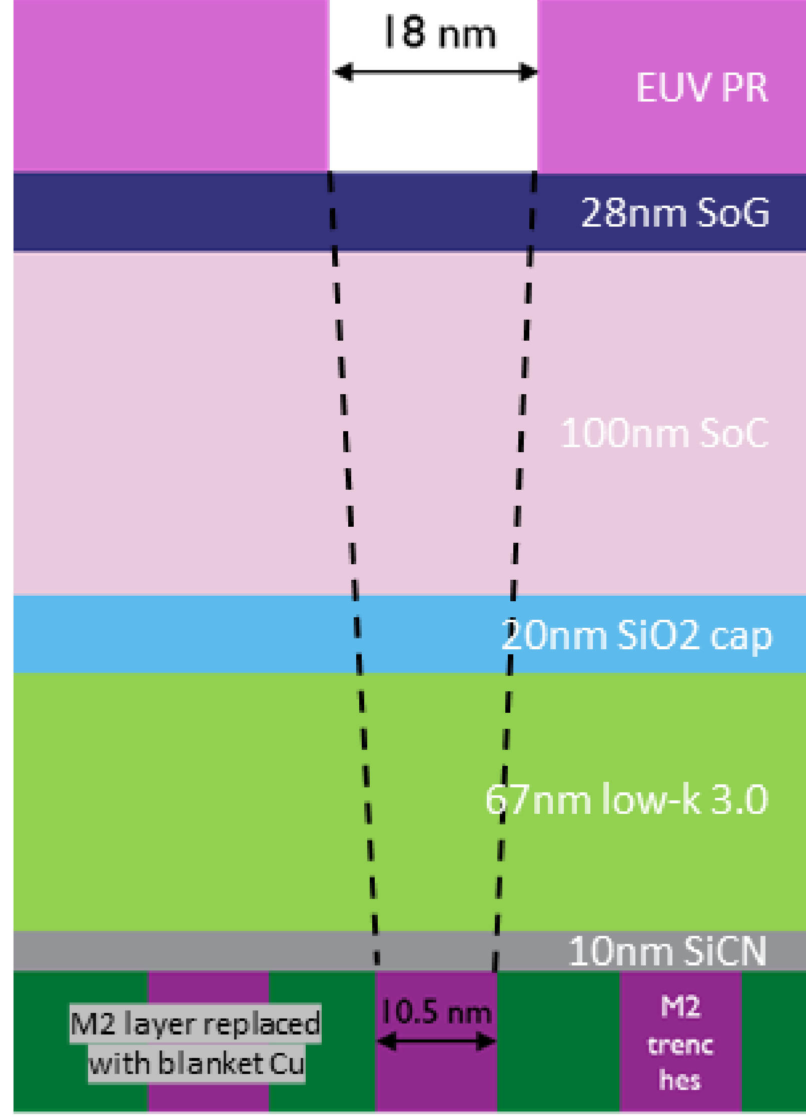

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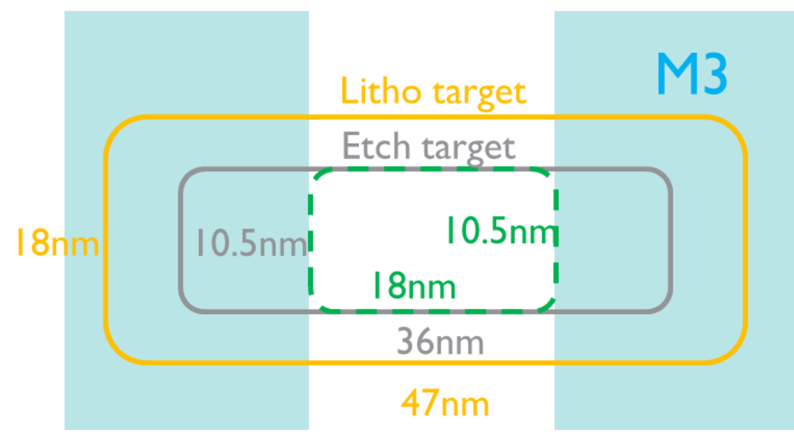

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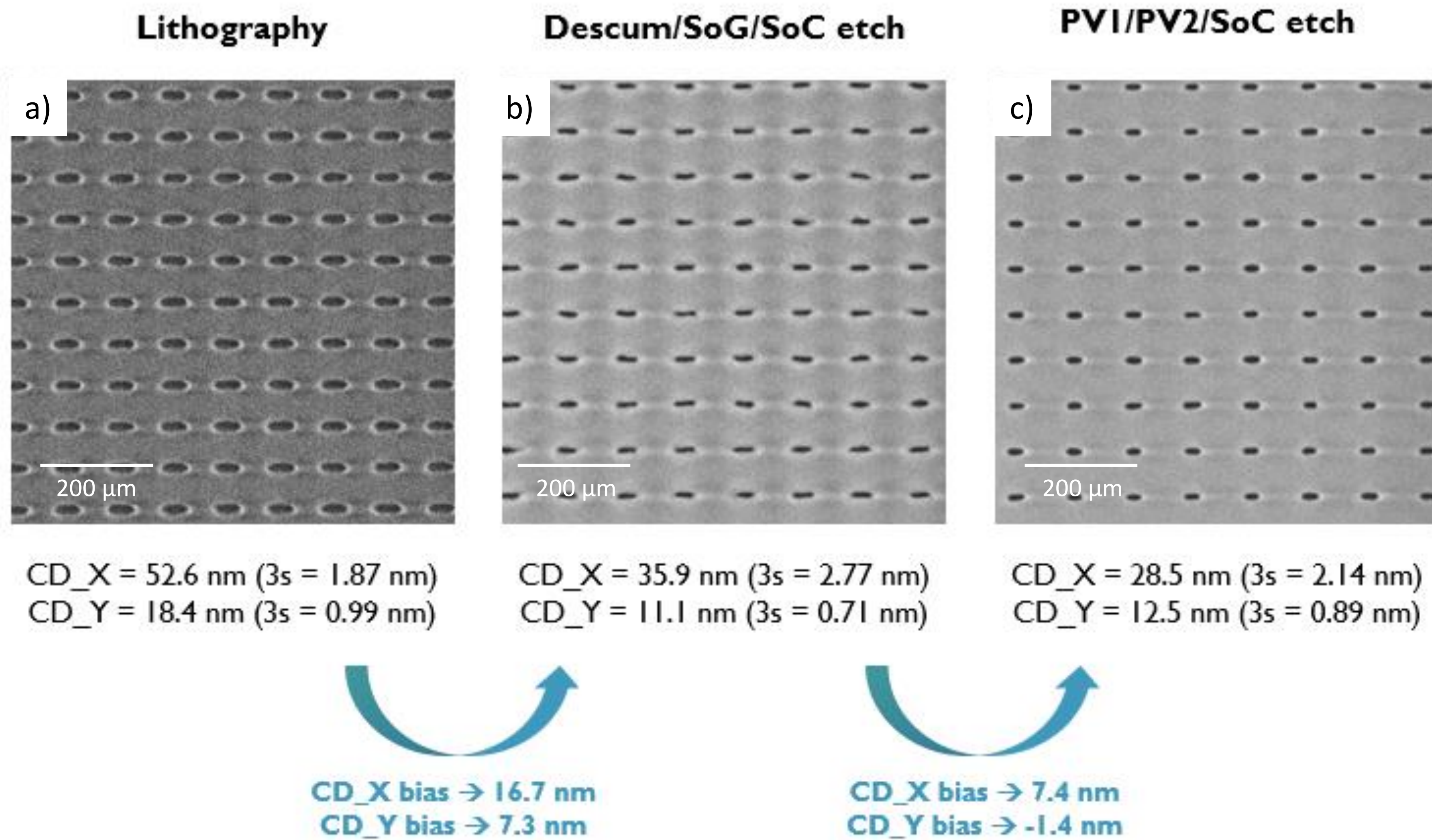

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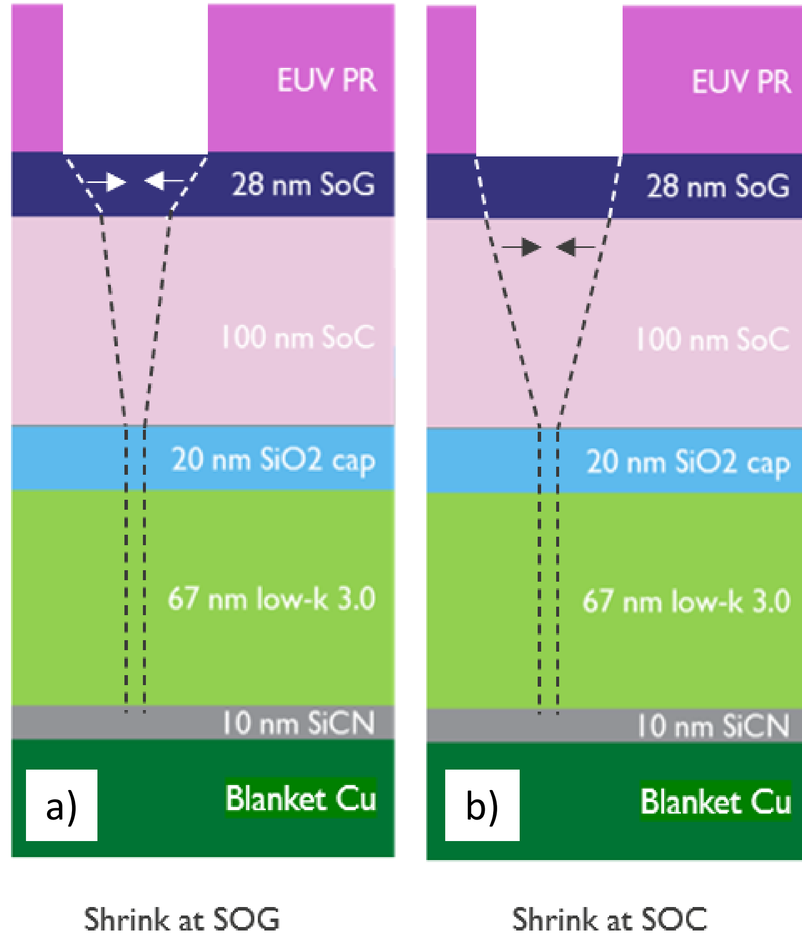

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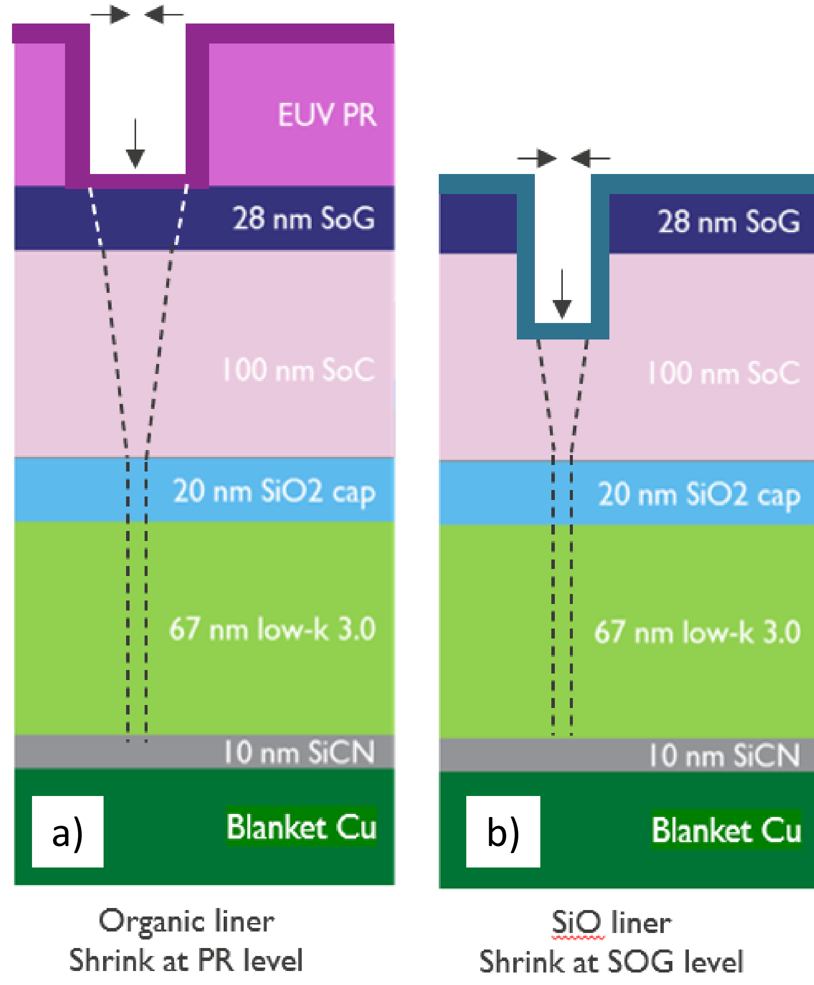

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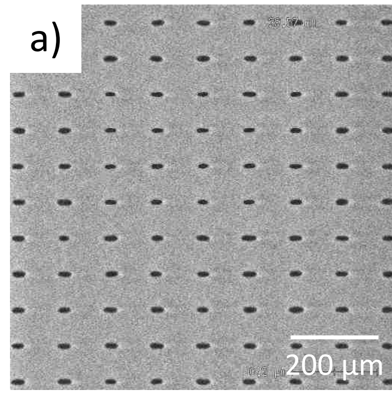
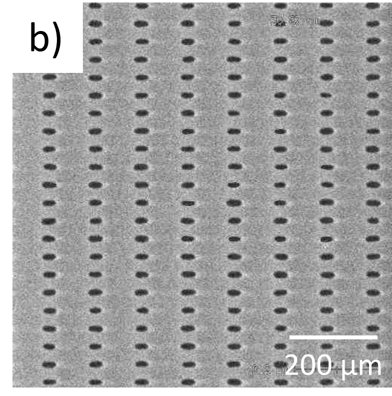


KVA pitch
108 x 84 nm



FF pitch
108 x 42 nm

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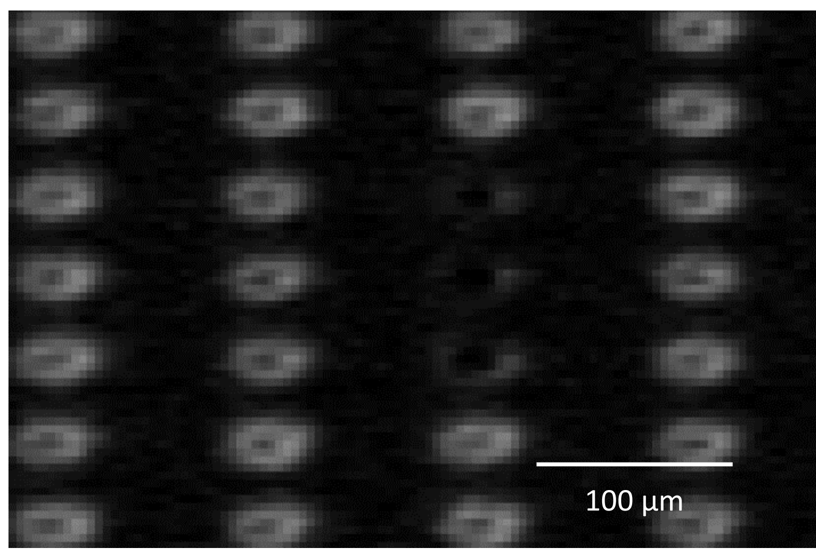

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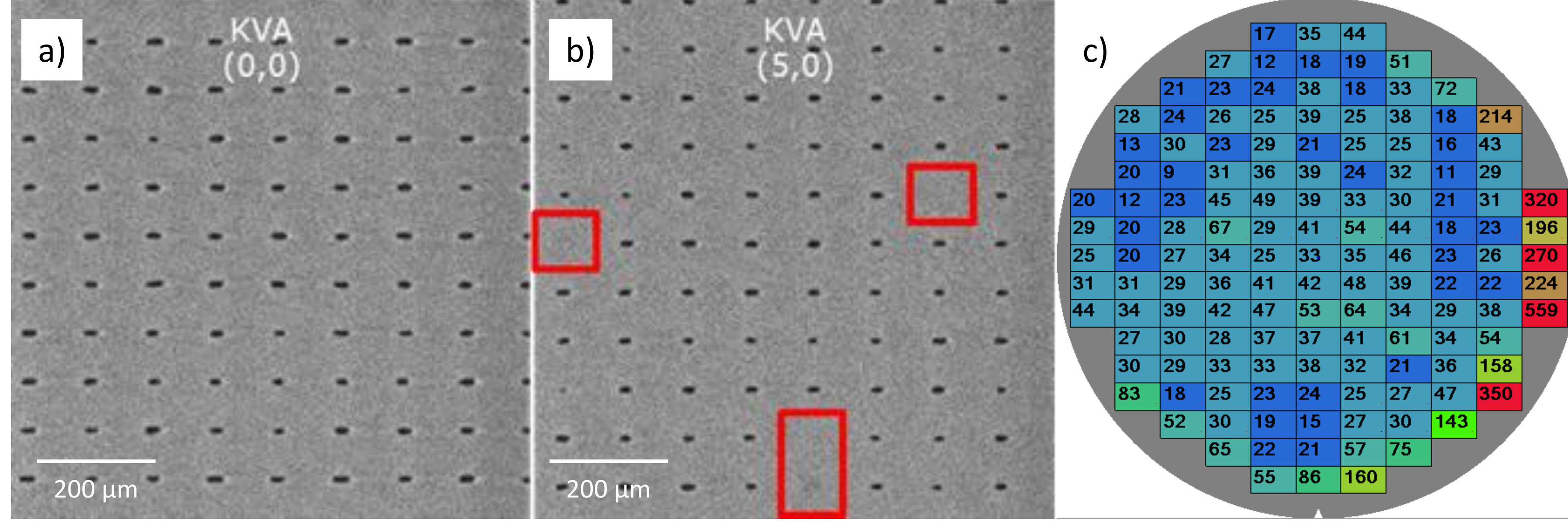

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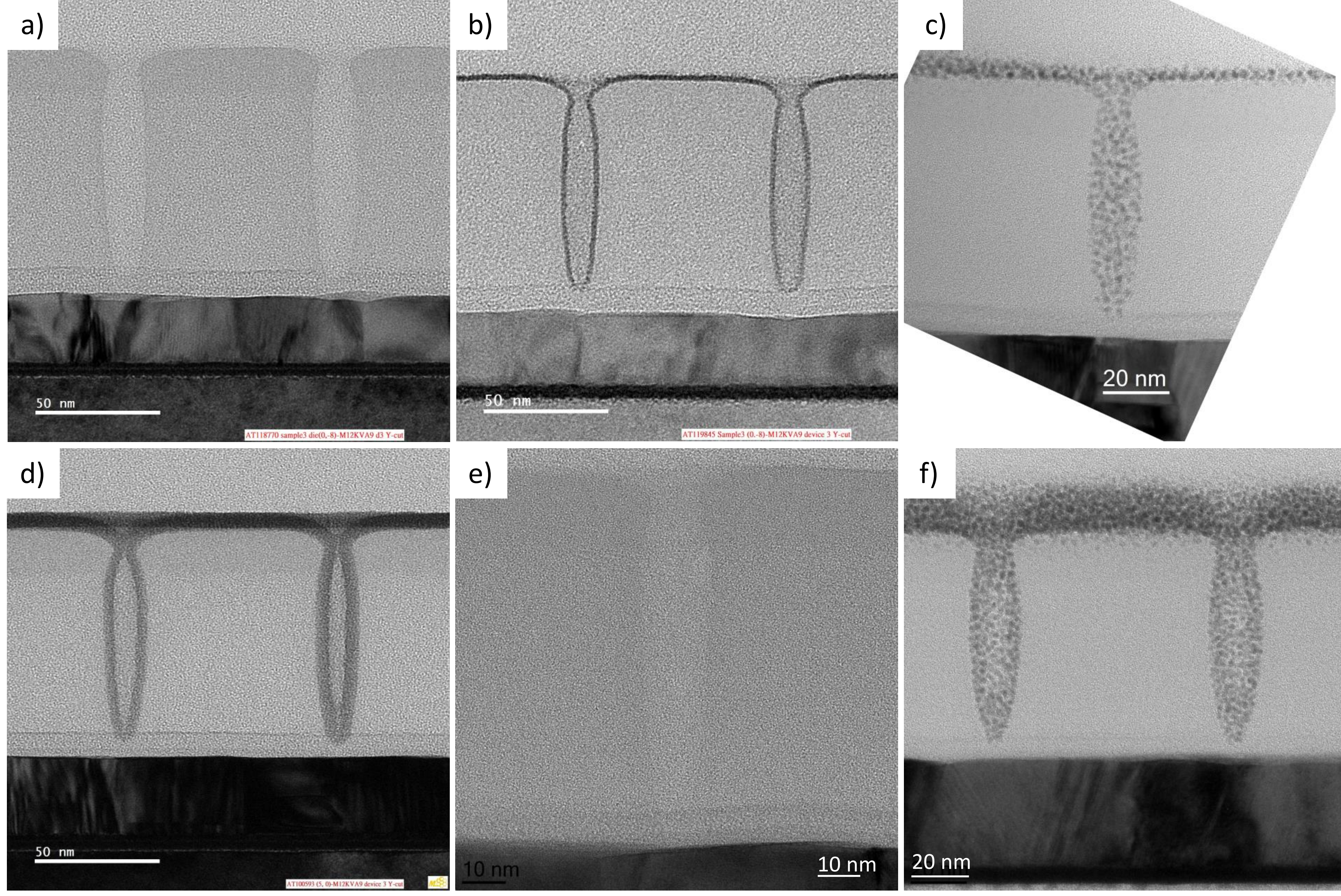

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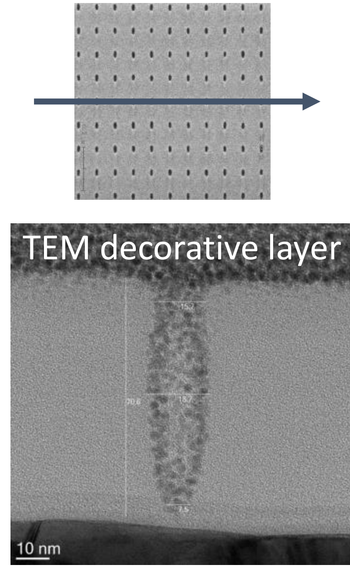
Via only (no metal lines)



a)

Via only, with metal TiN lines