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Building blocks of a flip-chip integrated superconducting quantum processor

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Supplementary material for this article is available [online](#)

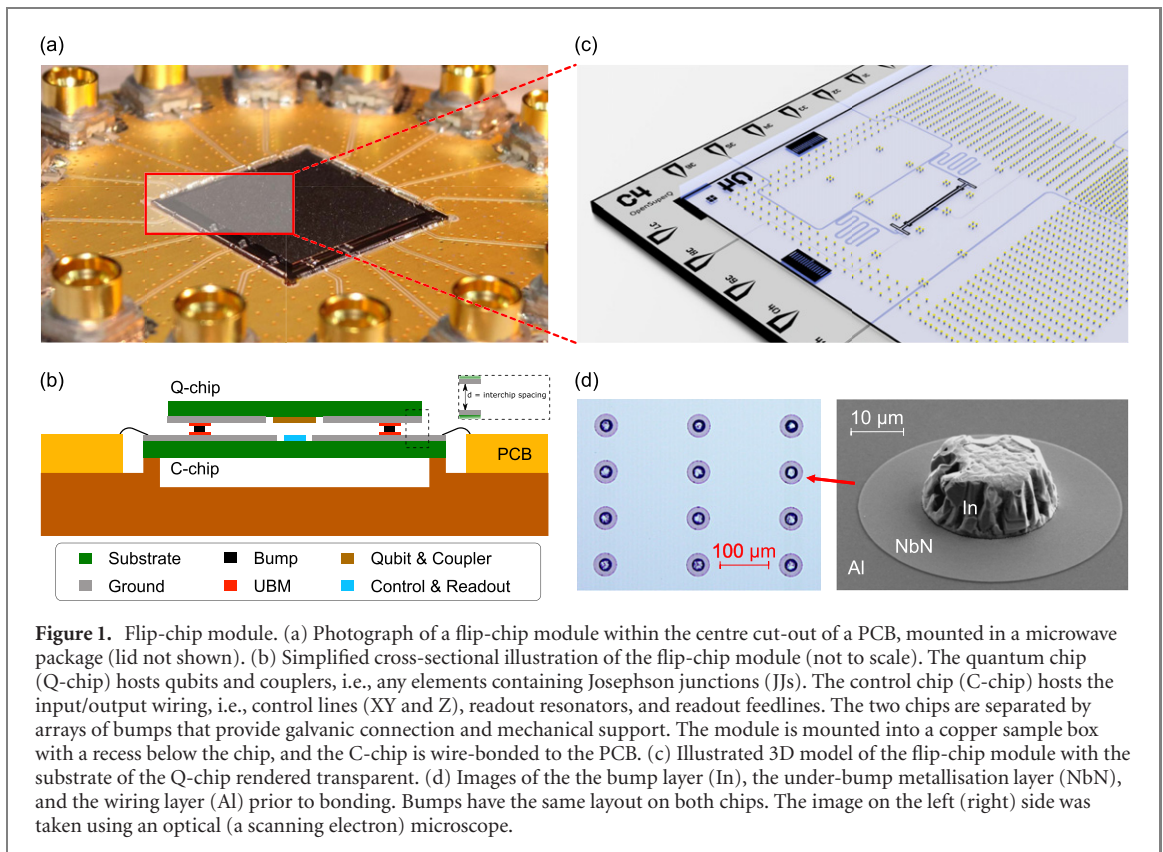
Abstract

We have integrated single and coupled superconducting transmon qubits into flip-chip modules. Each module consists of two chips—one quantum chip and one control chip—that are bump-bonded together. We demonstrate time-averaged coherence times exceeding 90 μ s, single-qubit gate fidelities exceeding 99.9%, and two-qubit gate fidelities above 98.6%. We also present device design methods and discuss the sensitivity of device parameters to variation in interchip spacing. Notably, the additional flip-chip fabrication steps do not degrade the qubit performance compared to our baseline state-of-the-art in single-chip, planar circuits. This integration technique can be extended to the realisation of quantum processors accommodating hundreds of qubits in one module as it offers adequate input/output wiring access to all qubits and couplers.

1. Introduction

The realisation of superconducting quantum processors with arrays of increasing numbers of qubits faces several interesting engineering and physics challenges [1–3]. From the hardware perspective, scaled-up circuit designs and fabrication processes must not degrade the device performance, which otherwise would adversely affect the fidelity of quantum algorithms. This already becomes non-trivial at the scale of dozens of interconnected qubits, which requires intricate routing of the input/output microwave circuitry.

In conventional devices fabricated on a single chip, one approach to routing signal lines is to implement signal crossovers using superconducting air-bridges [4–6]. Furthermore, to minimise signal crosstalk, transmission lines can be enclosed in elongated ‘tunnels’, which connect the ground planes on either side of the lines [4]. While feasible in small-scale circuits, these techniques alone seem insufficient for scaling up further. Monolithic integration, featuring buried multi-layer superconducting wiring, is an appealing solution [7]; however, this technology has not been demonstrated in coexistence with high-performance superconducting qubits.



Two other scalable 3D-integration approaches are multi-chip (flip-chip or interposer chip) circuits and out-of-plane wiring [1, 2, 8–16]. Both approaches have the advantage that the chip hosting the quantum circuitry can be fabricated separately, with minimal extra processing that risks degrading qubit performance.

Multi-chip implementations [1, 2, 8–12] typically separate the quantum and the input/output wiring circuitry onto different chips. These chips are then connected to each other in a multi-chip module by flip-chip bump-bonding techniques. This enables flexible signal routing from the perimeter of the wiring chip to the capacitive, inductive, or galvanic point of contact with the quantum chip. Combined with superconducting through-silicon-via technology for grounding and signal routing [17], this technique would enable higher-density wiring with connections from the entire back plane of the wiring chip, rather than solely from the perimeter.

Out-of-plane wiring implementations eliminate the need for multiple chips, but instead deploy, e.g., spring-loaded [13–15] or coaxial [16] pins that approach the chip perpendicularly. Such implementations yield direct access to components within the two-dimensional qubit array, obviating the need of routing from the edges of the chip.

In this paper, we demonstrate superconducting quantum devices in a scalable architecture by integrating them into a flip-chip module comprised of two silicon chips, which we denote as the control (C) chip and the quantum (Q) chip, see figures 1(a)–(c). The device consists of fixed-frequency aluminium transmon qubits and a flux-tunable parametric coupler on the Q-chip. These components are capacitively and inductively coupled to the control lines (XY and Z, respectively) and qubit-readout resonators located on the C-chip. The attained qubit performance is near the state of the art for flip-chip devices. We characterise single-qubit and two-qubit (CZ) gates with average fidelities of 99.97% and 98.66%, respectively. The measured average T_1 relaxation time in single-qubit devices is as high as 110 μs , which, notably, is not degraded compared to our baseline single-chip devices [18–20] and comparable to state-of-the-art 3D-integrated devices reported by other groups [1–3, 9, 11, 21–23]. Moreover, we discuss device parameter sensitivities due to variations in the interchip spacing.

2. Design and simulation workflow

The design process of the devices in this work typically begins by determining the target parameters at the Hamiltonian level (qubit and coupler $|0\rangle$ -to- $|1\rangle$ transition frequencies f_{01} , anharmonicities α , readout

frequencies f_c , coupling rates g , Purcell-decay limit T_p , etc). These target parameters are chosen to be similar to those of our standard single-chip devices [19]. This comparison enables us to benchmark flip-chip device performances, and also validate the accuracy of the device simulation and fabrication processes.

Next, we employ ANSYS—a finite element electromagnetic simulation software suite—to find the right geometry that corresponds to the target parameters [24]. Specifically, the ANSYS HFSS eigenmode solver is used to predict resonator frequencies, while the ANSYS Maxwell electrostatic solver is used to determine capacitance values between the various elements. In the simulation software, the model consists of two silicon (Si) chips that are facing each other, similar to the model shown in figure 1(b). The chips are separated by the interchip spacing d . The metallic layer of each chip is represented by a planar sheet (zero thickness) located directly on the surface of each chip. The sheet is then given the appropriate boundary condition (for eigenmode simulations) or excitation mode (for electrostatic simulations). We typically aim for a convergence criterion below 0.5% for both solvers [see section 2 of the supplementary materials (<https://stacks.iop.org/QST/7/035018/mmedia>) for more details].

In practice, variations in the interchip spacing d introduced by the flip-chip bonding process leads to deviations from the target device parameters. To understand the extent to which these would affect the device parameters, we first build a simulation model with a target interchip spacing (here $d_{\text{target}} = 8 \mu\text{m}$). Next, two additional simulations are performed for $d = d_{\text{target}} \pm 1 \mu\text{m}$, i.e., 7 and 9 μm . This leads to a range of device parameters that can be compared with the target parameters. In addition, this enables us to anticipate changes in device parameters—caused by variations in d —that can lead to degraded device performance. For instance, the increase in the coupling strength between a qubit and its readout resonator when $d < d_{\text{target}}$ may lead to a Purcell-limited qubit T_1 . In such a case, we will target lower coupling strength at $d_{\text{target}} = 8 \mu\text{m}$ so that the qubit is not Purcell-limited for a smaller d (at least when $d > 7 \mu\text{m}$). Section 5.2 will discuss in more details the sensitivity of various parameters to variations in d .

3. Fabrication

The device fabrication is based on our standard qubit process at Chalmers [150 nm-thick aluminium (Al) on 280 μm -thick high-resistivity intrinsic Si] [18, 19]. The quantum (Q) and control (C) chips are connected together into a module by bump-bonding a pattern of compressible pillars of superconducting indium (In). This provides mechanical interchip separation and galvanic connection to their respective ground planes. Indium has been shown to be compatible with superconducting qubit fabrication processes [8, 25]. An under-bump-metallisation (UBM) layer of superconducting NbN separates the Al film and In pillars. The UBM is meant to act as a diffusion barrier that prevents the formation of an Al–In intermetallic state [26] and to protect the Al film from corrosion during bump fabrication. The bumps and UBM are shown in figure 1(d).

At Chalmers, we fabricated two 2 inch wafers, one containing four C-chips (14.3 mm \times 14.3 mm) and the other containing four Q-chips (12 mm \times 12 mm). First, an Al film was deposited on both wafers by e-beam evaporation. Second, the UBM pads were deposited in a process comprised of sputtering of a 50 nm-thick NbN film on patterned resists followed by liftoff. Thereafter, the wiring layer was etched out of the Al film. As a final step, the JJs were fabricated on the Q-wafer [18].

At VTT, In pillars on both wafers were formed by evaporation of a thick film (8 μm) on optically-patterned single-layer resist with a sidewall profile optimised for liftoff. After liftoff and dicing, individual chips were bonded into modules by compression at room temperature, creating superconducting electrical contacts between the chips without degrading the Al tunnel junctions and electrodes.

Again at Chalmers, the flip-chip modules were wire-bonded with Al wire to a printed circuit board (PCB) within an engineered, connectorised microwave package initially designed at ETH (see photograph in figure 1(a) and cross-section illustration in figure 1(b)).

4. Device characterisation

4.1. Interchip spacing, chip tilt, and transition temperatures

In this section, we report on the statistical analysis of the interchip spacing and chip tilt achieved in our flip-chip modules, and the superconducting transition temperatures of the materials comprising the flip-chip stack.

Deviations from the targeted interchip spacing d_{target} or non-zero tilt between the nominally parallel chip surfaces can occur due to slight variations in the bump-bonding process between different runs. We characterise these deviations non-destructively at VTT, using a scanning electron microscope, by measuring the distance z_i between the two surfaces at each of the four corners of the flip-chip module. The interchip

spacing d at the centre of each module is inferred from the average of these four values, i.e., $\bar{d} = (\sum_{i=1}^4 z_i)/4$. The chip tilt Δd is defined as the largest difference between z_i of any two corners, i.e., $\Delta d = \max(|z_i - z_j|)$ for $i \neq j$. The chip tilt angle $\Delta\theta$ is defined as the largest tilt angle measured between any two corners. Measurements of 17 flip-chip modules yield the following sample means and standard deviations: $\bar{d} = (7.8 \pm 0.8) \mu\text{m}$, $\Delta d = (1.7 \pm 1.0) \mu\text{m}$, and $\Delta\theta = (126 \pm 76) \mu\text{rad}$. We refer the reader to section 3.1 of the supplementary materials for more details.

Non-superconducting materials and interfaces in the flip-chip connections is a potential source of non-negligible Joule heating, especially when used for delivering inter-chip flux bias currents, which can be in the range of milliamperes. Using four-point probe measurements, we characterise the resistance of a daisy chain of 1200 bonded bump pairs, where each unit of the daisy chain consists of a planar interconnecting segment of Al and a pair of bonded In bumps with NbN UBM layers. In order to determine the superconducting transition temperatures T_c of the In bumps, we also characterise a separate daisy chain structure that omits Al and has NbN in the interconnecting planar segments. The T_c of NbN, In, and Al are observed near 12 K, 3.3 K, and 1.2 K respectively, indicating that all part of the stack are superconducting at millikelvin temperatures. Below approximately 1.2 K, we observe no resistance above the noise floor of the measurement system, which sets an upper bound of $\lesssim 50 \text{ n}\Omega$ per daisy chain unit. This measurement-setup-limited upper bound is comparable to the values reported in other works [8, 25]. Refer to section 3.2 of the supplementary materials for the plots of temperature-dependent resistance values for the different material stacks and more details about the measurement apparatus.

4.2. Control elements and gate fidelities

In this section, we demonstrate the high-fidelity single-qubit and two-qubit gates driven by the control elements on the C-chip. Figure 2(a) illustrates a flip-chip device containing two fixed-frequency transmon qubits and a frequency-tunable coupler on the Q-chip. They face the control elements (XY1, XY2, Z), readout resonators (readout 1, readout 2), and a feedthrough transmission line on the C-chip. The XY-line (or charge-line) is an open-ended coplanar-waveguide transmission line, capacitively coupled to the qubit (see the leftmost inset of figure 2(a)) and is used for driving qubit-state transitions. The Z-line (or flux-line) is a shorted loop, concentric with the coupler's superconducting quantum interference device (SQUID) axis (see the middle inset of figure 2(a)), and is used to provide static and alternating magnetic flux to parametrically modulate the coupler and drive two-qubit gates. The readout elements are quarter-wavelength ($\lambda/4$) transmission-line resonators that are capacitively coupled to the qubits (see the rightmost inset of figure 2(a)) and are also coupled to a feedthrough transmission line for multiplexed readout. The table in figure 2(b) contains a basic summary of the device parameters. More details can be found in section 4 of the supplementary materials.

We first demonstrate the functionality of the XY-line for coherent driving of the qubit. Figure 2(c) shows an oscillation in the first excited state population (P_1) of qubit 1 when a 20 kHz detuned Ramsey pulse sequence is applied via XY1 [27].

Next, we turn our attention to the Z-line. By varying the direct current applied to the line, we change the magnetic flux Φ_c threading the SQUID loop, which, in turn, changes the resonant frequency of the coupler ($f_c = f_{c0} \sqrt{|\cos(\pi\Phi_c/\Phi_0)|}$, where f_{c0} is the zero-bias coupler frequency, $\Phi_0 = h/2e$ is the flux quantum, h is the Planck constant, and e is the electron charge). When the coupler is tuned into resonance with the qubit, the two systems hybridise. This results in an avoided level crossing in the frequency spectroscopy data as shown in figure 2(d) for qubit 2, yielding the coupler–qubit coupling strength for qubit 2, $g_{q2,c} \sim 30 \text{ MHz}$. Similarly for qubit 1, $g_{q1,c} \sim 27 \text{ MHz}$.

We focus on one of the two-qubit gates natively available in our coupled system—the controlled-Z (CZ) gate—which implements a π phase shift on the joint qubit state $|q_1 q_2\rangle = |11\rangle$ and leaves the other computational states unchanged. The CZ gate is implemented by parametric modulation of the coupler frequency via the Z-line [28, 29]. It brings the state on a round trip from $|11\rangle$ to $|02\rangle$ and back (referred to as the CZ₀₂ transition in the energy diagram of figure 2(e)).

We bias the SQUID of the coupler at a non-zero flux offset (here, $\Phi_c = 0.34\Phi_0$), prepare both qubits simultaneously in the $|11\rangle$ -state (via XY1, XY2), apply a pulsed, alternating-current modulation to the Z-line, and measure the joint probability of the $|02\rangle$ -state (see the pulse sequence in figure 2(e)). By varying both modulation frequency and CZ-pulse duration, we observe the expected oscillation in the population of the $|02\rangle$ -state as shown in figure 2(e).

A common way to benchmark the performance of single-qubit and two-qubit gates is by performing randomised benchmarking (RB) experiments [30]. Reference RB experiments consist of the application of random Clifford sequences of varying lengths m to the qubits which have been prepared in an initial state (typically the ground state), followed by an inverting gate to create an overall identity operation (see

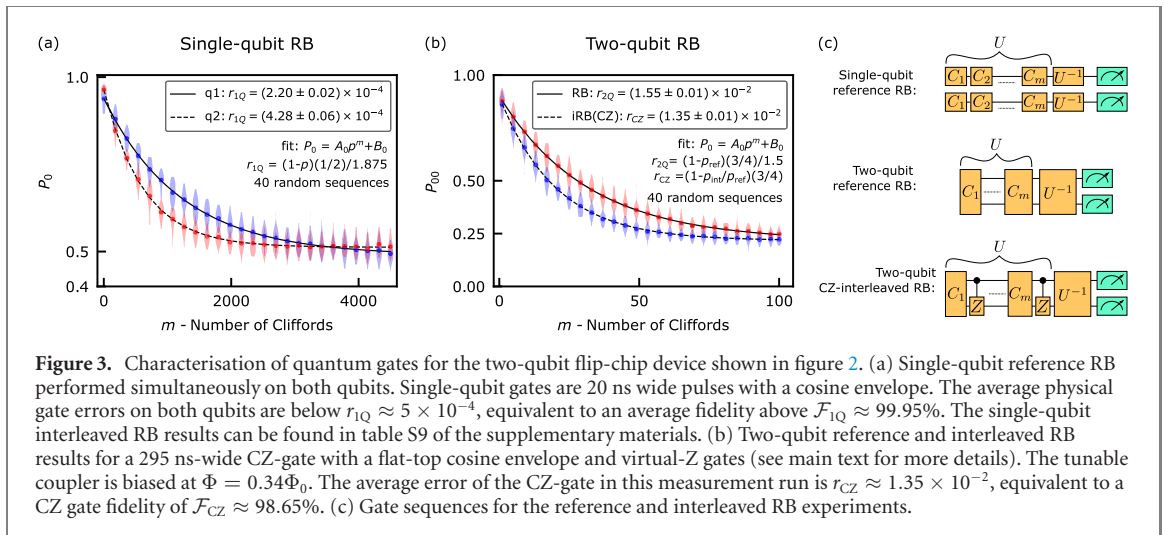
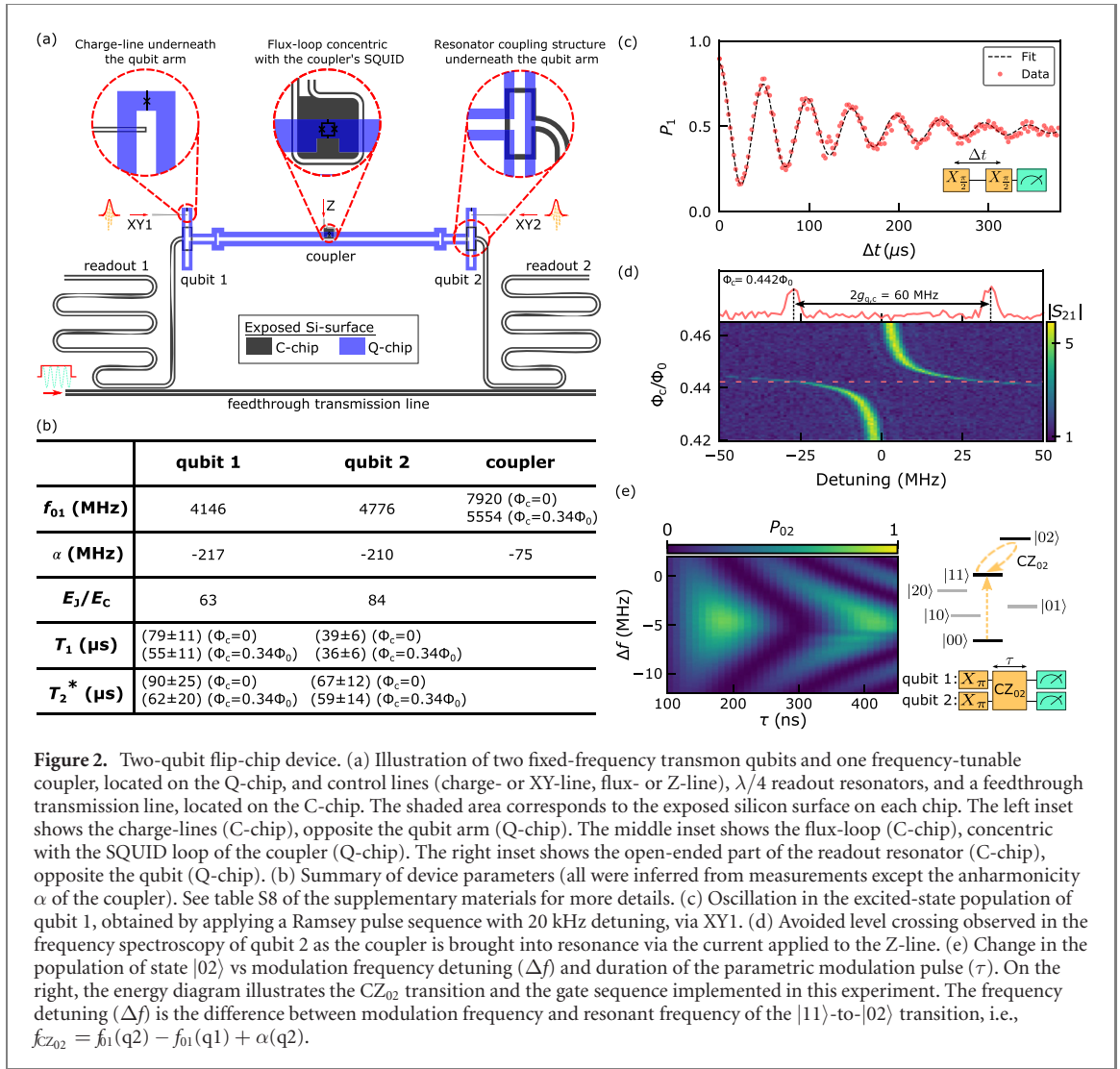
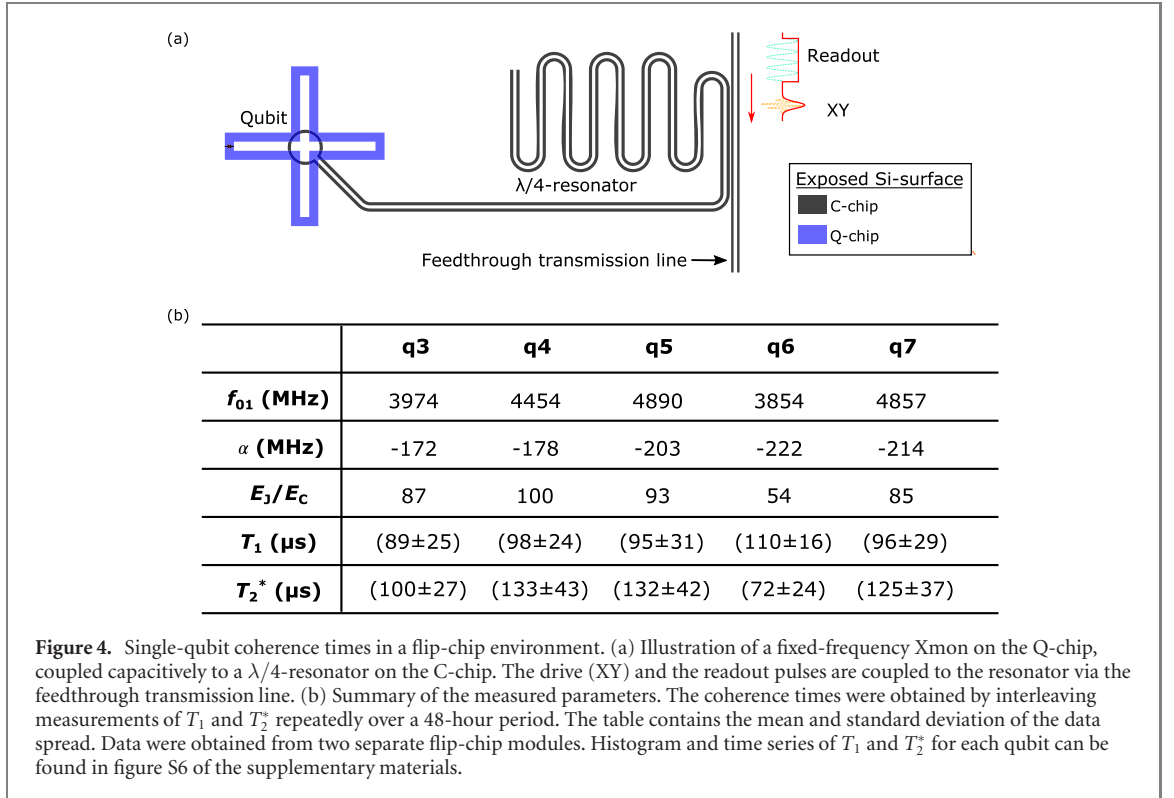


figure 3(c)). Each Clifford is a combination of several physical gates from our gate set. The decay constant of the measured sequence fidelity versus m provides an estimate of the average gate error [31, 32].

Our single-qubit gate is implemented by applying a 20 ns pulse with a cosine envelope, and is calibrated to maximise population transfer while minimising phase error [33–35]. Figure 3(a) shows results from single-qubit reference RB experiments performed simultaneously on both qubits. From this data, the average physical gate error of qubit 1 is $r_{1Q}(q1) = (2.20 \pm 0.02) \times 10^{-4}$, and of qubit 2 is



$r_{1Q}(q2) = (4.28 \pm 0.06) \times 10^{-4}$, where the uncertainty represents the standard error of the fit.

Furthermore, averaging the gate errors obtained from repeating single-qubit reference RB measurements over the course of 8 hours, without any additional gate recalibration in between, reveals similar results, $\bar{r}_{1Q}(q1) = (2.3 \pm 0.1) \times 10^{-4}$ for qubit 1 and $\bar{r}_{1Q}(q2) = (4.2 \pm 0.1) \times 10^{-4}$ for qubit 2, where the uncertainty is from the standard deviation of the spread (see figure S4 in section 4 of the supplementary materials). In terms of average physical gate fidelities, the 8-hour average values are

$$\bar{F}_{q1,meas} = 1 - \bar{r}_{1Q}(q1) = (99.977 \pm 0.001)\%$$

for qubit 1 and $\bar{F}_{q2,meas} = 1 - \bar{r}_{1Q}(q2) = (99.958 \pm 0.001)\%$ for qubit 2.

The CZ gate consists of a 295 ns flat-top pulse with a cosine-shaped rise and fall profile, complemented by virtual Z-rotations to both qubits. The latter serves to correct for additional dispersive shifts to both qubits introduced by the coupler during modulation [36]. Figure 3(b) shows the result from implementing a reference two-qubit RB experiment reaching an average physical gate error of $r_{2Q} = (1.55 \pm 0.01) \times 10^{-2}$. As this reference RB sequence contains a mixture of single-qubit and CZ gates, a variant sequence is performed by interleaving each random Clifford with a CZ gate (see figure 3(c) for the pulse sequence). The interleaved RB experiment can provide an estimate of the error per CZ gate, which in the case of figure 3(b) is $r_{CZ} = (1.35 \pm 0.01) \times 10^{-2}$. Similarly, the average CZ error is characterised over the course of 10 hours. Without any gate-recalibration in-between, we obtain an average CZ error of $\bar{r}_{CZ} = (1.34 \pm 0.08) \times 10^{-2}$ or equivalently a CZ fidelity of $\bar{F}_{CZ,meas} = 1 - \bar{r}_{CZ} = (98.66 \pm 0.08)\%$ (see figure S4 in section 4 of the supplementary materials).

4.3. Coherence times

Another common benchmark is the qubit coherence times, which, in the absence of other errors, set a bound on the device performance. In this section, we investigate whether the coherence time is substantially affected by the presence of another Si chip in close proximity and by the additional flip-chip fabrication process.

The table in figure 2(b) summarises the coherence times of the two-qubit flip-chip device (shown in figure 2(a)) obtained by interleaving measurements of relaxation times T_1 and Ramsey free-induction decay times T_2^* simultaneously on both qubits, and repeatedly over a 36-hour period. In this device, qubits 1 and 2 exhibit average $T_1 = 79 \mu$ s and 39μ s, respectively (at $\Phi_c/\Phi_0 = 0$). Simple estimations of the limit imposed by decays via the readout resonator and the XY-line show that both qubits in this flip-chip module are indeed Purcell-decay limited, with qubit 2 being penalised more for having stronger coupling and smaller frequency detuning from its readout resonator (see discussion in section 4.3 of the supplementary materials).

To further investigate the level of qubit coherence that can be achieved in the flip-chip fabrication process outlined in section 3, we characterised the coherence times of single-qubit flip-chip devices in a configuration shown in figure 4(a). In this simplified design, the ‘Xmon’ [37] qubit-state control and readout are both performed via the feedthrough transmission line that is coupled to the $\lambda/4$ -resonator, i.e., without a separate XY-line. Basic parameters of the five single-qubit flip-chip Xmons characterised in this work are summarised in the table in figure 4(b), with most exhibiting average values of T_1 and T_2^* above 90 μs . In contrast to the qubits in figure 2(b), a simple estimation of the T_1 -limit due to relaxation via the readout resonator shows that these qubits are not yet Purcell-decay limited by the coupling to the $\lambda/4$ -resonator ($T_p > 160 \mu\text{s}$, see section 5 of the supplementary materials).

5. Discussion

5.1. Gate fidelities and coherence times

Our demonstrated average gate fidelities in flip-chip are comparable to those obtained in single-chip devices [19] and those reported by other groups in flip-chip modules [1, 2, 9, 12, 38]. In particular, the short gate duration in reference [1] enabled a CZ fidelity of almost 99.6% in one qubit pair (figure S17 in its supplementary materials), in a scheme that relies on having frequency-tunable qubits. The coherence-time limit to the gate fidelities in our case is estimated to be $\mathcal{F}_{1Q,inc} \sim 99.98\%$ and $\mathcal{F}_{CZ,inc} \sim 99.34\%$ according to reference [39] (see section 6 of the supplementary materials). This indicates that the measured average single-qubit gate fidelity ($\bar{\mathcal{F}}_{1Q,meas} = (\bar{\mathcal{F}}_{q1,meas} + \bar{\mathcal{F}}_{q2,meas})/2 \sim 99.97\%$) and the average CZ gate fidelity ($\bar{\mathcal{F}}_{CZ,meas} = 98.66\%$) are still limited by both coherent and incoherent errors, with the single-qubit gate fidelities being closer to coherence-limited. Measures to improve the gate fidelities include decreasing the CZ gate duration, device redesign, and deploying more involved gate optimisation strategies [36].

Most of the single-qubit flip-chip devices in this work exhibit average $T_1 > 90 \mu\text{s}$ with average $T_2^* > T_1$, which is not degraded compared to our previously reported single-chip qubit coherence times for similar device geometry [18, 20]. Analysis of the participation ratio simulation results (section 7 of the supplementary material) shows that the metallic layer of the second chip does cause a redistribution of electric energy from the substrate to the vacuum space in-between the chips while leaving that within the thin oxide interfaces largely unchanged. Therefore, we do not expect higher losses in flip-chip for the device geometry we use, provided that the additional fabrication steps do not add significant lossy materials nor residues. This explains the similarity between the high coherence results in flip-chip and single-chip devices. Our coherence times also compare favourably to values reported for flip-chip devices by other groups [1, 2, 9, 11, 12, 21, 40].

Further work aiming to improve qubit coherence times in general will include device design and process development, in particular to reduce the loss contribution of dielectrics. Recently, transmons made of tantalum showed promisingly long T_1 as high as $\sim 500 \mu\text{s}$ in planar, single chips [41, 42]. We note that reference [11] reported on T_1 degradation of a ‘floating’ transmon design from $\sim 160 \mu\text{s}$ in the single-chip case down to $\sim 60 \mu\text{s}$ in the flip-chip case (see tables II & III in appendix A of reference [11]), highlighting the difficulty of developing fabrication processes and designs compatible with preserved coherence.

In a scaled-up quantum processor consisting of a two-dimensional array of interconnected qubits, multiple signal lines would be routed close together on the *C*-chip and would also pass directly below the couplers on the *Q*-chip. Understanding the extent to which this would induce signal crosstalk and influence the device parameters by added capacitance, inductance, and dielectric loss participation is a matter of ongoing investigation.

5.2. Parameter sensitivity

The ability to design and manufacture quantum processors according to the desired specification is of paramount importance in view of the resources required to fabricate and characterise them. One challenge with flip-chip integrated devices is that the interchip spacing d plays an important role in determining the device parameters. The statistics taken for a small number of modules in section 4.1 yield the following values for interchip spacing $d = (7.8 \pm 0.8) \mu\text{m}$ and chip tilt $\Delta d = (1.7 \pm 1.0) \mu\text{m}$. This justifies the design strategy described in section 2 (design for $d_{\text{target}} = 8 \mu\text{m}$, and examine parameter changes at $d = d_{\text{target}} \pm 1 \mu\text{m}$), which partially allows us to include design margins towards deviations in device parameters due to module-to-module variations in d and non-parallel chips (tilt, i.e., $\Delta d > 0$) within each module.

To quantify the parameter sensitivity of the flip-chip device, we consider as an example the parameter variation in the two-qubit flip-chip device of figure 2(a) due to a deviation of d by 1 μm from its target value. For larger deviations, see section 4.3 of the supplementary material.

According to our electromagnetic simulations, a 1 μm variation in d results in a 2.6% variation in the qubit self-capacitance. This is in contrast to single-chip qubits, whose charging energy is determined entirely by lithography, with negligible variations. Such variations have implications for the achievable qubit-frequency precision; this is particularly important for multi-qubit processors with fixed-frequency qubits, for which the frequency allocation for neighbouring qubits has to be carefully designed to minimise crosstalk. Adding the variation due to Josephson-junction resistance variations in our current process [20], the estimated qubit-frequency variation for a 4 GHz transmon qubit becomes 4.1% (see section 8 of the supplementary materials).

Other quantities are more strongly dependent on d , such as the coupling capacitance between XY-line and qubit or between readout resonator and qubit: our simulations indicate a 12% change for a 1 μm variation in d . This, in turn, affects the readout condition and the Purcell-decay limit imposed on the qubit. However, these couplings can be designed with a safe margin to anticipate variations induced during flip-chip bonding, as briefly described in section 2.

Likewise, to perform frequency-division multiplexed readout without crosstalk, resonators sharing the same feedthrough transmission line must be sufficiently separated in frequency. Module-to-module variations in d result in off-target resonant frequencies: in the absence of chip tilt ($\Delta d = 0$), the frequencies are shifted in the same direction, but in the presence of tilt they are shifted in opposite directions and may come too close. For the coplanar-waveguide resonators in figure 2(a), our electromagnetic simulations indicate that a 1 μm variation in d results in a 2% variation of the resonant frequency (120 MHz for a 6 GHz resonator). The frequencies must be allocated with this clearance in mind to ensure that frequency collisions between resonators due to chip tilt can be avoided.

Looking ahead, at least two possible improvements can be made to decrease the parameter sensitivity due to variations in d . The first is to implement hard-stop spacers to better control the resulting interchip spacing and tilt [21]. Another solution is to revise the device designs: for instance, a qubit facing a bare Si surface on the C-chip has a smaller relative contribution to its capacitance from the ground plane of the C-chip than one facing a superconducting ground plane, resulting in lower sensitivity to variations in d .

5.3. Chip deformation

The chip can also be deformed during bonding. Such deformation would result in a non-linearly varying chip separation across the module, which, if not understood properly, could adversely affect our ability to accurately target specific device parameters in a large quantum processor. Unfortunately, such deformation cannot be reliably deduced solely from the measurement of chip separation on each corner of the module. A more thorough investigation would require a full imaging of the chip surface before and after bonding. A parallel investigation track would be to compare measured device parameters to simulation and infer the local separation between the two chips at the device location.

5.4. Choice of target interchip spacing

Two considerations guided our choice of target interchip spacing, $d_{\text{target}} = 8 \mu\text{m}$. Larger values of d_{target} result in device parameters that are less sensitive to deviations in d (as shown in section 4.3 of the supplementary material). On the other hand, the lithography and deposition of indium bumps becomes impractical for $d_{\text{target}} > 8 \mu\text{m}$. Therefore, we aimed for a target value of 8 μm .

6. Conclusion

We have demonstrated the basic building blocks of a flip-chip integrated quantum processor and achieved transmon coherence times and quantum gate fidelities approaching the best flip-chip device performances reported in literature [1, 2, 12]. A comparison of coherence times with those from in-house-fabricated single-chip devices indicates that the qubits are not degraded by the additional flip-chip fabrication steps at this level of performance. The pristine flip-chip environment demonstrated in this work is therefore ready to be used for the investigation and implementation of multi-qubit processors.









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Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

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