Polarity-dependent threshold voltage shift in ovonic threshold switches: Challenges and opportunities

Taras Ravsher[1,2*], Robin Degraeve[2], Daniele Garbin[2], Andrea Fantini[2], Sergiu Clima[2], Gabriele Luca Donadio[2], Shreya Kundu[2], Hubert Hody[2], Wouter Devulder[2], Jan Van Houdt[1,2], Valeri Afanas'ev[1], Romain Delhougne[2], Gouri Sankar Kar[2]
[1]KU Leuven, Celestijnenlaan 200D, 3001 Leuven, Belgium; [2]IMEC, Kapeldreef 75, 3001 Leuven, Belgium; *taras.ravsher@imec.be

***Abstract*—**In this paper we investigate the operation of Si-Ge-As-Te Ovonic Threshold Switch (OTS) selectors under bipolar pulses. We observe that the threshold voltage increases noticeably if the previous pulse had opposite polarity. This effect is consistently present under different test conditions and persists for a long time (>1000s). We also investigate its impact on 1S1R operation, and discuss possible applications, such as OTS-only memory element.

I. Introduction

Success of next-generation resistive cross-point memory arrays (**Fig. 1a**) depends on the development of highly non-linear selector devices **[1]**. One of the promising candidates with respect to phase-change memory (PCM) technology are chalcogenide-based ovonic threshold switches (OTS). OTS can reversibly turn from an insulating state into a dynamic low-resistance state upon the application of voltage which exceeds certain threshold voltage V_{th} (see **Fig. 1b**). A forming process is necessary during the first pulse, which requires a larger voltage to switch, a first-fire (FF) voltage V_{FF} (**Fig. 3a**). Decreased threshold voltage after the FF pulse can be attributed to the "quenched" defects that remain in the delocalized state after the switch-off, facilitating creation of conduction cluster during subsequent cycles (**Fig. 3b,c**) **[2]**. In this work we show that, additionally, V_{th} depends on the relative polarity of the current and previously applied pulse.

II. Experimental

Devices under test (DUT) consisted of 20nm thick SiGeAsTe film fabricated in a pillar device configuration (see **Fig. 2**). TiN was used for both top (TE) and bottom (BE) electrodes. Integrated series resistor (R_s) was included to limit the maximum operating current. Additionally, 1S1R cells with 50nm GeSbTe (GST) PCM elements and Carbon-based electrodes were tested.

III. Polarity-dependence of threshold voltage

To test the impact of pulse polarity, a wave form with two positive pulses followed by two negative pulses was applied (see **Fig. 4a**). Resulting I-V characteristics are shown in **Fig. 4**. Naturally, the threshold voltage is higher during the positive FF pulse ($V_{FF,pos}$) compared to the subsequent switching pulse ($V_{th,pos}$). Interestingly, during the next two negative pulses, V_{th} is higher for the first one ($|V_{th,neg,1}|>|V_{th,neg,2}|$). The device behaves as if an additional forming process is necessary when switching in the polarity opposite to that used for the FF pulse. In other words, the conduction cluster is *directional*, and a new path must be formed when operating in different polarity.

Same measurement was repeated across 35 dies (**Fig. 5**). It shows that this effect is significant and is present for all devices. The distribution of V_{th} (**Fig. 5a)** demonstrates that there is a clear shift between $V_{th,neg,1}$ and $V_{th,neg,2}$, with median-to-median separation of $\Delta V_{th,neg,}^{median}$=260mV. **Fig. 5b** shows the distribution of a relative V_{th} shift in the negative direction ($\Delta V_{th,neg}=|V_{th,neg,1}|-|V_{th,neg,2}|$). Note, that every measured device experiences a small, but non-zero shift. The $\Delta V_{th,neg}$ values appear to show no spatial distribution (see **Fig. 5c**, note that only half of the wafer was available for the measurements).

Similar measurement was repeated on a number of devices with different values of R_s, to investigate the dependence on the operating current (I_{op}). **Fig. 6** shows the extracted threshold voltage shift $\Delta V_{th,neg}$ as a function of I_{op}. A clear trend can be observed, where $\Delta V_{th,neg}$ increases for smaller I_{op} values, with $\Delta V_{th,neg}$>300mV for R_s=37kΩ (I_{op}≈100μA). On the other hand, for R_s=2.5kΩ (I_{op}≈1.5mA) the V_{th} shift almost disappears. We believe this is related to the fact that for the smaller I_{op}, the conduction cluster is not fully formed (there are fewer defects involved) **[3]** and, therefore, it will be more susceptible to additional forming required to switch it in opposite polarity.

IV. Random polarity pulse characterization

In order to explore this phenomenon in detail and exclude any impact from the initial FF pulse, a more elaborate characterization procedure was developed. It consisted of a sequence of 100 triangular pulses (with the duration t_{pulse}=10μs and delay of t_{delay}=10μs between pulses), where the polarity of each pulse was chosen randomly (**Fig. 7a**). Here, the pulses are classified into two families: those that are the *same* polarity as the preceding pulse (colored blue), and those for which the previous pulse was of *opposite* polarity (colored red).

A. V_{th} evolution over 100 cycles vs pulse polarity

An example of the resulting I-V characteristics is shown in **Fig. 7b** (note, only a rising edge of the pulse, i.e. the switch-on transition, is displayed). One can clearly see that in the negative read-out branch there is a noticeable difference between the two pulse families, with $|V_{th,neg}^{opp}|>|V_{th,neg}^{same}|$. In the positive branch there seems to be no shift. The reason for this is not clear at the moment, but it might be related to the inevitable asymmetry of the interfaces at TE and BE. Evolution of the extracted V_{th} vs cycle number presented in **Fig. 7c**, confirms that $\Delta V_{th,neg}$ shift persists for at least 100 cycles. **Fig. 7d** shows the corresponding V_{th} distributions from all cycles. Similar to the results in **Fig. 5**, a strong shift of ~280mV between $V_{th,neg}^{opp}$ and $V_{th,neg}^{same}$ is present.

In order to get statistically reliable results, the same measurement was repeated on 30 identical devices (a unique random-polarity sequence was generated for each of them). The results are summarized in **Fig. 8**, showing the distribution of V_{th} across all 30 dies and all 100 cycles. It confirms that there is a significant shift in the negative branch. Again, the two distributions overlap in the positive branch. This seems to correlate with the fact that also the FF voltage is larger in the negative polarity (**Fig. 9**). Perhaps, larger V_{FF} in the negative polarity is linked to a weaker conduction cluster, resulting in a stronger polarity-dependence, following the same logic as in the case of I_{op} impact. Indeed, also for this random-polarity measurement increasing I_{op} leads to a decrease in median-to-median $\Delta V_{th,neg}$ shift, as shown in **Fig. 10**.

B. Impact of relaxation time between pulses

In order to assess the impact of the relaxation time, another measurement was performed with much longer delay (t_{delay}=1s). Resulting V_{th} distribution is shown in **Fig. 11a**. Even with an increased delay time, the $\Delta V_{th,neg}$ shift still persists. However, there are few differences, compared to the data in **Fig. 8**: (i) the absolute value of V_{th} is larger due to the V_{th} relaxation effect **[4]**, (ii) $\Delta V_{th,neg}$ is larger compared to t_{delay}=10µs (see **Fig. 11c**) and (iii) now a small window in the positive branch ($\Delta V_{th,pos}$) starts to appear. Increased $\Delta V_{th,neg}$ for longer t_{delay} is in line with the results on I_{op} dependence. Now, the cluster will also be smaller because fewer quenched defects remain **[2]**.

This experiment suggests that ΔV_{th} shift is very robust and persistent – V_{th} is history-dependent, and it "remembers" the polarity of the previous pulse even after 1s delay (the effect even gets stronger over time). Moreover, we performed a single device measurement with much longer delay time of t_{delay}=1000s (≈17min), which shows similar behavior (**Fig. 12**). One can think of practical applications, where this effect may be utilized. For example, *OTS selector itself can act as a memory element*, without the need for a PCM cell (such element would also be self-rectifying, significantly reducing the complexity of the memory array). Alternatively, this effect may be used to enhance the operation of a standard 1S1R cell, as will be discussed in section **V**.

C. Updated OTS switching model with directional cluster

Based on the data presented so far we update our OTS switching model **[2]** to incorporate this effect. One possible explanation for it is that the conduction process through a cluster is directional. To realize this, we propose a model with two types of defects – with energy levels close to the conduction band (CB) and the valence band (VB), as shown in **Fig. 13a**. Under zero electric field both types correspond to what we referred previously as localized defects. We suggest that, upon the application of sufficiently large electric field, the levels that align in energy may interact to form a delocalized defect pair. This way, most of the logic from our Monte-Carlo model can be reused, though with some differences. With the proposed model, a pair of defects in a delocalized state contributes to the conduction only in one direction. Therefore, if a cluster was formed in a BE→TE direction (**Fig. 13b**), some additional defects will need to switch to allow it to conduct in a TE→BE direction (**Fig. 13c**), thus increasing a voltage required for switching. Alternatively, this effect may be caused by a local charging phenomenon. Considering that OTS switching is filamentary, the polarity of charge trapped close to the constriction point will be different for opposite bias polarities. Further investigation is necessary to clarify the exact mechanism behind this effect.

V. V_{TH} SHIFT IN 1S1R CELL

OTS selector is intended to be operated in a 1S1R cell, together with a memory element, such as GST PCM (**Fig. 14a**). After a write operation (short amorphizing pulse for RESET or triangular pulse followed by a longer crystallization plateau for SET, see **Fig. 14b**) the effective V_{th} of the complete cell changes ($|V_{th}^{RESET}|>|V_{th}^{SET}|$) **[5]**, and the read operation is typically performed in the same direction (**Fig. 14c**). However, since the V_{th} of OTS is polarity-dependent, this should affect the operation of 1S1R cell. To test this, the pulse form shown in **Fig. 15a** was employed, consisting of different combinations of positive/negative write and read operations. The result of such a measurement is shown in **Fig. 15b**. One can see that in addition to the SET-RESET split, there is also a shift in V_{th} depending on the polarity of the SET/RESET pulse compared to that of the read pulse (again, only in the negative branch). Extracted V_{th} distributions (**Fig. 15c**) show rather strong shift after SET operation ($\Delta V_{th,neg}^{SET}$=300mV), while a significantly lower shift can be observed for RESET ($\Delta V_{th,neg}^{RESET}$=90mV). Despite the lower $\Delta V_{th,neg}^{RESET}$, the shift is very consistent. This can be seen in **Fig. 15d**, which shows that relative $\Delta V_{th,neg}$ (with respect to each cycle) is >0 for each of the 30 dies.

This effect can be a potential reliability issue, since it introduces an additional source of V_{th} instability, which may be triggered by any unexpected opposite polarity pulse. On the other hand, OTS serves here as an additional memory element. This way, a 4-level cell may be realized, when operating 1S1R in both positive and negative polarities. Additionally, it may also be used to increase the memory window, by performing SET and RESET operations with opposite polarities.

SUMMARY

In this work we describe a phenomenon of a history-dependent V_{th} in OTS devices and show that $|V_{th}|$ increases if the polarity of the pulse is opposite to that of the previous one. Understanding what controls the magnitude of this effect may pave the way towards exploiting it to enhance existing 1S1R technology and develop new memory solutions based on OTS as self-rectifying memory element.

ACKNOWLEDGMENT

T.R. would like to thank FWO for the funding provided via SB research fellowship (grant no 1SD4721).

REFERENCES

[1] Burr *et al.*, *J. Vac. Sci. Technol. B*, vol. 32, no. 4, p. 040802, Jul. 2014, doi: 10.1116/1.4889999 [2] Degraeve *et al.*, in *2021 IRPS*, Mar. 2021, pp. 1–5. doi: 10.1109/IRPS46558.2021.9405114 [3] Kabuyanagi *et al.*, in *2020 VLSI* pp. 1–2. doi: 10.1109/VLSITechnology18217.2020.9265011 [4] Chai *et al.*, in 2019 *VLSI*, pp. T238–T239. doi: 10.23919/VLSIT.2019.8776566 [5] Chien *et al.*, *IEEE Trans. Electron Devices*, vol. 65, no. 11, pp. 5172–5179, Nov. 2018, doi: 10.1109/TED.2018.2871197.

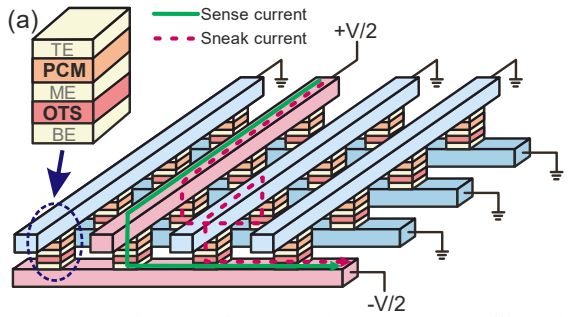


Fig. 1: (a) Schematic of a cross-point memory array, illustrating sneak current path. (b) Typical I-V characteristics of a Si-Ge-As-Te OTS selector, showing the definition of half-bias non-linearity $NL_{1/2}$.

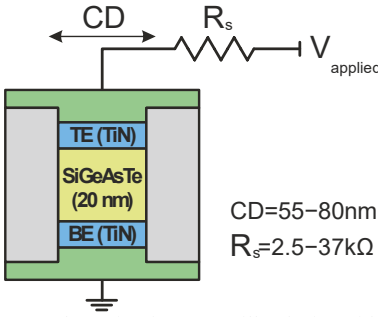


Fig. 2: Schematic of an OTS pillar device with an integrated series resistor.

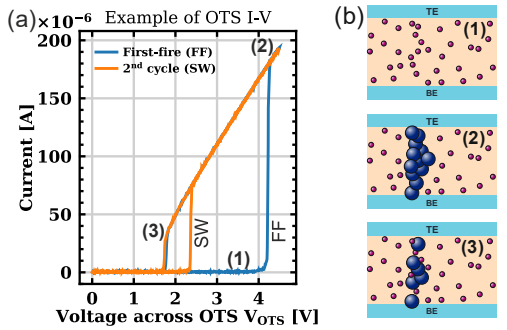


Fig. 3: (a) Typical OTS I-V characteristics during the first-fire (FF) and subsequent switching cycle (SW), with $V_{th}<V_{FF}$. (b) A model of OTS switching – conduction cluster is formed from delocalized defects [2]. (c) Transition between localized and delocalized states is controlled by electric field and temperature.

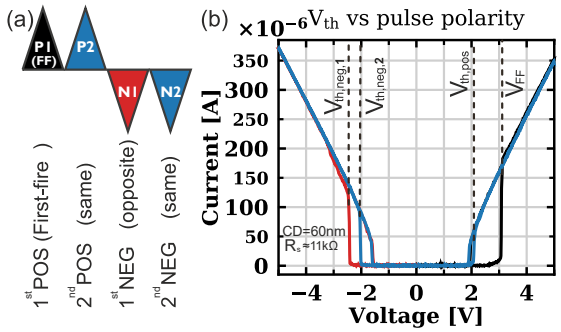


Fig. 4: (a) Pulse form used to test polarity dependence of V_{th}. (b) An example of the resulting I-V characteristics. Threshold voltage is higher during the first pulse in the negative direction, compared to the next cycle ($|V_{th,neg,1}|>|V_{th,neg,2}|$).

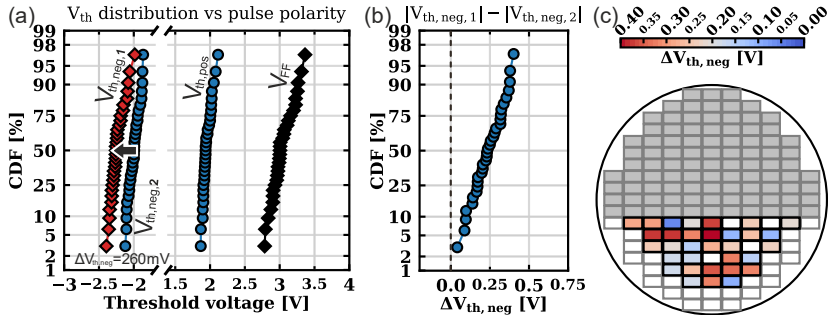


Fig. 5: (a) Distribution of V_{th} measured across 35 dies (as described in **Fig. 4**). (b) Relative V_{th} increase in negative polarity ($\Delta V_{th,neg}=|V_{th,neg,1}|-|V_{th,neg,2}|$). Note, that $\Delta V_{th,neg}>0$ for every measured device. (c) Wafer map showing spatial distribution of $\Delta V_{th,neg}$.

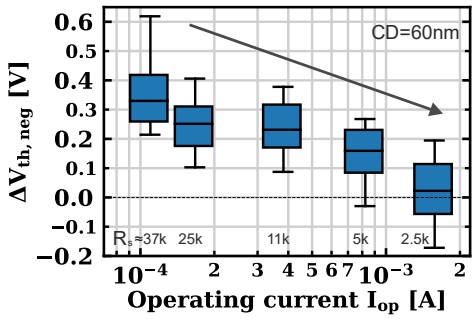


Fig. 6: Threshold voltage shift $\Delta V_{th,neg}$ measured on devices with different series resistance. $\Delta V_{th,neg}$ is the highest for large R_s values (lower operating current I_{op}).

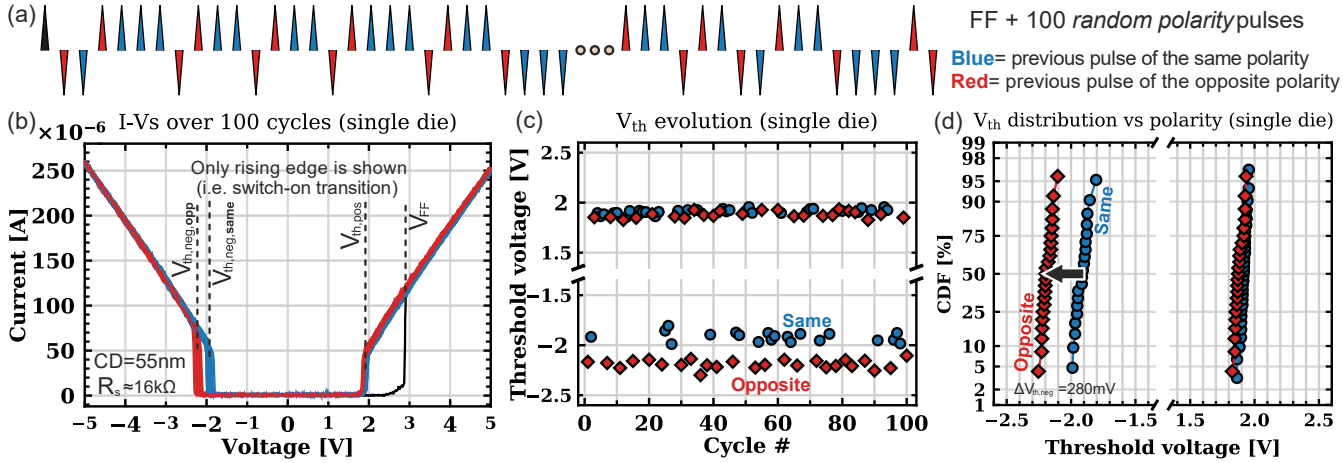


Fig. 7: Random polarity pulse sequence. (a) Test waveform with 100 pulses of random polarity. Color-code corresponds to the polarity of the *previous* pulse. (b) Typical I-V characteristics of a representative device and (c) extracted V_{th} evolution throughout 100 cycles. (d) Distribution of V_{th}, showing a clear difference between same ($V_{th,same}$) and opposite ($V_{th,opp}$) polarity of the previous pulse, in the negative read-out branch.

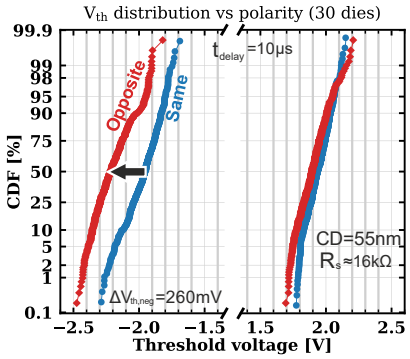


Fig. 8: Same measurement as in **Fig. 7**, repeated across 30 dies. Strong $\Delta V_{th,neg}$ shift can be clearly seen. In the positive branch $V_{th,pos}^{same} \approx V_{th,pos}^{opp}$.

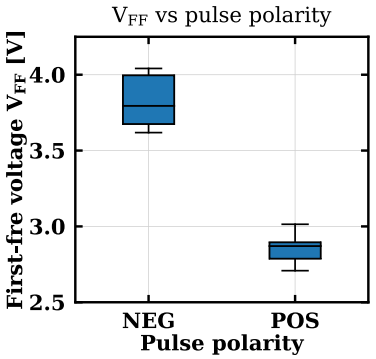


Fig. 9: First fire voltage is higher in the negative direction, $|V_{FF,neg}|>|V_{FF,pos}|$. This may be related to ΔV_{th} only being observed in the negative branch.

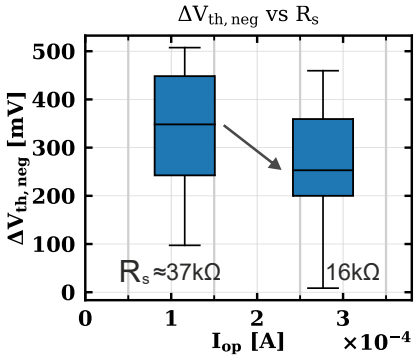
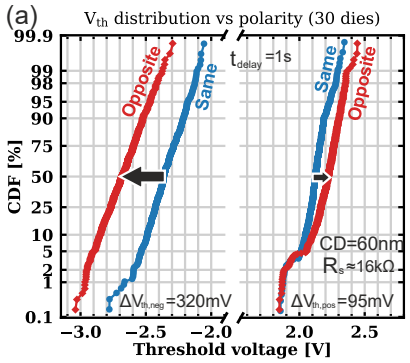


Fig. 10: $\Delta V_{th,neg}$ shift in the negative readout branch is larger for larger R_s (i.e., smaller I_{op}), same as in **Fig. 6**.



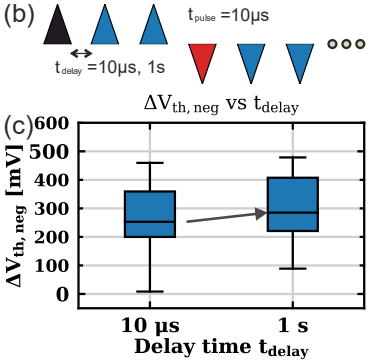


Fig. 11: (a) Same measurement as in **Fig. 8**, but with longer delay time between pulses (t_{delay}=1s), as shown in (b). After this rather long delay, $\Delta V_{th,neg}$ still persists. (c) Moreover, it is even enhanced compared to t_{delay}=10µs. Also, a shift starts to appear in the positive branch $\Delta V_{th,pos}>0$, as seen in (a).

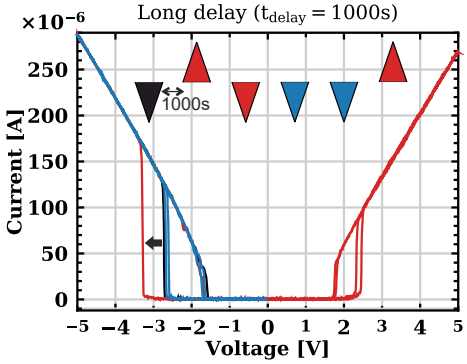


Fig. 12: Even after t_{delay}=1000s (≈17min) the shift still persists (measurement on a single device). This effect is long-lasting, suggesting that OTS only device can be used as a self-rectifying memory element.

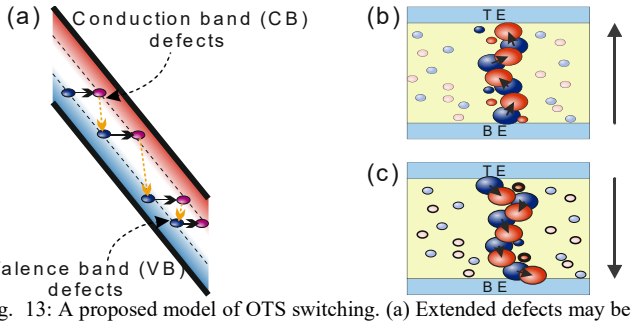


Fig. 13: A proposed model of OTS switching. (a) Extended defects may be formed from a pair of CB and VB defects, that align in energy under applied field. (b),(c) This implies that conduction cluster is directional.

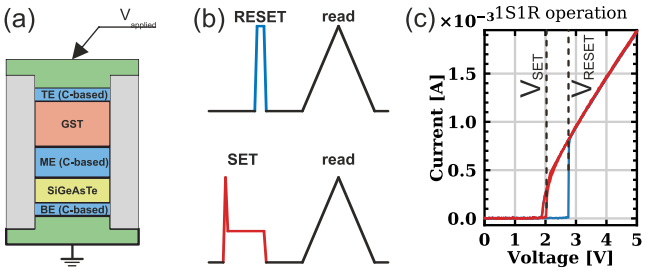


Fig. 14: 1S1R cell operations. (a) Schematic of 1S1R pillar device. (b) Pulses used for write operations: RESET (amorphization) and SET (crystallization). (c) Resulting read-out I-V characteristics, showing $V_{SET}<V_{RESET}$.

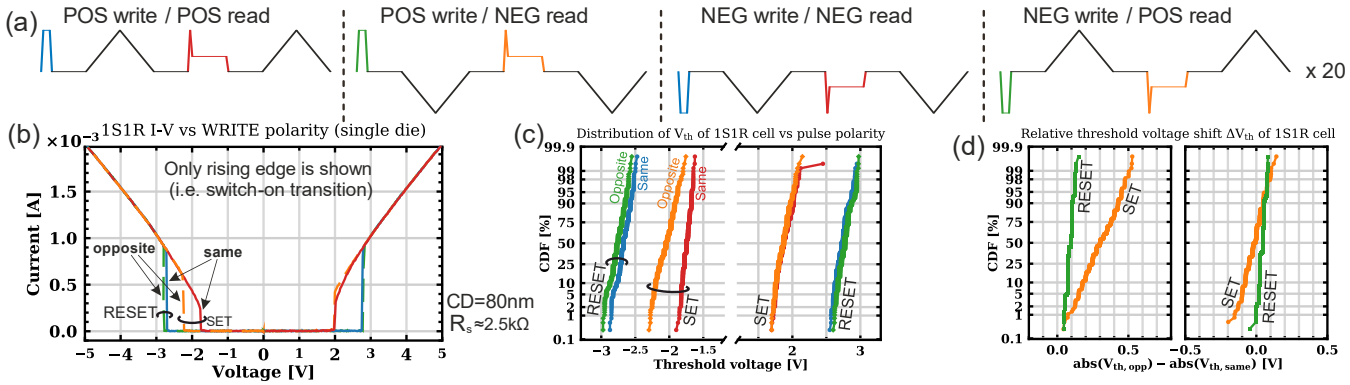


Fig. 15: Polarity-induced V_{th} shift in 1S1R cell. (a) Pulse form with various combination of positive and negative write & read operations, repeated 20 times for each device. (b) An example of I-V (representative die) for one of the cycles (only rising edge shown). (c) Extracted V_{th} distribution (30 dies x 20 cycles). In addition to SET-RESET shift, V_{th} depends on the polarity of the write operation. (d) $\Delta V_{th,neg}>0$ for all devices in the negative branch, $\Delta V_{th}\approx 0$ in positive.