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Epitaxial buffer structures grown on 200 mm engineering substrates for 1200 V E-mode HEMT application ⒡

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ABSTRACT

In this work, we demonstrate the epitaxial growth of a gallium-nitride (GaN) buffer structure qualified for 1200 V applications on 200 mm engineered poly-AlN substrates with hard breakdown >1200 V. The manufacturability of a 1200 V qualified buffer structure opens doors to high voltage GaN-based power applications such as in electric cars. Key to achieving the high breakdown voltage is careful engineering of the complex epitaxial material stack in combination with the use of 200 mm engineered poly-AlN substrates. The CMOS-fab friendly engineered poly-AlN substrates have a coefficient of thermal expansion (CTE) that closely matches the CTE of the GaN/AlGaN epitaxial layers, paving the way for a thicker buffer structure on large diameter substrates, while maintaining the mechanical strength of the substrates and reaching higher voltage operation.

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(Al)GaN buffer growth on Si is becoming standard technology;[1–4] however, the high voltage operation >1200 V requires either native or engineered substrates as the mechanical strength of traditional 200 mm Si wafers even with thickness larger than 1100 μm does not allow growing thicker stacks, which is critical to enable high voltage operation.[5–7] This is mainly due to a large lattice and coefficient of thermal expansion (CTE) mismatch between GaN and Si. Therefore, the use of substrates with a CTE-matched core is one of the solutions to enable high voltage operation. One such option is to use engineered poly-AlN substrates mainly due to their CTE-matched core to GaN and higher mechanical strength of the wafers.[8] The engineered poly-AlN substrates are commercially available from Qromis, Inc., also known as QST® substrates.[9] In this work, we will demonstrate 1200 V buffers on 200 mm engineered poly-AlN substrates (QST®) for p-GaN gate based E-mode HEMT devices. Two different buffer schemes based on intrinsic (carbon comes from Al and Ga precursors) and extrinsic (dedicated source for carbon) C-doping will be presented. The buffer scheme on QST® substrates is based on the reversed stepped superlattice (RSSL) scheme, a proprietary concept that Imec invented.[10] The RSSL buffer scheme was chosen in the epitaxial

process development instead of a single superlattice (SL) buffer scheme, because the RSSL buffer scheme features a much larger flexibility in stress engineering and, hence, becomes a more promising candidate for the growth of thick buffer structures on the engineered substrates of large size, which show different mechanical behaviors than regular Si substrates.

Furthermore, it must be noted that strong strain partition effect exists for (Al)GaN growth on engineered substrates such as SOI and QST®.[11] The strain partition effect occurs when most of the strain is accommodated in a compliant substrate [i.e., the top Si (111) device layer in the case of SOI and QST® in Fig. 2], which is usually thinner than the stack thickness itself. This strong strain partition leads to built-up of high curvature during the growth. One approach to limit the *in situ* curvature built-up is to use thicker complaint substrates. However, this will not be sufficient enough, and the strain partition effect will remain the limiting factor preventing the growth of thicker buffers for high voltage applications. Conventional buffer schemes using stepped SL (i.e., Eq. Al-1% > Eq. Al-2% in Fig. 1, for more details on the stepped SL scheme, readers are referred to Ref. 12) are based on continuous built-up of compressive stress, which leads to
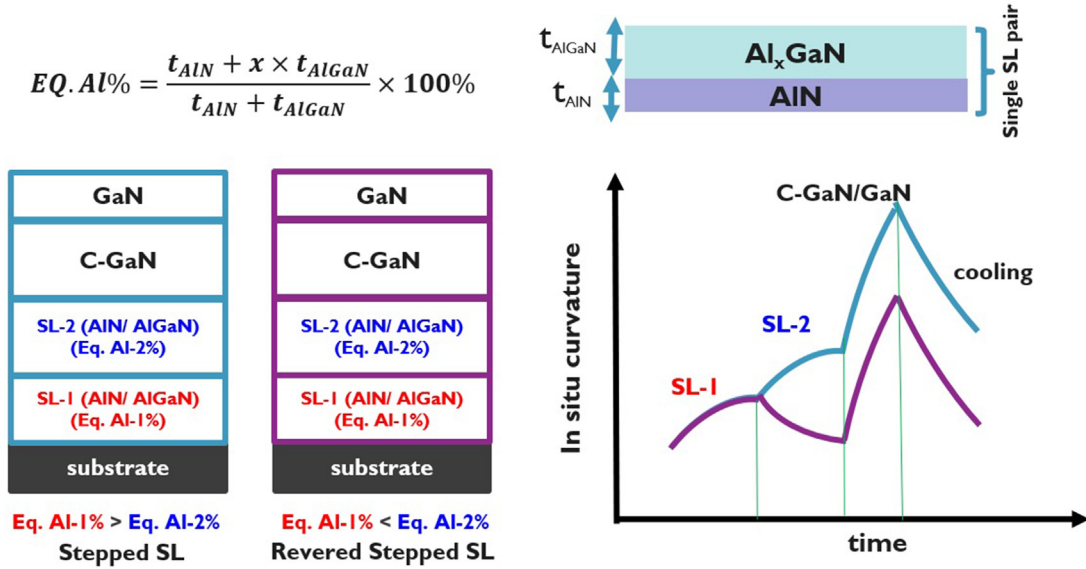
FIG. 1. Conceptual representation of stepped SL and reversed stepped SL. The equivalent Al% in the SL is calculated using the formula shown in the figure. t_{AlN} and t_{AlGaN} are thicknesses of AlN and Al$_x$GaN in the SL pair. x is Al%.

high curvature on the QST® substrates during growth. Therefore, the growth of thicker buffers on QST® substrates requires introduction of tensile stress in order to limit the *in situ* curvature built-up. This can be achieved through introduction of alternative compressive and tensile stress (i.e., Eq. Al-1% < Eq. Al-2% in Fig. 1). Following this, the reversed SL can also be stacked in order to optimize the *ex situ* wafer bow. However, in this study, we have only used the single reversed SL approach, which already allows us to grow buffer structures as thick as 7 μm with very low bow values as discussed later. Using the RSSL approach, no wafer breakage has been observed during epitaxial

growth in our metalorganic chemical vapor deposition chamber or while device processing.

All epitaxial stacks discussed in the following were grown on 200 mm QST® substrates using a state-of-the-art planetary AIXTRON G5+ C reactor®. Three different stack concepts as shown in Fig. 2 were investigated. From here on, these stack concepts are referred to as stack A and stack B (both with intrinsic C-doping) and stack C (with extrinsic C-doping). All stacks are based on the RSSL scheme. The main difference between stack A and stack B is in the buffer region. Aside from the different Al% in the SL region, stack B has
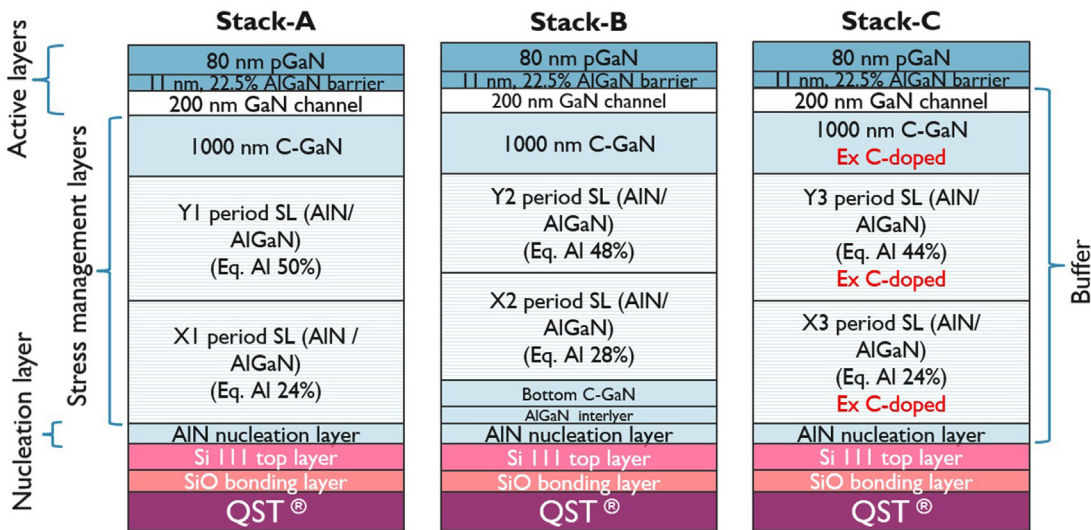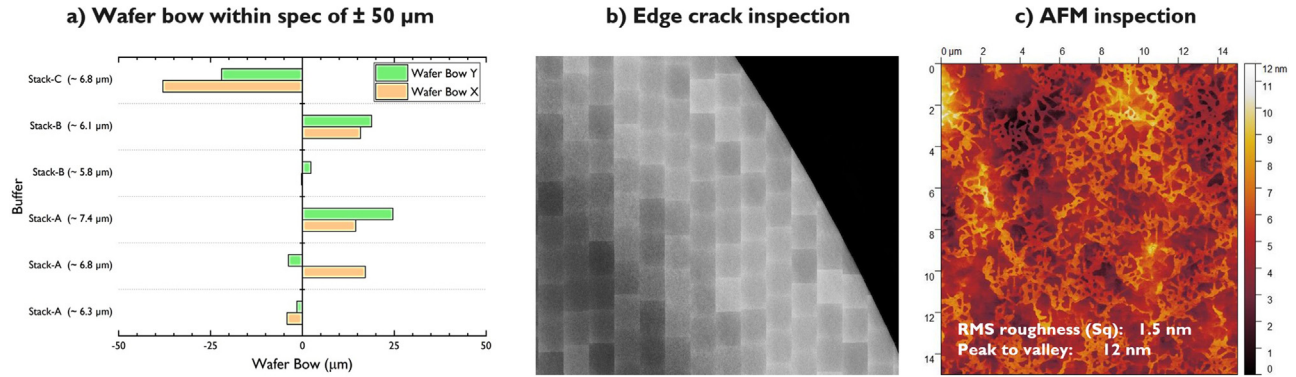

FIG. 2. HEMT stacks based on intrinsic (stack A and stack B) and extrinsic (stack C) C-doping developed in this study. Buffer thicknesses of stack A and stack B vary from 5.3–7.4 to 4.8–6.1 μm, respectively. Stack C has a thickness of ~6.8 μm.

FIG. 3. (a) Wafer bow on stack A, stack B, and stack C with various thicknesses, (b) CAMTEK edge inspection (the square pattern on the wafer is due to stitching of measurement shots), and (c) AFM inspection on ∼6.8 μm thick stack C.

bottom C-doped GaN and AlGaN interlayers. The motivation for the use of bottom interlayers will be discussed later. Stack C is based on external C-doping in the SL and GaN:C. There are different routes by which a higher V_{BD} can be achieved for GaN-based epitaxial stacks: (a) by increasing Al% in the SL region, as the critical electric field of AlN (12 MV/cm) is greater than that of GaN (3.4 MV/cm),[13] (b) optimizing C-levels mainly in the SL and GaN:C by using either an external C-doping source such as ethylene (C_2H_4) or by adjusting process parameters (which impacts the crystal quality), and (c) by increasing the buffer thickness to reduce the critical field at the AlN/Si interface.[13,14] Routes (a) and (b) have been optimized prior to this study. Route (c) will be assessed in this study beside the different stack concepts. Therefore, stack A and stack B were grown with different thicknesses of the stress management layers to reach the target V_{BD} of at least 1200 V. It must be noted that low post-epi bow values were achieved even for thicker buffer (∼7 μm) stacks by tuning the individual layer thicknesses of the stress management layers [Fig. 3(a)]. No slip lines and deep cracks were observed through the wafer during CAMTEK (an optical method to inspect inner cracks and slip lines in epitaxial layers) inspections as shown in Fig. 3(b). The surface roughness extracted from AFM measurements for the 6.8 μm thick stack C

is as low as 1.5 nm [Fig. 3(c)]. Figure 4 shows TEM inspections on all stacks. It is evident that the high threading dislocation density is present at an AlN/Si device layer interface and runs through the whole stack. Similar behavior has been observed for GaN on Si growth. Defect control has not been focus of this study as it is known on the contrary that large density of these defects might actually help to reduce the dispersion for intentionally C-doped buffers.[15] The crystalline quality of the AlN nucleation and (Al)GaN buffer is benchmarked using HR-XRD measurements in Table I. Important to note is that test structures to measure V_{BD} and buffer dispersion were fabricated on the newly developed stacks according to the process flow described in Ref. 7.

Low vertical buffer leakage (to have a good ON/OFF current ratio for the transistors) and low buffer dispersion (for good dynamic performance of the device) are two crucial parameters for power device applications.[16–18] The buffer leakage is evaluated for intrinsically C-doped stack A and stack B with different thicknesses as shown in Fig. 5. The measurement setup for vertical buffer leakage currents in forward (FWD) and reverse (REV) bias is shown in the inset of Fig. 5(d). Figures 5(a) and 5(d) show the comparison of buffer leakage current for 5.3 and 7.2 μm thick stack A at 25 and 150 °C, respectively. The
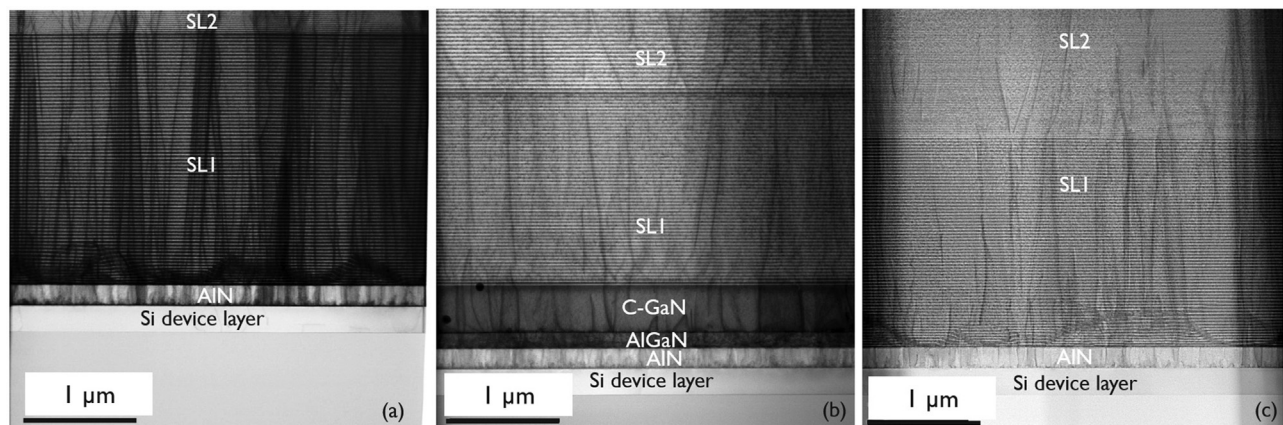
FIG. 4. STEM inspections on (a) stack A, (b) stack B, and (c) stack C. The threading dislocations start at the AlN/Si interface and run through the whole stack.

TABLE I. HR-XRD benchmark for buffer structures.

Stack	AlN (002) Mean (Std. Dev.) (arcsec)	GaN (002) Mean (Std. Dev.) (arcsec)	GaN (102) Mean (Std. Dev.) (arcsec)
A	694 (14)	536 (51)	1647 (46)
B	845 (78)	530 (36)	1538 (29)
C	853 (25)	731 (24)	1706 (46)

V_{BD} scales with total stack thickness, reaching >1200 V for 7.2 μm stack A both in FWD as well as in the REV direction for a maximum allowed buffer current limit of 1 μA/mm^2 at 25 °C and 10 μA/mm^2 at 150 °C (shaded region in cyan). However, the FWD and REV I–V characteristics are asymmetric for stack A. This is particularly apparent for elevated temperatures where there is a difference of >300 V between FWD and REV biasing. For stack B in Figs. 5(b) and 5(e), a similar trend in V_{BD} scaling is observed as a function of thickness, although maximum V_{BD} for the thickest stack B (i.e., 6.1 μm) is limited to ∼900 V. This is mainly because the total stack thickness is lower as compared to stack A with V_{BD} >1200 V. Increasing the total stack thickness to 7 μm will allow to achieve V_{BD} >1200 V.

It is evident that the insertion of bottom C-GaN and AlGaN interlayers in stack B allows us to achieve symmetric I–V characteristics in FWD and REV directions compared to stack A. However, it is known from GaN on Si experiments (not shown here) that the main reason for such asymmetry is absolute C-concentration in the SL

region. For tuned (and uniform C-levels) across the wafers, there is negligible difference in FWD and REV I–V characteristics as shown in Figs. 5(c) and 5(f) for extrinsic C-doped stack C.

Note that the systematic failures have been observed in the center region of the wafer (i.e., lower V_{BD} compared to middle and edge regions) for both stack A and stack B independent of the total stack thickness. This is due to a non-uniform intrinsic C-doping within the wafer as shown in Fig. 6(a) for the 7.2 μm stack A. Optimizing this uniformity has not been the focus of this work. By adjusting the local V/III ratio and flow distribution, an improvement can be expected. The average C-level can be controlled by conventional tuning, e.g., temperature and V/III ratio.[19] Adjusting the C-level by an intrinsic doping level requires unfavored process conditions for crystal quality and limits the process parameter space significantly. As a preferred choice, the C-level and uniformity can be controlled by using an external C-doping source. This allows a very wide process window and combines very high crystal quality with C-density optimized for high breakdown and with little to no buffer dispersion.[20,21] We have chosen this route, as will be discussed for stack C.

To avoid the narrow process window of intrinsically doped stacks and to optimize the C-level and crystal quality at the same time, it is the preferred choice to use extrinsic C-doping in the SL and GaN:C (i.e., stack C developed in this study). Mainly, extrinsic doping offers the choice to combine high growth temperature with high C-levels at high V/III ratio. The C-level and uniformity can be easily adjusted by the precursor flow rate and the distribution via the fivefold injector of
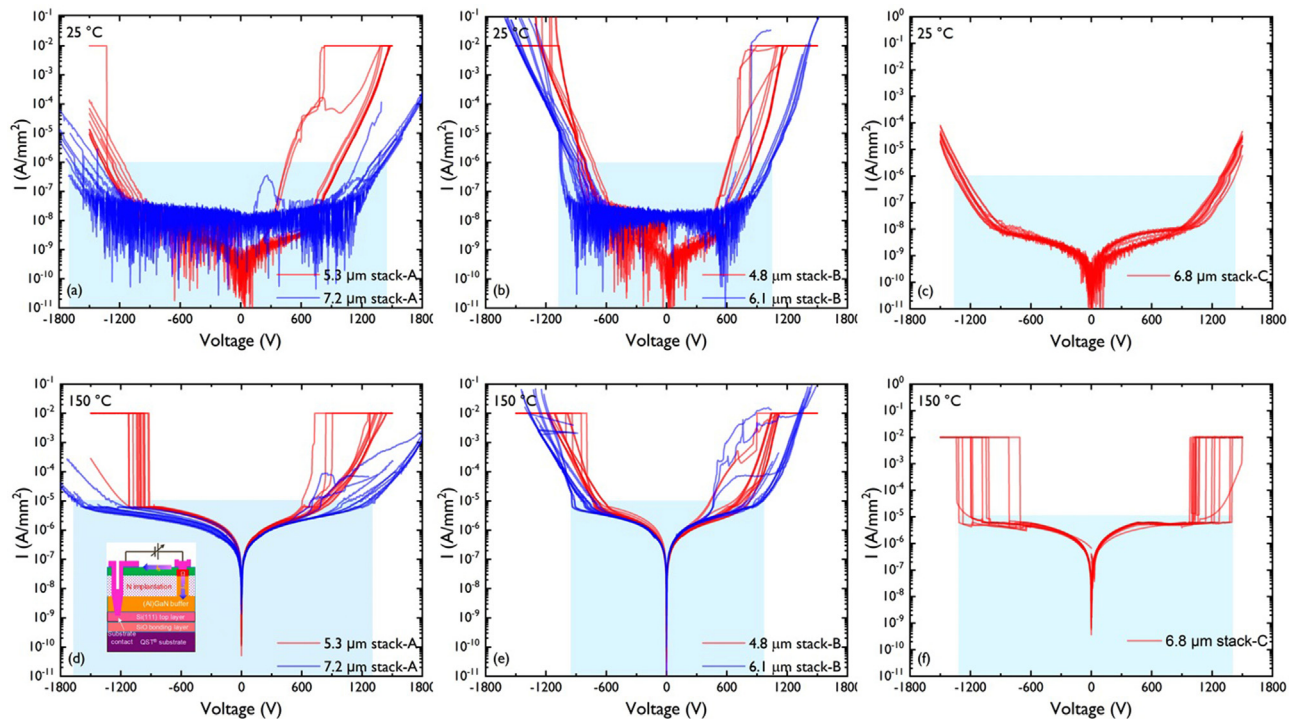

FIG. 5. Vertical buffer leakage measurements for intrinsic C-doped (a) and (d) stack A (5.3 μm vs 7.2 μm), (b) and (e) stack B (4.8 vs 6.1 μm), and (c) and (f) stack C (6.8 μm) at 25 and 150 °C. The measurement setup is shown in the inset of Fig. 5(d).
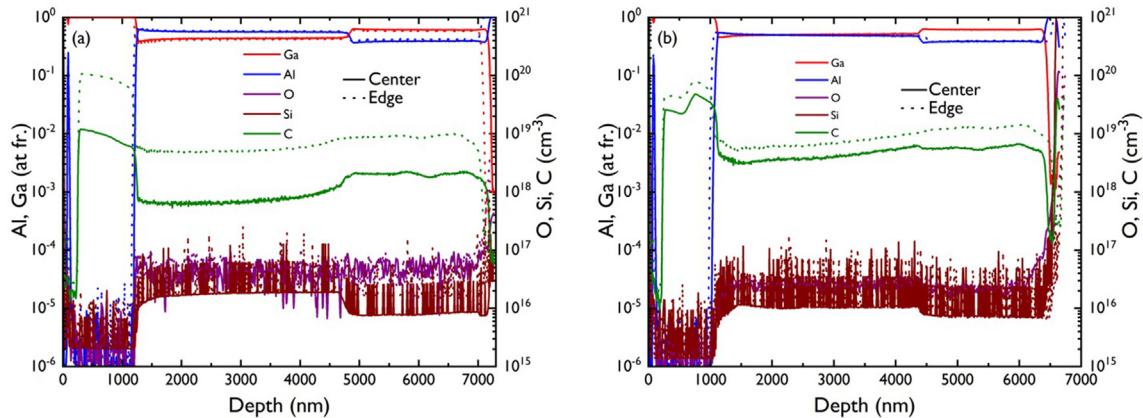
FIG. 6. SIMS measurements showing Ga, Al, Si, O, and C profiles at the center and edge of the (a) 7.2 μm stack A and (b) 6.8 μm stack C.

the G5+ C reactor®. Figure 6(b) shows improved center to edge uniformity for stack C using extrinsic C-doping in SL and C-GaN.

Figures 5(c) and 5(f) show the comparison of the buffer leakage current for a 6.8 μm thick stack C at 25 and 150 °C, respectively. The V_{BD} is uniform throughout the wafer, demonstrating the clear advantage of using an external C-doping source to control the C-level in SL and GaN:C. V_{BD} is >1200 V at 25 °C. At 150 °C, some of the structures start to fail around 1000–1100 V. The root cause for these sudden failures is not yet understood. For the moment, we can exclude extrinsic C-doping as the origin of these failure, as earlier experiments in GaN-on-Si have shown improved device yield (see the supplementary material for V_{BD} comparison between GaN on Si and QST® buffers). Further increasing the buffer thickness to 7.2 μm as for stack C will provide sufficient margin in V_{BD} so that all structures within the wafer reach the target voltage of 1200 V at higher temperatures as well.

Next, the buffer dispersion using the two-dimensional electron gas (2DEG) transmission line method (TLM) structure was evaluated. First, the initial current between two Ohmic contacts is measured [Fig. 7(a)]. Second, a back-gating of either −900 or −1200 V [Fig. 7(b)] depending on the stack thickness is applied for 10 s on the substrate electrode [V_{subs} in Fig. 7(a) contacted from the surface using deep via processing, covered with a thick Al-containing metal], followed by a TLM current measurement. The initial and final current (after back-gating stress) is converted to R_0 and R_{TLM}, respectively. Figures 8(a)

and 8(b) show the buffer dispersion (R_{TLM}/R_0) for the thickest stack A (7.2 μm) and stack B (6.1 μm). It is evident that the buffer dispersion is slightly on the higher side (within a range of ± 25%) for stack A, similar to results for other buffer thicknesses. However, the buffer dispersion for 6.1 μm stack B is extremely low within a range of ±5%. Furthermore, the extrinsically C-doped stack C shows advantages over the intrinsic doping in stack A with a very narrow distribution for buffer dispersion even at −1200 V as shown in Fig. 8(c).

It must be noted that there is basically no difference between dispersion performance at 25 and 150 °C for individual stacks. However, buffer dispersion is significantly improved while comparing stack A and stack C, which are based on the same buffer scheme except that SL and C-GaN are extrinsically doped. It has been reported in the literature that extrinsically C-doped GaN buffers have better dynamic properties.[22] This has been related to a more efficient transport of trapped charge for extrinsically C-doped GaN. However, the findings in Ref. 22 were limited to different C-doping methods in C-GaN only, and the doping method in other stress relief layers was kept the same (i.e., intrinsic). The impact of extrinsically C-doped SL layers on charge transport requires further understanding as scope of the future work. On the other hand, for intrinsic stacks, buffer dispersion is also improved for stack B as compared to stack A. This could also be due to insertion of bottom C-GaN as discussed for improved symmetry of I-V characteristics. However, this requires further technology
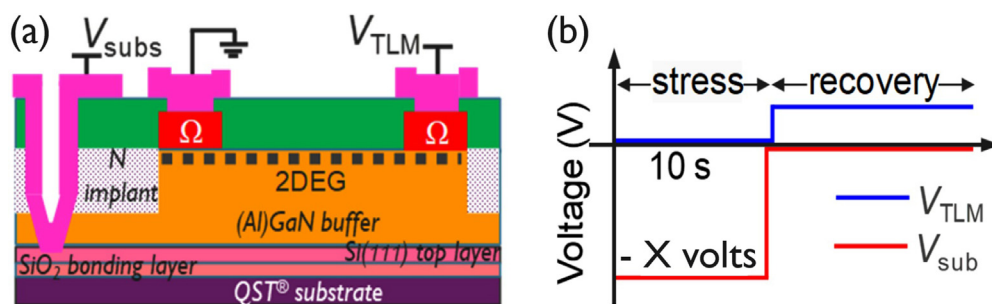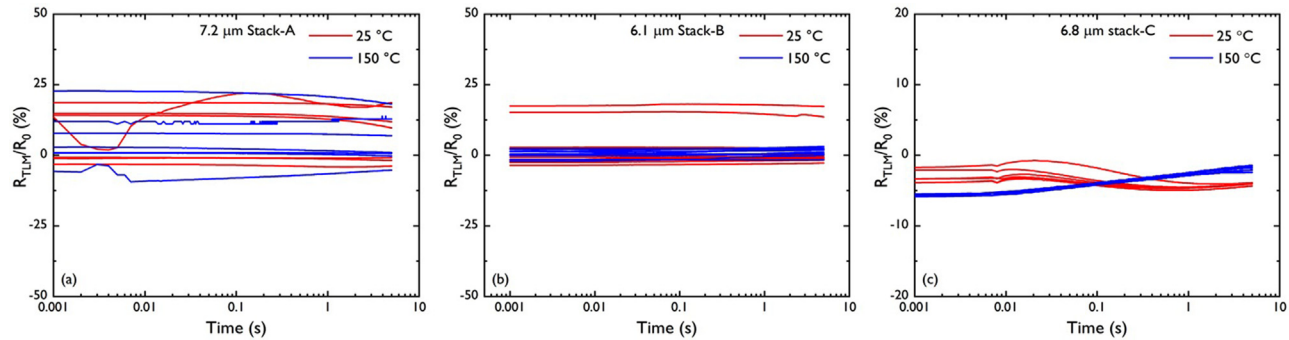

FIG. 7. (a) Test structure and (b) test procedure to measure buffer dispersion. X varies from −650 to −1200 V depending on the stack thickness.

FIG. 8. Buffer dispersion and recovery of (a) 7.2 μm stack A, (b) 6.1 μm stack B, and (c) 6.8 μm stack B at 25 and 150 °C after (a) −1200 V/10 s, (b) −900 V/10 s, and (c) −1200 V/10 s back-gating stress on the Si (111) device layer, respectively.

computer aided design simulations to study the physical mechanisms impacting the buffer dispersion and the I-V characteristics by insertion of bottom C-GaN and AlGaN interlayer.

To summarize, buffer stacks targeting higher vertical buffer breakdown were developed on commercially available poly-AlN (QST®) substrates. The target $V_{BD} >1200$ V was reached with 7.2 μm epitaxial intrinsically C-doped stack A. Stacks with intrinsic C-doping suffer from non-uniform V_{BD}. We demonstrated that by introducing an external C source during epitaxial growth, the uniform and symmetric buffer leakage in forward and backward bias conditions is reached with a buffer dispersion below 7%, both at 25 and 150 °C. These extrinsically C-doped buffers of 6.8 μm-thick can be used for applications above 1000 V. In the future work, a slight increase in the total buffer thickness is planned in order to reach the +1200 V target.

See the supplementary material for more information on V_{BD} comparison between Si and QST®.

AUTHOR DECLARATIONS
Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Anurag Vohra: Formal analysis (lead); Investigation (lead); Writing – original draft (lead); Writing – review and editing (lead). **Karen Geens:** Formal analysis (supporting); Investigation (supporting). **Ming Zhao:** Formal analysis (supporting); Investigation (supporting). **Olga Syshchyk:** Formal analysis (supporting); Investigation (supporting). **Herwig Hahn:** Formal analysis (supporting); Investigation (supporting). **Dirk Fahle:** Formal analysis (supporting); Investigation (supporting). **Benoit Bakeroot:** Formal analysis (supporting); Funding acquisition (supporting); Investigation (supporting); Resources (supporting). **Dirk Wellekens:** Data curation (lead).

Benjamin Vanhove: Data curation (supporting). **Robert Langer:** Project administration (supporting); Resources (supporting). **Stefaan Decoutere:** Funding acquisition (lead); Project administration (lead).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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