A Holistic Evaluation of Buried Power Rails and Back-side Power for Sub-5nm Technology Nodes

S. S. Teja Nibhanupudi, *Student Member, IEEE,* Divya Prasad, Shidhartha Das, Odysseas Zografos, Alex Robinson, Anshul Gupta, Alessio Spessot, Peter Debacker, Diederik Verkest, Julien Ryckaert, Geert Hellings, James Myers, Brian Cline, and Jaydeep P. Kulkarni *Senior Member, IEEE*

***Abstract*—Buried power rail and back-side power delivery grid have been proposed as solutions to scaling challenges that arise beyond the 5nm technology node, mainly to lower IR drop and further shrink area. This paper demonstrates a holistic evaluation of this technology and its variants at the microprocessor level. This is carried out by taking a Arm® Cortex®-A53 design through the standard-VLSI physical design implementation flow on Imec's iN6 node, equivalent to the industry 3nm technology node, which features the buried power technology. The power, performance, area, on-chip IR drop, off-chip voltage droop metrics are benchmarked, and implications on power gating are explored. An extensive Design-Technology-Co-Optimization study of the back-side power grid is presented to enhance the decoupling capacitance by sweeping associated technology parameters showcasing further optimization opportunities in manufacturing. The conclusions of this work highlight that the front-side power delivery network with buried rails achieves a 25% lower on-chip IR drop and 17% lower off-chip voltage droop (power supply noise) resulting in 21% lower guard band voltage. On the other hand, the back-side power grid with buried power rails achieves 85% lower on-chip IR drop and 30% off-chip voltage droop resulting in 60% lower guard band voltage. In addition, the impact of buried power rails and back-side power grids on power gated designs are evaluated.**

I. Introduction

Traditional dimension scaling in semiconductor technology nodes has been achieved by scaling of metal pitch (MP) and contacted poly pitch (CPP). In the advanced CMOS technology nodes (sub-10nm), the metal half-pitch has scaled to very narrow dimensions (sub-20nm) [1]. At these metal line widths, the resistivity of the metal increases significantly due to increased size-effects of wires such as surface and grain-boundary scattering [2]. The increased resistivity aggravates the IR drop problem and has become a significant bottleneck in high-performance designs at sub-5nm CMOS technology nodes. To ensure a lower IR drop, designers are often forced to trade-off signal routing resources to build finer, robust power grids. Buried power rails have been recently proposed as a technology booster for sub-5nm CMOS nodes to enable standard cell area scaling and to lower the IR drop problem [3]-[4]. In this technology, the power rails (e.g., VDD, VSS) are buried within the silicon substrate and tapped through special vias to connect to the power grid (front- or back-side). The buried power rails with high aspect ratio minimize the IR drop by allowing a lower-resistance path for power delivery to the transistors [5].

In addition to on-chip IR drop, parasitic effects introduced by the other components of the power delivery network such as PCB, package, C4 bumps, etc., induce voltage droop upon transient current spike events [6]. This off-chip voltage droop can be lowered by increasing the on-chip decoupling capacitance. In the Buried rail technology, since the metal lines are routed beneath the substrate where no signals are routed, low-resistance high-aspect-ratio power rails can be realized. The high-aspect-ratio helps increase the decoupling capacitance between supply and ground, thus lowering the off-chip voltage droop associated with spontaneous current spike events.

In this paper, we present a holistic evaluation of the buried power rails and back-side power grid by considering three power delivery network (PDN) configurations - conventional PDN named front side (FS), front side power delivery with buried power rails (FSBPR), and back-side power delivery with buried power rails (BSBPR). These configurations are evaluated to quantify the impact on Performance-Power-Area (PPA), on-chip IR drop, off-chip voltage droop and power gating using a representative 64-bit CPU such as Arm® Cortex®-A53 CPU. Previous studies in this domain focused either on physical design [4] or PDN modelling [7]

Our main contributions in this paper are as follows:

- Comprehensive analysis elaborating on the critical trade-offs between microprocessor performance and on-chip IR drop for different PDN configurations presented in our previous work [5].
- Holistic Design-Technology-Co-Optimization (DTCO) study of the back-side power delivery network through sweeping technology parameters to optimize both on-chip IR drop and off-chip voltage droop.
- Evaluating potential challenges involved in the integration of power gates with buried power rails and back-side power grid technology. Extensive analysis highlighting the impact of buried power rails on local power grid resistance.

The rest of the paper is organized as follows. Section II provides an introduction to the concept of buried power rails and back-side power delivery. Various power delivery configurations are described in Section III. Section IV presents the results for CPU design, on-chip IR drop, off-chip voltage droop, and gated power grid design. Section V presents a summary and conclusion.

S.S.Teja Nibhanupudi and Jaydeep P. Kulkarni are with the Department of Electrical and Computer Engineering, University of Texas at Austin, Austin, TX, 78712 USA e-mail: subrahmanya_teja@utexas.edu, jaydeep@austin.utexas.edu Divya Prasad, Shidhartha Das, Alex Robinson, James Myers and Brian Cline are with ARM Research, Austin, TX, USA. Odysseas Zografos, Anshul Gupta, Alessio Spessot, Peter Debacker, Diederik Verkest, Julien Ryckaert, and Geert Hellings are with IMEC Leuven, Belgium.

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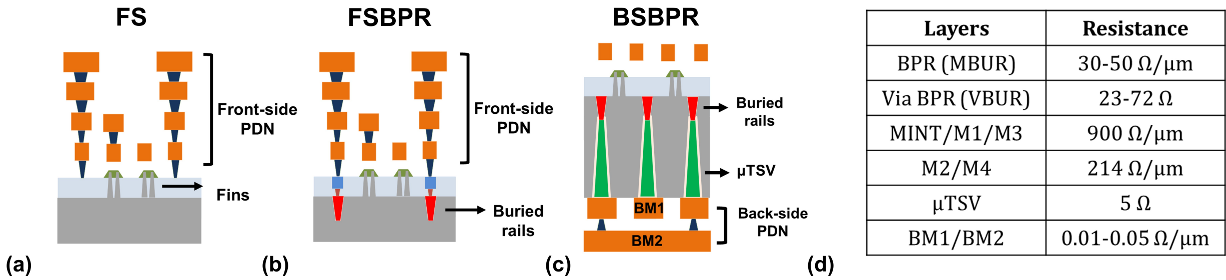

Layers	Resistance
BPR (MBUR)	30-50 Ω/µm
Via BPR (VBUR)	23-72 Ω
MINT/M1/M3	900 Ω/µm
M2/M4	214 Ω/µm
µTSV	5 Ω
BM1/BM2	0.01-0.05 Ω/µm

Fig. 1: (a) Front-side power delivery network schematic (b) Front-side power delivery with buried power rails schematic (c) Back-side power delivery with buried power rails schematic (d) Table showing the resistance of critical metal layers.

II. TECHNOLOGY DETAILS

A. Buried Power Rails

Buried power rails can be implemented in the FinFET technology at the cell boundaries [4]. After fin formation, the BPR process modules begin by etching a cavity in the Shallow-Trench-Isolation (STI) extending into bulk silicon. This is followed by atomic-layer-deposition (ALD) of a thin dielectric barrier layer to isolate the buried rail from the Si bulk electrically [8]. The cavity is then filled with metals that can withstand FEOL thermal budgets such as Ruthenium (Ru) or Tungsten (W) and capped for further FEOL integration. Experimentally demonstrated buried power rails exhibit resistances between 30Ω/µm and 50Ω/µm [4].

B. Back-side Power delivery

Back-side power delivery is a unique 3D-integration technique wherein the entire power delivery network is integrated on the back-side of the chip [9]. Fine pitch micro-Through-Silicon-Vias (µTSV) connect the buried power rails to the PDN on the back-side. After the processing on the front side, the wafer is thinned to 500nm, and µTSVs are etched from the back-side, using the BPR metal as an etch stop layer [10]. This is followed by the deposition of the back-side metal layers to distribute the power to C4 bumps. Recent studies have successfully demonstrated functional transistors powered through back-side power grid [11].

III. POWER DELIVERY NETWORK CONFIGURATIONS

In this paper, we explore three different power delivery configurations; namely,

- Front-Side (FS) where the signal and power nets are routed on the front side of the chip (Fig.1(a))
- Front-Side power delivery with Buried-Power-Rails (FSBPR) which is similar to FS except that the power supply tracks for the standard cells are buried within the substrate (Fig.1(b))
- Back-side power delivery with Buried-Power-Rails (BSBPR) where the power nets are routed on the back-side of the chip but the signal nets are routed on the front side of the chip (Fig.1(c))

A. BPR Standard cell design and metal interconnect

To evaluate the system-level impact of buried power rails, standard cells in IMEC's-iN6 technology node (equivalent to IRDS 3nm [1]) have been designed with and without incorporating the buried power rails. The FS configuration is implemented through conventional design flow using standard cell library without BPR. The FSBPR/BSBPR configurations use the standard cell library implementing BPR technology along with modified standard-cell layout, technology LEF (Library Exchange Format), and interconnect RC files which capture the effect of BPR. The standard cells in this technology node are 6-track high with 4-tracks reserved for routing and 2-tracks for power rails. Although BPR can enable standard cell height scaling to 5-tracks, this work considers only 6-track high cells. This enables fair and effective evaluation of just the buried rail as a technology booster for advanced nodes from IR drop perspective. The iN6 technology has a 14-metal layer interconnect stack: M1-M13 and MINT (intermediate metal layer in iN6 technology node for local routing), with interconnect pitches representative of ∼3nm technology node with a single Re-Distribution layer (RDL) to connect the C4 bumps. The FSBPR and BSBPR configurations have an additional buried metal layer (MBUR). Figure.1(d) presents the resistance of some of the fine pitch metal interconnect layers.

B. Frontside/Conventional PDN (FS)

In the FS configuration, the power supply tracks reside on the MINT metal layer (first BEOL metal-layer below M1). The small MINT metal pitch (∼22nm) results in highly resistive

PDN configuration	PDN design	Layers	VDD-VSS pitch
FS (FSBPR)	PDN1 (PDN4)	M3-M4 M7-M13	32CPP 32CPP
	PDN2 (PDN5)	M3-M4 M7-M13	16CPP 16CPP
	PDN3 (PDN6)	M3 M4 M7-M13	16CPP 8CPP 16CPP
BSBPR	PDN7	µTSV BM1 BM2	2µm 2µm 2µm
	PDN8	µTSV BM1 BM2	750nm 750nm 2µm
	PDN9	µTSV BM1 BM2	500nm 500nm 2µm

TABLE I: PDN configuration specifications (CPP=45nm)

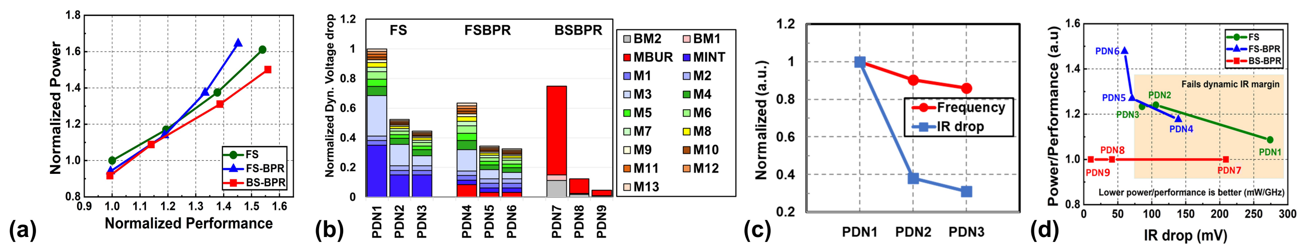

Fig. 2: (a) Normalized power vs. performance [5] (b) Layer-based IR drop distributions for PDN1-9 (c) Frequency and IR drop variation for PDN1-3 (d) Energy vs. dynamic IR drop for all the PDN configurations. [5]

power rails with resistance about 900Ω/µm [12], resulting in IR drop hot spots in the CPU design, as will be discussed in subsequent sections. To study the impact of PDN design on performance/IR drop, three different PDN designs are considered with increasing power grid density (PDN1 having the sparsest and PDN3 having the densest). Table.1 presents the specifications of each of the PDN designs for the FS configuration. Each of the three PDN designs dedicates four metal layers (M1, M2, M5, M6) for enabling local signal routing. The power grid on these four metal layers is only restricted to the via structure (no metal stripes on these layers).

C. Front-side PDN with Buried Rails (FSBPR)

The power rails of standard cells use the MBUR layer (buried metal layer) in the FSBPR configuration. The access to the buried power rails is restricted to specific "tapping" points where the dielectric is etched to create special vias (buried via - VBUR). These special vias are embedded within dedicated tap-cells carefully placed across the design. The tap cells consume additional area and obstruct the placement of the standard cells in the design. Therefore the placement of tap-cells is a crucial design constraint in FSBPR designs. Similar to FS configuration, three PDN designs are considered (PDN4-PDN6) for FSBPR configuration, as presented in Table.1.

D. Back-side PDN with Buried Power Rails (BS-BPR)

The BSBPR configuration eliminates the overhead due to tap-cells needed in the FSBPR configuration. It reduces the wiring congestion on the front side since all the metal resources can be dedicated to signal/clock routing. However, the signal I/Os would have to pass through the back-side of the chip along with power rails to finally connect to C4 bumps [13]. The additional parasitic capacitance induced by BPR and µTSVs can be compensated using technology innovations [13]. In recent years, this configuration has gained attention (even from semiconductor companies) owing to the tremendous potential of realizing low-power chips [14]. In this study, the power delivery network on the back-side is limited to 3 metal layers (MBUR: Buried metal, BM1:back-side metal-1, BM2:back-side metal-2). Additional layers can be added on the back side if required by the design specifications. Since the back-side metal stack is dedicated to power-ground routing, metal interconnects can have large track widths ($>$ 250nm), which can significantly lower the resistance of the grid. The IR drop is reduced as the µTSV pitch reduces but at the cost of increased process complexity. To study the impact of µTSV pitch on the IR drop, three PDN designs are considered in this study with decreasing µTSV pitch (PDN7 having the largest and PDN9 having the smallest) as presented in Table.2.

IV. RESULTS

A. CPU Performance and IR drop

To evaluate the system-level impact of the different PDN configurations, physical design implementation of a representative 64-bit high-efficiency CPU such as Cortex-A53 is realized using imec's iN6 library. The designs have a single power domain (VDD=0.7V) and are compared under iso-area conditions (die area - 150um x 150um). Figure.2(a) shows the power vs. performance of the chip for the three PDN configurations. The implementations that utilize the BSBPR configuration consume lower power than the FS/FSBPR configurations across the entire range of design frequencies due to the significantly reduced routing congestion. In comparison, the FSBPR configuration consumes higher power compared to FS configuration due to the overhead created by tap-cells. Overall for an iso-frequency of 1.4 (normalized units), the FSBPR consumes 10% higher power, and BSBPR consumes 8% lower power than FS configuration.

The placed and routed physical design of the Cortex-A53 CPU is used for vector-less dynamic IR drop analysis in the Cadence Voltus environment [15]. Figure.2(b) shows the layer-based distribution of IR drop for each of the 9 PDN designs (Table.1). In the FS configuration, the highly resistive local metal layers (MINT-M3) contribute about 60% of the IR drop in PDN1 with 32CPP pitch. This significant IR drop in the local metal layers is reduced to half in PDN2 with 16CPP metal pitch. The IR drop is further reduced by specifically reducing only the M4 metal pitch to 8CPP in PDN3. The denser M4 metal pitch reduces the IR drop on the highly resistive M3 metal layer. In the FSBPR configuration, the less resistive MBUR layer (30Ω/µm) replaces the highly resistive MINT layer (900Ω/µm). This reduces the overall IR drop in the FSBPR configuration by $\sim$ 30% across all the three PDN designs (PDN4, PDN5, PDN6). The BSBPR configuration IR drop is strongly dependent on the µTSV pitch. Although the MBUR has low resistance (30Ω/µm), increasing the µTSV pitch significantly increases the voltage drop on MBUR layer compared to the less resistive back-side metal layers (BM1, BM2).

Figure.2(c) shows the variation in maximum achieved frequency and IR drop for the three PDN designs in the FS configuration. As expected, the IR drop and the maximum achieved frequency reduce as the power grid density increases.

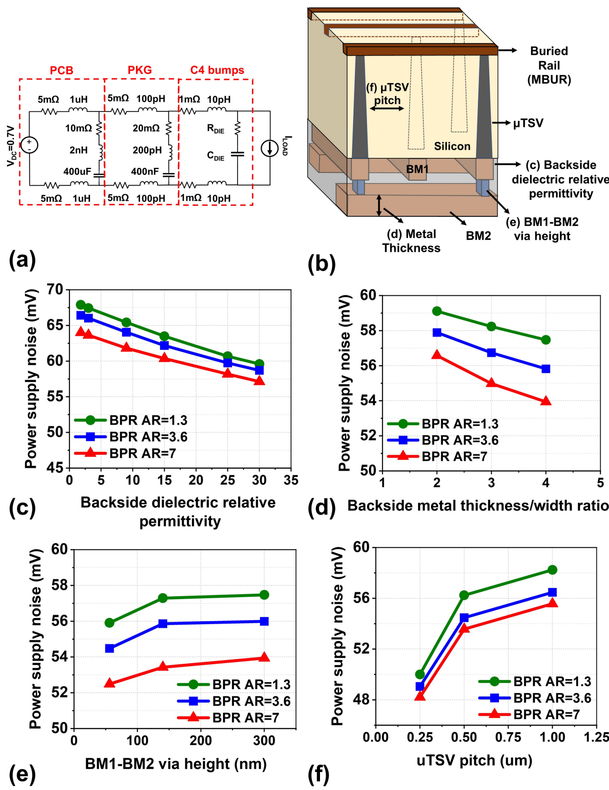

Fig. 3: (a) Equivalent circuit model for chip-package-PCB system (b) illustration of possible optimizations in BSBPR. Power supply noise variation with (c) back-side dielectric relative permittivity (d) back-side metal thickness-to-width ratio (e) BM1-BM2 via height (f) µTSV pitch

The performance degrades by 30%, and the IR drop improves by 70%, moving from PDN1 to PDN3. A similar trend is observed for the PDN designs when implemented using the FSBPR configuration. Figure.2(d) summarizes the trade-off between power/performance and IR drop for all the PDN designs considered in this study. The power divided by performance metric (mW/GHz) estimates the energy loss to lower the IR drop in different PDN configurations. Despite the increased energy loss incurred while moving from PDN1 to PDN3, the FS configuration does not meet the IR drop target. The FSBPR configuration, although meets the IR drop target, it experiences higher energy loss due to the overhead of the tap cells. On the contrary, the BSBPR configuration completely decouples this trade-off and does not incur any energy loss to lower the IR drop.

B. Off-chip voltage droop analysis

The IR drop analysis presented in section IV-A is limited to on-chip power delivery network. However, the chip-package-PCB parasitics induce power supply noise (off-chip voltage droop) during transient current spike events. The power supply noise is estimated by simulating the equivalent circuit shown in Figure.3(a) [6]. This power supply noise can be lowered by increasing the on-chip decoupling capacitance [6],[16].

The buried power rails increase the decoupling capacitance as they are enclosed in relatively high permittivity material (Silicon: k $\sim$ 11.7) compared to inter-layer dielectric (k $\sim$ 1.8). The buried rail thickness is also higher than local metal layers (M1-M6) which enhances the sidewall decoupling capacitance.

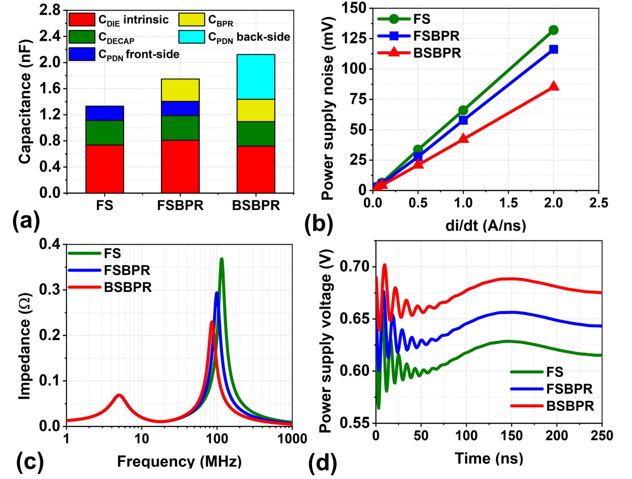

Fig. 4: (a) Decoupling capacitance comparison highlighting the contribution of different components (b) Power supply noise variation with rate of change of current for step input (c) Impedance profile of the die-package-PCB system (d) Voltage transient upon transient current spike event.

The resistance/capacitance of the buried rail and rest of the PDN are obtained using Synopsys Raphael RC extraction engine. The increased decoupling capacitance due to buried rail lowers the power supply noise (magnitude of first voltage droop) by 17% in FSBPR compared to FS configuration. The simulations have been conducted considering an 8-core configuration with one core switching and the other cores providing useful decoupling capacitance. In the BSBPR configuration, the power grid on the back side can be optimized independently to increase the decoupling capacitance and lower the power supply noise. The decoupling capacitance from the back-side power grid can be increased by,

- increasing back-side dielectric relative permittivity
- increasing back-side metal thickness
- reducing via height connecting back-side metal layers
- reducing µTSV pitch

These modifications are not possible in the FS/FSBPR configuration due to the risk of increasing signal-to-signal noise coupling. Therefore the BSBPR configuration provides this unique opportunity to increase the decoupling capacitance and reduce the power supply noise (magnitude of first voltage droop) without impacting the signal integrity. Figure.3(c) shows the variation of the power supply noise with the back-side dielectric relative permittivity for three different BPR aspect ratios. CMOS compatible high-k oxides such as Al_2O_3 (k$\sim$9) [17] or HfO_2 (k$\sim$23) [18] can replace the usually preferred low-k inter-layer dielectrics (k$\sim$1.8). The power supply noise is reduced by 12% by increasing the dielectric relative permittivity from 1.8 to about 25. Increasing the back-side metal thickness increases the side-wall capacitance and reduces the power supply noise, as shown by Figure.3(d). Similarly, reducing the via height between the back-side metal layers increases the capacitance between BM1 and BM2 layers as shown by Figure.3(e). Further, reducing the µTSV pitch increases the sidewall capacitance and helps reduce the power supply noise. As shown by Figure.3(f) reducing the µTSV pitch from 1µm to 0.25µm reduces the power supply noise by 15%. Overall, the optimized BSBPR con-

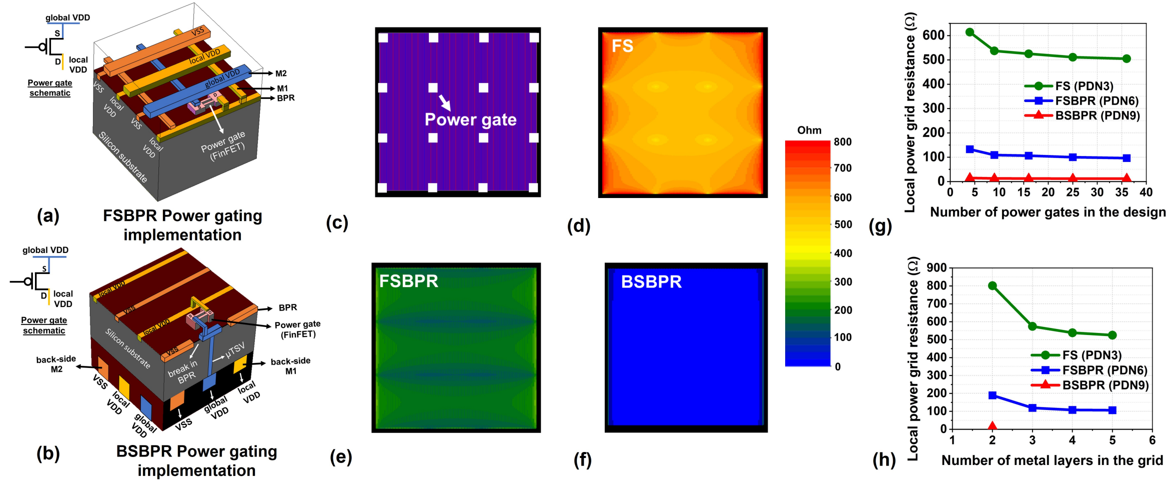

Fig. 5: Schematic showing (a) FSBPR power gate implementation (b) BSBPR power gate implementation. (c) Power grid map showing uniformly distributed power gate. Effective resistance heatmap of (d) FS (e) FSBPR (f) BSBPR PDN designs (g) Local power grid resistance variation with the number of power gates in the design (h) Local power grid resistance variation with number of metal layers in the power grid

figuration (dielectric permittivity=25, thickness/width ratio=3, via height=140nm, μTSV pitch=250nm) has 59% and 21% higher decoupling capacitance compared to FS and FSBPR configurations respectively. Figure.4(a) shows the decoupling capacitance contribution from various components of the on-chip PDN. Figure.4(b) shows the variation in power supply noise with the di/dt for the transient current spike event. The optimized BSBPR configuration has lower power supply noise compared to FS and FSBPR. In frequency domain, the peak impedance of BSBPR shifts to lower frequencies and the magnitude of the peak is reduced by 34% as seen from Figure.4(c). The corresponding time domain voltage transient simulated with step current input is shown in Figure.4(d). The waveform shows the worst-case instance experiencing dynamic IR drop (due to power grid resistance) superimposed by the power supply noise (due to off-chip voltage droop) for FS, FSBPR, and BSBPR configurations.

C. Power gate implementation

The on-chip IR drop and off-chip voltage droop analysis presented in sections IVA and IVB do not account for power gates in the design. However, most modern SoC modules implement power gating to minimize the leakage power consumed by inactive cores [19]. In the power gating technique, the local power grid (or power domain) is connected to the global power grid (main power supply) through switchable transistors called power gates. This subsection presents the impact of buried power rails on the designs employing the power gating technique. Figure.5(a) and figure.5(b) illustrate the potential power gate integration methodology for FSBPR and BSBPR designs, respectively. The standard cells and BEOL metal interconnects are omitted in the diagram for clarity. Also, the global VDD (main power supply), local VDD (power domain), and VSS interconnects are color-coded to match the power gate schematic (inset of fig.5(a),(b)). In the FSBPR configuration, the power gate is connected to the local VDD on the BPR layer (instead of the MINT layer for FS configuration). To facilitate this connection, the buried via (VBPR) needs to be accommodated within the standard cell of the power gate. In the BSBPR configuration, low resistance back-side metals are employed to implement both local and global power grids to minimize IR drop. The global VDD connects to the power gate through back-side metals and μTSVs. Since the μTSV needs BPR to land, the VSS buried power rail can be split to create an isolated global VDD BPR island, as shown in the figure.5(b). The drain of the power gate then connects to the local VDD BPR, which distributes power to the standard cells through the back-side metals.

Typically in power gating implementations, the global power grid is designed using higher (BEOL) metal layers (>M6 or M7), and the local power grid is designed using lower metal layers. The highly resistive local power grid contributes significantly to the overall IR drop of the design. Therefore, in this sub-section, the impact of buried rails on power gating designs is studied by considering the local power grid resistance. The local power grid resistance (for FS,FSBPR, and BSBPR designs) is analyzed using the Cadence Voltus simulation environment. The power gates are uniformly distributed across the chip area (fig.5(c)) and the effective resistance from the power gates to every standard cell is determined. Figure.5 (d),(e),(f) show the effective resistance heatmap for tight pitch PDN designs of each configuration: FS-PDN3, FSBPR-PDN6 and BSBPR-PDN9. The number of power gates required in a design is dependent on several factors such as power-gate resistance, operational frequency of the chip, input vectors etc.,. Therefore, we analyze the variation of peak resistance (worst-case located standard cell) with the number of power gates in the design as shown by Figure.5(g). Here an important trend can be observed, the resistance of the power grid reduces and saturates at a certain value for each configuration. This minimum limit is determined by the resistance of the lowest metal layer from the nearest via to the worst case standard cell (located half-way between two VDD lines). Since the resistance of MINT layer is high (MINT resistance is ∼30x MBUR resistance (fig.1(d))), the FS configuration local power grid resistance is 4.5x higher than FSBPR and 40x higher than BSBPR configurations.

In the FS/FSBPR configurations, the local power grid uses

PDN	Area	Frequency	Power	IR drop	Power supply noise	Local power grid resistance
FS	1x	1x	1x	1x	1x	1x
FSBPR	1x	1x	1.1x	0.75x	0.85x	0.25x
BSBPR	1x	1x	0.92x	0.15x	0.7x	0.02x

TABLE II: Comparison of important design metrics

up to 6 lower metal layers where most of the signals are also routed. If the local power grid resistance can meet the desired target resistance with fewer metal layers, additional metal layers can be exclusively allocated for signal routing and global power grid routing. Figure.5(h) shows the variation in local power grid resistance with the number of metal layers employed. The BSBPR configuration is shown with a single point since the local power grid is designed using the two available back-side metal layers. In the FS/FSBPR configurations the resistance reduces as the higher metal layers (having lower resistance) are added to the local power grid. As expected, the FSBPR local power grid has lower resistance than the FS local power grid. To meet the desired resistance target (derived from activity in the cores), the FSBPR power grid can employ fewer metal layers compared to an FS configuration. Overall, the FSBPR local power grids achieve ∼4.5x lower resistance compared to FS configuration local power grids owing to the enhanced current carrying capability of the buried power rails. Since very low resistive back-side metals are used to implement local power grid in BSBPR, the tight pitch PDN9 has ∼ 40x lower resistance compared to FS configuration. Overall, the low resistance BPR and back-side metal layers (fig.1(d)) can help alleviate the IR drop problem in power-gated designs.

V. Conclusion

A thorough PDN design study considering different possible power delivery configurations using buried power rail technology is presented. The system-level impact has been evaluated through physical design implementation of a 64-bit high-efficiency CPU such as Cortex-A53 at the sub-5nm node. The power, performance, IR drop metrics have been presented for the FS, FSBPR, and BSBPR configurations. The FSBPR and BSBPR configurations can lower the IR drop by 25% and 85%, respectively, compared to the FS configuration, thereby comfortably meeting the 10% IR drop target. Further, a unique method to enhance the decoupling capacitance of the BSBPR configuration is presented, resulting in 30% lower power supply noise consumption than the FS configuration. Finally, the impact of buried power rail on power gating implementation is presented. The local power grid resistance of FSBPR and BSBPR show ∼ 4.5x and ∼ 40x lower resistance compared to FS configuration.

VI. ACKNOWLEDGEMENTS

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