Single- Versus Multi-Step Trap Assisted Tunneling Currents—Part II: The Role of Polarons

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***Abstract*— Using the framework developed in the first part of this work, we demonstrate the capabilities of the extended two-state nonradiative multi-phonon (NMP) model by reproducing leakage current characteristics of two selected technologies. First, we identify the temperature-activated leakage mechanism in SiC/SiO_2 stacks using a tens of nanometer thick thermally grown oxide as trap-assisted tunneling (TAT) through defects. Interestingly, this effect can be reproduced with the same parameters in a SiC/SiO_2 stack with deposited oxide. Our simulations demonstrate that these charge transition centers are distributed within only a few nanometers from the SiC/SiO_2 interface. The low thermal activation of the leakage current is linked to the low relaxation energies of the involved traps compared with those typically involved in bias temperature instability (BTI) and Random Telegraph Noise (RTN). Second, a similar mechanism can explain TAT characteristics and transient charge trapping currents in Metal–Insulator–Metal (MIM) capacitors with a ZrO_2 insulating layer. By comparison of our model parameters to theoretical density functional theory (DFT) calculations, we identify self-trapped electrons (polarons) as a likely cause for these effects, as they have the required low relaxation energies.**

***Index Terms*— Device reliability, metal–oxide–semiconductor (MOS), nonradiative multi-phonon (NMP), SiC MOSFET, stress-induced leakage current (SILC), trap-assisted tunneling (TAT).**

I. Introduction

GATE leakage currents in 4H-SiC/SiO_2 MOSFETs and Metal Oxide Semiconductor Capacitors (MOSCAPs) used for high-voltage power switches in modern power conversion circuits have been reported frequently [1]–[3]. It is commonly assumed that trap-assisted charge conduction is responsible for the strong temperature activation of these leakage currents. These trap-assisted tunneling (TAT) currents have been observed for medium field strengths of $E_{ox} \approx 5\ MVcm^{-1}$ and above even for tens of nanometer thick SiO_2 layers on silicon carbide (SiC) substrates [3]–[6]. Also, other binary oxides with high electrical permittivity (e.g., HfO_2, ZrO_2) show thermally activated leakage currents [7]–[9], which limit their performance when used as dielectrics in logic and memory devices. Typically, analytical expressions are used to describe the TAT currents [10], neglecting the details of the underlying physical mechanism. The identification of the current conduction mechanism and the involved electrically active defects can help optimize the device design and processing to limit the additional power dissipation and dielectric degradation over the device lifetime due to these leakage currents. Therefore, we aim to identify the underlying mechanisms that cause the transient gate leakage currents in a SiC/SiO_2 metal–oxide–semiconductor (MOS) using physically reasonable defect parameters using the model derived in part I of this work [11]. In addition, we demonstrate the capability of our modeling approach to reproduce two different trap-assisted conduction mechanisms by explaining the measured leakage currents in a TiN/ZrO_2/TiN (TZT) structure used for storage capacitors in dynamic random access memory (DRAM) with improved accuracy compared with the original work [9].

For the simulation of the tunnel currents, a generic model is required to reproduce:

1) the *field dependence* of the current;
2) the *temperature activation* of the current; and
3) the *transient shape* of the current due to charge transfer kinetics,

as well as to account for the *shift of the threshold voltage* due to captured charge. Furthermore, a physical modeling approach should use *defect parameters consistent* with experimental observations and/or *ab initio* predictions. In addition to fulfilling these requirements, our model is inherently capable of calculating gate current variability. The extracted defect parameters required to reproduce the experimental data are compared with those predicted by first-principle methods for self-trapped electrons in these dielectrics. The consistency between our model parameters and our density functional

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theory (DFT) predictions suggests that these self-trapped electrons (polarons) are the root cause of the observed TAT currents. In particular, the substantially smaller relaxation energies compared with other oxide defects and a shallow acceptor-like trap level are characteristic for these polarons.

II. Simulation Results

In this section, we use our approach to explain the conduction mechanism based on mainly nonradiative multi-phonon (NMP) charge transitions in oxide defects. The parameters to describe these charge transition kinetics are extracted by calibrating our model to the measurement data. The time-zero leakage mechanism in the SiC/SiO_2 MOS structure (Technology 1) is thereby revealed to be trap-assisted. In addition, we identify different TAT current mechanisms in the TZT capacitor (Technology 2). The capability of the model to inherently account for multiple tunneling mechanisms is thereby demonstrated, and the parameters used in the simulations are linked to those extracted from *ab initio* calculations.

A. Technology 1–Poly-Si/SiO_2/SiC MOS

1) Simulation: Recently, Moens *et al.* [6] reported temperature-activated gate currents in SiC MOSCAPs with a thermally grown SiO_2 of thickness $t_{diel} = 53$ nm on an n-doped ($N_D = 1 \times 10^{16}\,cm^{-3}$) 4H-SiC with an n^+-doped poly-Si gate contact. The thermal activation of their measured gate tunneling currents at oxide fields between $E_{ox} = 5$–8 MVcm^{-1} exceeds the values typically observed for Fowler–Nordheim (FN) tunneling, while above 8 MVcm^{-1} FN tunneling accounts for almost the entire leakage current. The additional current at lower E_{ox} has been speculated to originate from a trap-assisted mechanism involving oxide defects in the vicinity of the conducting channel/oxide interface [6]. These defects can capture electrons from the channel and further emit them to the SiO_2 conduction band from where they drift quickly to the gate contact. For example, for a 100-nm layer, the transition time was estimated to be about 1 ps (drift velocity $v_D > 1 \times 10^7\,cm\,s^{-1}$ for $E_{ox} > 1\,MV\,cm^{-1}$ [13], while fast measurement setups are able to resolve currents at a high resolution in the μs range [14]. Since such a drift time is many orders of magnitude shorter than the timescales relevant for TAT current measurements they can be neglected. Therefore, the conduction mechanism can simply be modeled by accurately describing the tunneling probability in the NMP rates.

The material parameters for the SiC channel substrate and the SiO_2 layer were chosen based on [15] and [16]. Our simulation of the TAT currents reproduces the measured gate leakage current in both the regimes, with slopes significantly shallower and with larger thermal activation compared with the FN branch as shown in Fig. 1. Thereby, the hypothesis in [6] that the observed gate current is a result of electron capture from the SiC conduction band in combination with emission to the SiO_2 conduction band can be confirmed. Note that the trap occupation f_T at any (V_G, T) is negligibly low, which can be seen from the resulting threshold voltage shift ΔV_{th} in the mV regime shown in Fig. 2 ($f_T < 1 \times 10^{-2}$ for all defects at all (V_G, T), not shown). No significant charge build-up due to the defects responsible for the TAT current is therefore observed in the oxide and the transient current satisfies steady-state conditions at all times.

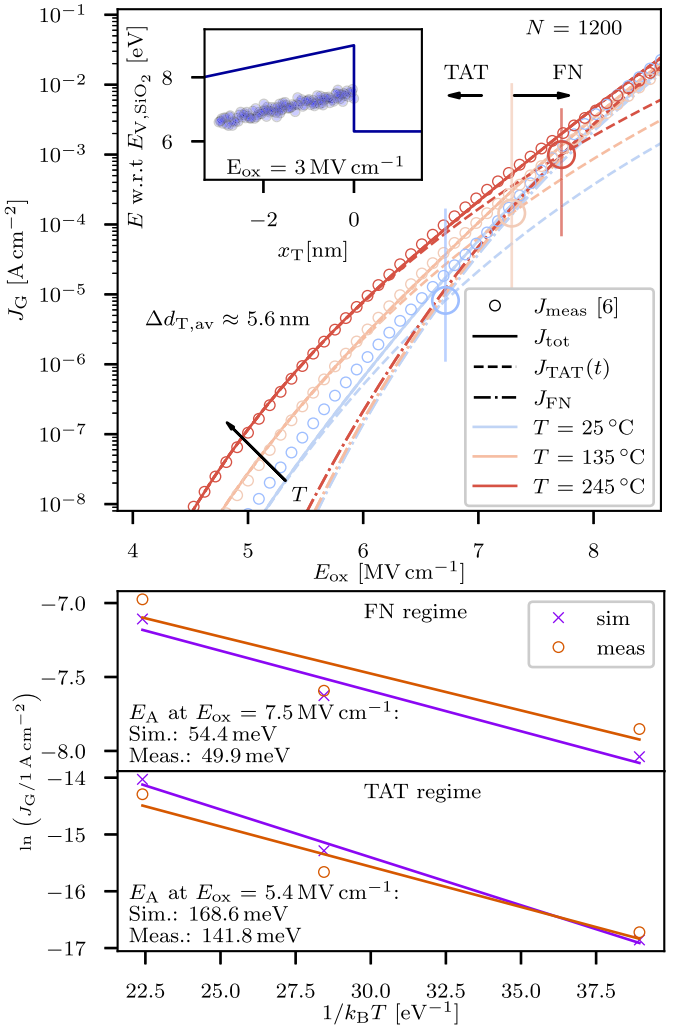

Fig. 1. Simulation results (lines) compared with measurement data (circles) of SiC MOSCAPs [6] **(top)**. The simulations can accurately reproduce the measurement characteristics. The calculation shows that the thermally activated leakage current can be explained by carriers tunneling from the substrate channel to traps located within 3 nm of the interface and then further to the conduction band of the insulator. The thermal activation of the trap-assisted current is well-reproduced by the NMP model as shown in the FN plots **(bottom)**. We remark that the tunneling current is non-Arrhenius and the estimated activation energies only approximations. At larger field strengths of about 7 MVcm^{-1} and above, FN tunneling dominates and is calculated using the Tsu–Esaki model [12].

TABLE I
NMP Parameters for Technology 1

Band	$\langle E_T \rangle$	σ_{E_T}	$\langle E_R \rangle$*	σ_{E_R}	x_T max.	N_T
TAT	2.85 eV	0.1 eV	0.89 eV	0.11 eV	3.0 nm	$7.6 \times 10^{18}\,cm^{-3}$
Polarons (DFT)	2.53 eV	0.23 eV	1.06 eV	0.23 eV	-	-

*$\langle R \rangle^{DFT}$ = 1.35 recalculated with the E_R-R correlation [18] for R = 1 as denoted in Fig. 6.

The defect parameters shown in Table I required to reproduce the gate current characteristics were extracted by

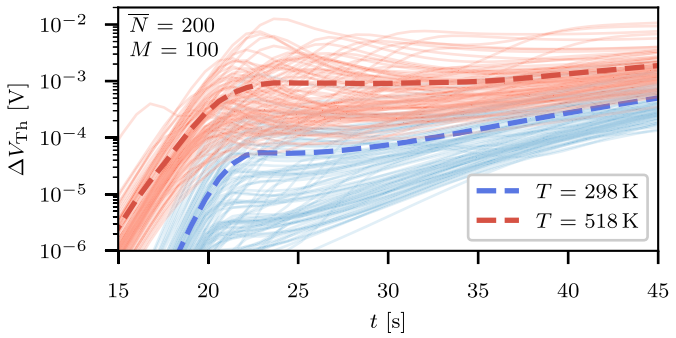

Fig. 2. Transient ΔV_{th} for $M = 100$ simulations with Poisson distributed number of defects $\overline{N} = 200$ with parameters of the extracted distribution (see Table I) **(solid)** together with the respective mean values **(dashed)**. ΔV_{th} as a measure of the average defect occupation is negligibly low for the demonstrated technology, as electrons captured from the channel by defects in its vicinity are almost instantly emitted toward the gate contact via the SiO_2 conduction band.

least-squares optimization taken between the measured and simulated gate currents on a logarithmic scale. The maximum distance in the x-direction from the interface was selected as $x_{\mathrm{T,max}} = 3$ nm, as an increase in this parameter had no impact on the simulation accuracy. Note that while this is the smallest maximum trap depth required to reproduce the measurement data, this does not implicate that the trap band is not distributed over the whole dielectric layer in a real device. This is emphasized in Fig. 3 which shows the defects within the sampled band that contribute to the total tunneling current at $T = 408$ K. While for lower gate bias the majority of the TAT current is conducted via traps with larger spatial distance to the channel/oxide interface, the distribution of the defects forming the percolation path broadens (e.g., more traps contribute to electron conduction) and shifts toward the interface in the simulation.

Such a conduction mechanism has already been suspected to be responsible for TAT in SiC/SiO_2 systems [1], [5]. Our spatial analysis of the leakage path supports the suggested "sweet spot" (certain trap level E_{T} and spatial location x_{T} required) hypotheses for traps enabling the conduction mechanism. In addition, Fiorenza *et al.* [4] have reported a similar mechanism but for negative bias in SiC pMOS devices subjected to an NO_2 post oxidation anneal (POA). It should be noted that for fields higher than 8–9 $\mathrm{MVcm^{-1}}$, impact ionization may play a crucial role in SiO_2 electron transport [17] and must be considered. To avoid this extra complication, we limit our fields to values smaller than 9 $\mathrm{MV\,cm^{-1}}$. Also, the time-zero modeling approach does not include defect generation and annealing as required for the description of stress-induced leakage currents (SILCs), but is considered to be negligible during short time gate bias sweeps in a pristine device.

2) Variability and Parameter Variation: With decreasing dielectric volume in scaled devices, only a small number of defects are present, assuming a constant defect density. This small number of defects can lead to a strong variability of possible conduction paths through the dielectric layer, depending on E_{T}, E_{R} and spatial location, as well as the actual number of defects in the device. To efficiently calculate TAT currents in large-area devices, a minimum number of defects should be used for the calculation that rebuilds the average current density in a large-area device. Fig. 4 shows how the gate-stack area influences the variability of our simulation result. The standard deviations emphasize that large $\overline{N}$ (i.e., large area) leads to relatively low variability (increasing with decreasing T); however, the expectation values (mean) still properly explain the data even with as few as $\overline{N} = 80$ defects sampled, when calculating $M = 100$ samples.

Next, the impact of the defect parameters on the TAT current is shown in Fig. 5. While an increase in the defect density N_{T} leads to a parallel shift of the device characteristics toward larger currents, a shift of the trap level E_{T} toward lower values will lead to a higher current at lower gate bias, as defects become aligned with the channel conduction band already at small V_{G}. Quite the contrary, charge hopping via defects to the conduction band of SiO_2 is observed only at larger V_{G} with defects having a higher E_{T}. As a result, the E_{T} alteration can lead to a strong variation in the shape of the I_{G}–V_{G} characteristics. Finally, a relaxation energy E_{R} modification toward lower values increases defect to defect and defect to reservoir coupling, leading to increased currents and lower thermal activation.

3) Chemical Composition of the Defects: Typically, defects considered responsible for charge trapping seen in bias temperature instability (BTI) and Random Telegraph Noise (RTN) [19] exhibit large E_{R} [20], [21], e.g., 1.5–4 eV. On the other hand, a suitable defect candidate for TAT currents in a-SiO_2 requires a relatively low E_{R}, around 1 eV. A self-trapped electron (polaron) structure shows such E_{T} and E_{R} values as obtained in atomistic studies for SiO_2 [22]–[24]. For instance, El-Sayed *et al.* [23] calculated E_{R} in the range of 0.72–1.7 eV for these elongated Si-O–Si bonds upon electron capture. As only a small number of structures were analyzed within this study, we extended these calculations to extract more accurate statistical properties of these defects.

For that, we prepared amorphous SiO_2 (a-SiO_2) models containing 216 atoms each by applying the established melt-and-quench technique within molecular dynamics to a $3 \times 3 \times 3$ supercell of β-cristobalite. The classical ReaxFF force field was used to describe the interactions in the SiO_2 system. Detailed descriptions of the procedure and the used parameters are discussed in [23]. The atomic positions and the cell vectors of the obtained structures were then relaxed further within DFT [25] so that the atomic forces were below 25 meV/Å and internal stress below 0.01 GPa. All DFT calculations were performed within the Gaussian plane wave method as implemented in the CP2K code [26] using the double-ζ Goedecker–Teter–Hutter [27] basis set for expanding the electron density and wave functions. To obtain an accurate electronic structure of the models, we used the nonlocal hybrid exchange correlation (XC) functional PBE0_TC_LRC [28], resulting in a single-particle bandgap of 8.1 eV in reasonable agreement with the experimental gap of a-SiO_2 thin films ($E_{\mathrm{g}} = 8.9$ eV). To mitigate the heavy computational costs of calculating the exact Hartree–Fock exchange integral, the *auxiliary density matrix Method* [29] was used to approximate the exchange with a small auxiliary basis set.

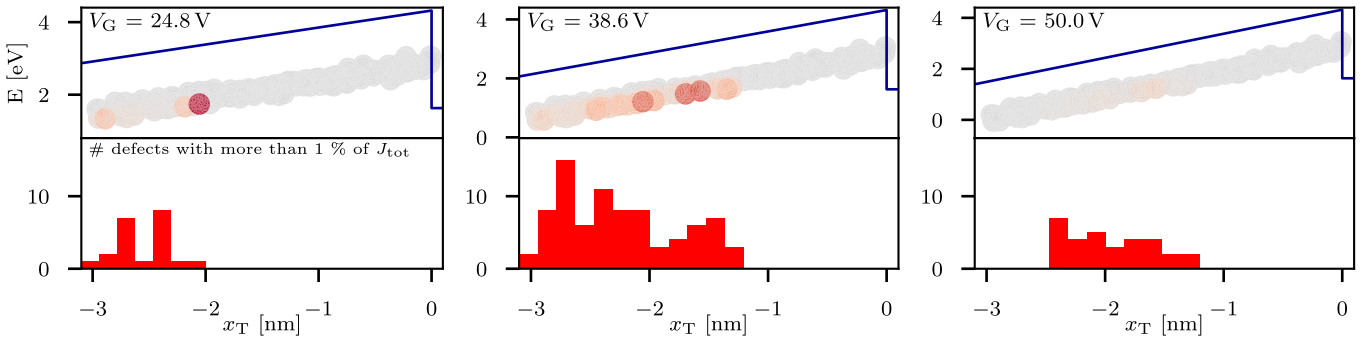

Fig. 3. Distributions of the total current over individual traps are shown for three different gate bias conditions at $T = 408$ K. The maximum depth required to explain the measurement data is $x_T \approx 3$ nm (tested by reducing the maximum trap depth distribution). This is most likely a result of the limited current measurement resolution and the minimum T selected for the experiment [6]. At lower bias, the majority of the current is conducted via traps between 2 and 3 nm from the SiC/SiO_2 interface, while at higher bias the conducting region shifts toward the interface.

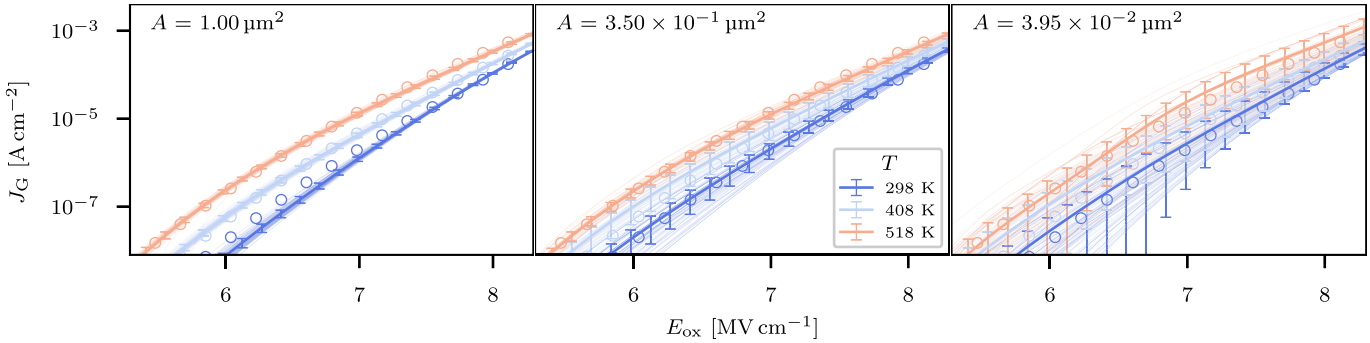

Fig. 4. Variance of the gate current for different device areas A_i as obtained by our model is shown for $M = 100$ devices each. The mean values (thick lines) are in good agreement with the experiment for a total gate area of $A = A_i M \approx 305 \times 10\ \mu m^2$, respectively **(left and center)**. However, the standard errors show a larger variance for the smallest area of $A = 3.95 \times 10^{-2}\ \mu m^2$ **(right)**. With a small number of $\overline{N} = 80$ defects per device only, the impact of the Poisson distribution becomes more dominant, while the mean values are still close to the measurements on large-area devices. Note that the simulation area is much smaller than a typical device area required for measuring leakage currents (above the fA regime).

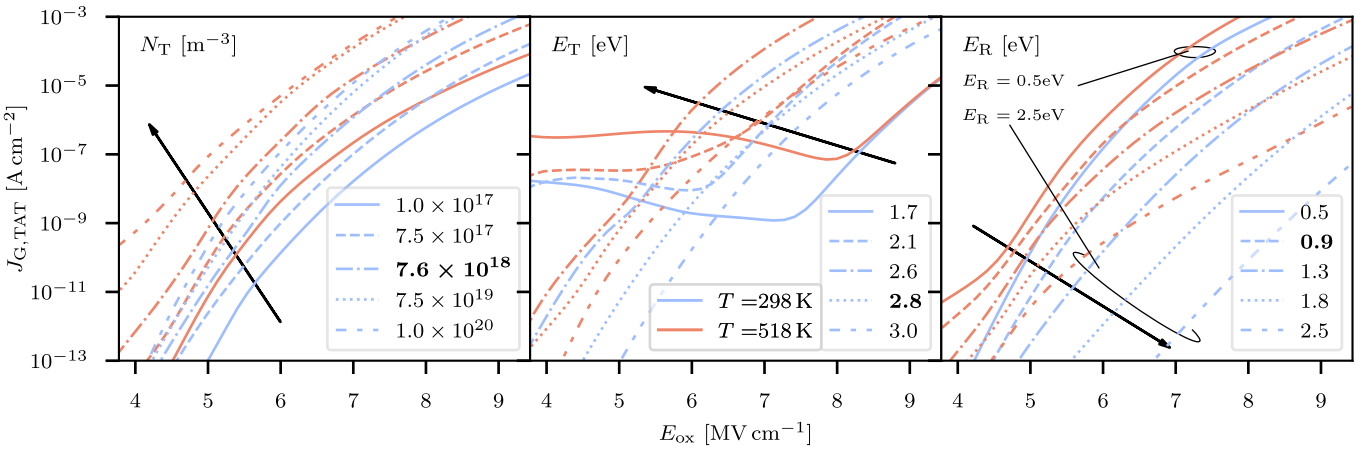

Fig. 5. Impact of the parameters on the total TAT current: N_T **(left)**, E_T **(center)** and E_R **(right)** for a wide range around the extracted defect parameters from Table I in **bold** for a constant defect number $N = 200$. While J_G scales with N_T, the shape of the characteristics is strongly influenced by the mean trap level E_T. A wide variation of E_R shows the strong influence of this parameter on the temperature activation of the current.

The disordered atomic structure gives rise to partially localized empty states close the SiO_2 conduction band edge. Polaron states in the structure can then be induced by injecting an electron into this state, leading to a structural relaxation accompanied by the collapse of the wave function onto a single Si atom [30] as shown in Fig. 6. The relaxation energy E_R is then given by the energy dissipated to the thermal bath during this relaxation. The thermodynamic charge trap levels of the polaron states were evaluated using the methodology presented in [31]. In addition, the Makov–Payne correction [32] was used to compensate for the spurious electrostatic self-interaction occurring in charged cells with periodic boundary conditions. The statistical distribution of the calculated charge transfer parameters shows reasonable

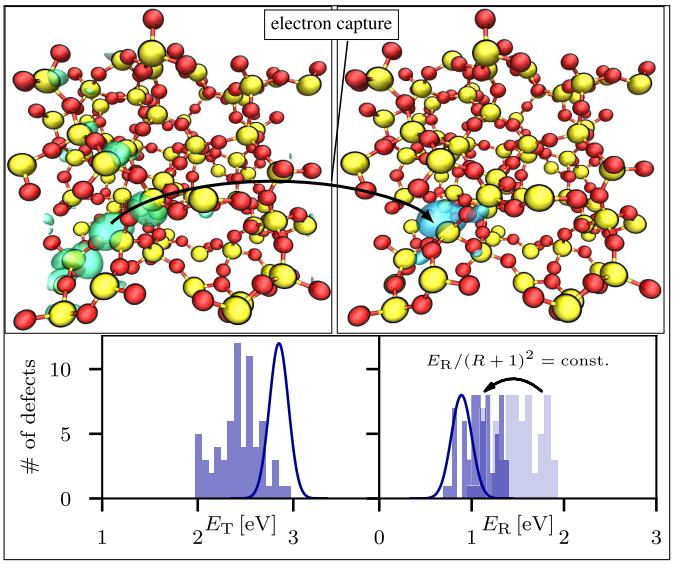

Fig. 6. Ball and stick model of an a-SiO_2 structure with Si (yellow) and O (red) showing the lowest unoccupied orbital **(top left)** and the corresponding localized wave function of the polaron upon electron capture **(top right)**. The elongated Si–O–Si bonds act as a trapping site here. The bottom panel shows a comparison of the associated charge transition parameters calculated with DFT (histogram) and the model value distributions required to explain the experimental data listed in Table I (lines).

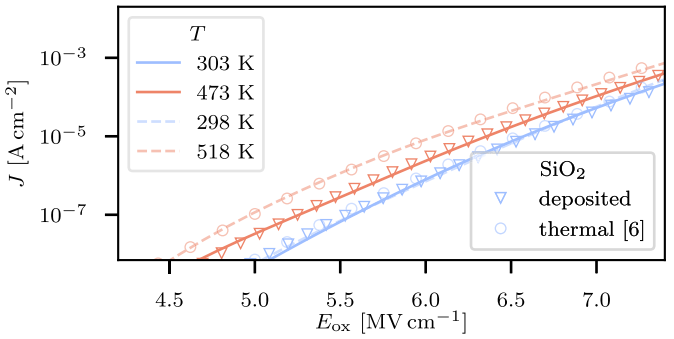

Fig. 7. Comparison of the tunneling current measured on a MOSCAP extracted from [6] with 53-nm SiO_2 **(circles and dashed lines)**, as calculated by our TAT and Tsu–Esaki model, with that of a nMOSFET using 70-nm deposited SiO_2 **(triangles and solid)** is shown. Both oxides show a comparable thermal activation of the tunneling currents, in both the TAT and FN regimes (compare Fig. 1).

agreement with those used for the TAT calculation within Comphy (see Table I and Fig. 6). Since the average curvature ratio $\langle R\rangle^{\mathrm{DFT}}$ in the resulting potential energy curves (PECs) calculated from DFT slightly differs from $R = 1$ used in the Comphy simulation, we recalculated the correlating $E_{\mathrm{R}}^{\mathrm{corr}}$ of the DFT calculation for $R = 1$, which is justified due to the correlation of these parameters shown in [18] and given by

$$\frac{E_{\mathrm{R}}^{\mathrm{DFT}}}{\left(R^{\mathrm{DFT}}+1\right)^2} = \frac{E_{\mathrm{R}}^{\mathrm{corr}}}{\left(R^{\mathrm{Comphy}}+1\right)^2} = \text{constant}. \tag{1}$$

Note that the agreement of both the shallow acceptor-like trap level and the low relaxation energy make such polarons a likely defect candidate for TAT in SiO_2.

4) Deposited Oxide: The oxide used in the investigated MOSCAPs is thermally grown and therefore potentially exhibits a different stochiometric composition compared with deposited SiO_2 as used for SiC trench MOSFETs. This distinct chemical composition together with a different SiC surface termination (a-face in trench, compared with Si-face in lateral devices) can facilitate or suppress defect formation when compared with the lateral MOSCAP. Therefore, we measured the leakage currents of a lateral MOSFET structure with gate area of $W \times L = 1.949$ mm^2 using SiO_2 deposited via chemical vapor deposition subjected to a subsequent post deposition anneal in a nitric-oxide (NO) ambient. While sweeping the gate from $V_{\mathrm{G}} = 20$–60 V at a sweep rate of about 33 mVs^{-1} with a step size of 0.01 V, the drain voltage was kept at 0.1 V while the source terminal was grounded for the sweep duration. Fig. 7 shows the measured gate currents on the lateral SiC/SiO_2 n-MOSFET with the slightly thicker oxide compared with the MOSCAP, together with a simulation with the same defect parameters as extracted from the MOSCAP leakage currents. A comparison regarding the thermal activation of the leakage currents reveals the same tunneling characteristics as a function of oxide field strength in both the structures. As a consequence, the time-zero gate leakage performance of the deposited oxide can be considered equal to that of the thermal grown oxide.

B. Technology 2–TiN/ZrO_2/TiN Capacitor

Metal–insulator–metal (MIM) capacitors using ZrO_2 as a high-k dielectric have been established as state-of-the-art DRAM storage capacitors [33]. However, they have shown increased thermally activated leakage currents [7], [34], which limit the further down-scaling of these devices. To explain the different slopes and thermal activation of the current characteristics at different oxide field strengths, Jegert *et al.* [7] suggested TAT conduction as the underlying mechanism. To investigate this hypothesis more closely, the second technology investigated in this work is a TZT capacitor with a $t_{\mathrm{diel}} = 8$ nm ZrO_2 layer stacked between TiN electrodes and an electrode area of about 1×10^{-4} cm^2, as reported by Padovani *et al.* [9]. In our simulation, we used the same material parameters for calculating the tunneling currents as the authors of the original study.

The observed tunneling current characteristics for the positive bias branch in Fig. 8 can be reproduced by the simulation using two trap bands with parameters listed in Table II. First, below voltages $V_{\mathrm{G}} \approx 1.7$ V between the two TiN electrodes, the leakage current shows *transient* charge trapping caused by defects exhibiting a relatively large E_{R} in the range of those known from defects considered responsible for charge trapping/BTI [20]. Although not shown in this work, the transient TAT currents at low V_{G} decrease with decreasing sweep rates as also stated in [7] or when maintaining a constant bias for a long time, as less charge can be captured at increased defect occupations. The maximum defect occupancy observed in the simulation leads to a shift of electrode voltage of ≈0.1 V that is needed to achieve the same electric field strength due to the accumulated charge and is integrated in a non-self-consistent

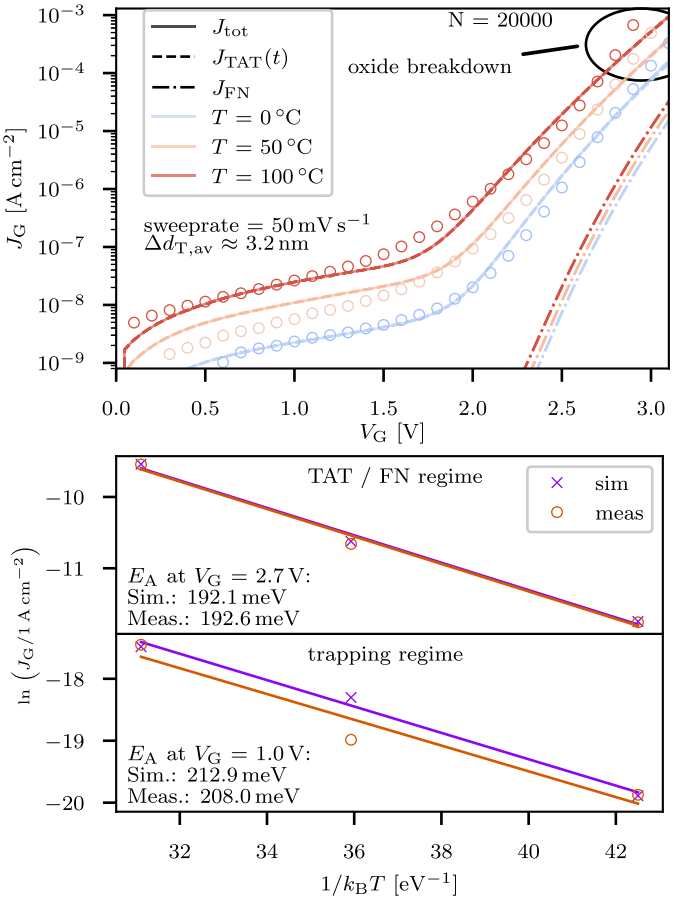

Fig. 8. MIM structures with single-layered ZrO_2 show two branches in the TAT currents. The low to medium electrode bias leakage currents up to $V_G \approx 1.5$ V appear due to charge captured from the channel in defects energetically aligned to the Fermi-level. This branch is not a steady-state current, but rather a transient current **(dashed lines)**. The second steeper branch above $V_G \approx 2$ V, on the other hand, shows TAT-FN characteristics in steady-state like the MOS structures shown in Fig. 1. The data have already been previously published in [9].

TABLE II
NMP PARAMETERS FOR TECHNOLOGY 2

Band	$\langle E_T \rangle$	σ_{E_T}	$\langle E_R \rangle$	σ_{E_R}	x_T max.	N_T
TAT	1.09 eV	0.1 eV	0.76 eV	0.1 eV	-	3×10^{19} cm^{-3}
Polarons (DFT)	1.24 eV	0.2 eV	0.7 eV	0.15 eV	-	-
trapping	0.35 eV	0.12 eV	2.6 eV	0.1 eV	-	6×10^{19} cm^{-3}

way within the Poisson equation in the calculation as described in [11]. Furthermore, the steep current branch above $V_G \approx 1.7$ V shows significant temperature activation. This branch is reproduced by the TAT/FN defect band with relatively low E_R in a comparable range as extracted for technology 1. These defects lead to a similar conduction behavior as described in Section II-A, in which the transient current calculation satisfies the steady-state condition.

Note that for $E_{ox} > 3.5$ MVcm^{-1} ($\approx V_G > 2.75$ V), the oxide starts to break down. As only preexisting defects are considered in the model, this mechanism is not covered in our simulation. In a similar fashion as in Section II-A, we created a-ZrO_2 models from $3 \times 3 \times 3$ cubic ZrO_2 cells using a Buckingham-like force field parameterized for describing

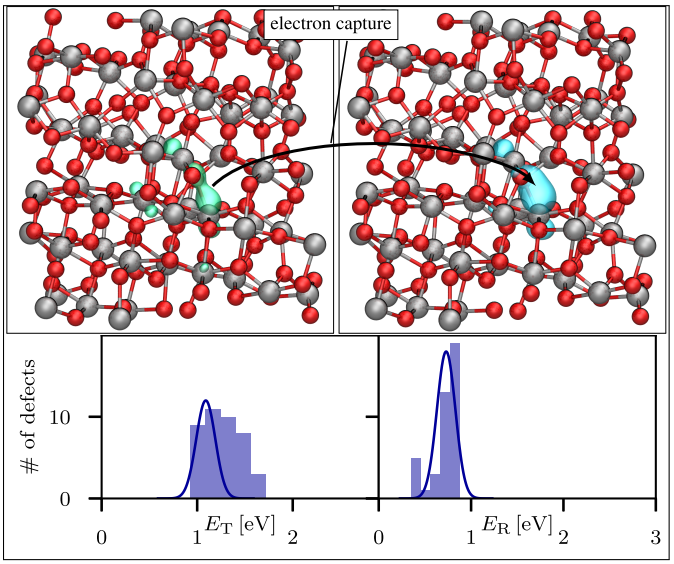

Fig. 9. Ball and stick model of the partially recrystallized ZrO_2 structure with Zr (gray) and O (red) showing the lowest unoccupied state **(top left)** and the corresponding localized wave function of the polaron upon electron capture **(top right)**. The bottom panel shows a comparison of the associated charge transition parameters calculated with DFT (histogram) and the model value distributions required to explain the experimental data listed in Table II (lines).

high-κ $ZrHfO_4$ alloys [35]. However, non-glass forming oxides like HfO_2 or ZrO_2 are known to easily crystallize (at least partially) during device processing conditions [36]. This effect has been captured using different quench rates ranging between 5 and 20 K/ps, leading to varying degrees of crystallinity within our model samples. The onset of crystallization can be seen in Fig. 9, where the lattice planes of the crystal are already established while local distortion of atomic positions is still present. Using the same DFT settings as for a-SiO_2, we obtain a theoretical bandgap of 5.9 eV in excellent agreement with the experimental values ($E_g = 5.8$ eV) [37]. As reported for other non-glassforming oxides [36], [38], we observe that sites with a locally reduced oxygen concentration act as precursor for an intrinsic electron polaron state. As in the case of SiO_2, our defect parameters derived from DFT are in excellent agreement with those used in the TAT calculation as shown in Table II.

C. Discussion

As a general conclusion, TAT conduction via polarons is in both the SiC/SiO_2/poly-Si system and the TiN/ZrO_2/TiN system enabled by a defect level situated between the conduction band edge of the reservoir electrode (substrate channel) and the insulator. Such a trap level and material configuration together with a low E_R can be considered a prerequisite for TAT in partly amorphous insulators, which is fulfilled by polarons, as their E_T will be close to the conduction band edge of the insulator with a relatively broad distribution, but not as close as in a crystalline material. For purely crystalline insulators, E_T of the polaron band shifts close to the insulator conduction band edge with discrete values, as schematically shown for a ZrO_2 layer in Fig. 10.

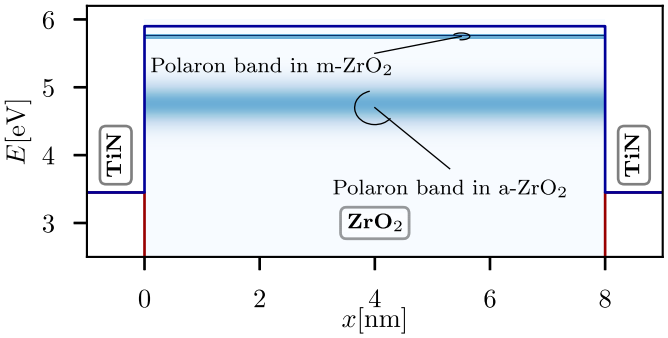

Fig. 10. Polaron defect band within amorphous ZrO_2 is schematically shown together with a polaron band the monolithic form of zirconia. The a-ZrO_2 polaron band shows a favorable E_T centered between the conduction band edges of the electrode and insulator with a broader distribution. Contrary, the m-ZrO_2 polaron band shows very narrow distributed E_T in close vicinity to the insulator conduction band edge.

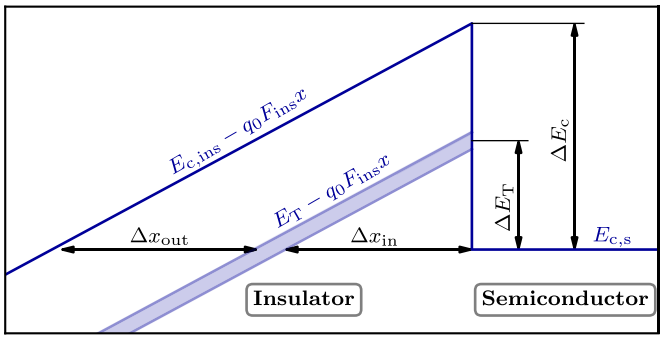

Fig. 11. Schematic representation of the energetic alignments of the conduction bands of a semiconductor/insulator material system together with a defect band that efficiently enables a TAT conduction path. At a given electric field F_{ins}, the distance of the input tunneling x_{in} must be sufficiently small and E_T must be aligned with the semiconductor Fermi-level to enable a steady-state current. As the output tunneling distance $\Delta x_{out} = \Delta x_{in}(\Delta E_c/\Delta E_T - 1)$, the energy ratio must be small enough to allow tunneling through the reduced barrier.

We expect these to be generic features of the polaron bands. Contrary to defects resulting from stoichiometric disorder, which are to be expected in higher densities only close to the interface, the polaron band is a bulk property and extends throughout the whole insulator. Also, the observation that in crystalline insulators the polaron band is narrow and close to the conduction band while in amorphous insulators it is deeper and considerably broader makes intuitively sense. To give some ballpark numbers on the requirements of TAT to be observed, it is a prerequisite that $\Delta E_T = E_T - E_{c,s}$ is sufficiently lowered by the electric field F_{ins} at a certain distance x_{in} to become zero, see Fig. 11. From $\Delta E_T - q_0 \Delta x_{in} F_{ins} = 0$ we obtain as a condition

$$\Delta E_T = q_0 \Delta x_{in} F_{ins}. \tag{2}$$

To observe significant TAT, Δx_{in} must not be too large, otherwise the tunneling factor will reduce the time constants and thus the current too much. Following similar arguments, the electron must than continue from the trap to the $E_{c,\text{insulator}}$ to lead to TAT, and we obtain

$$\Delta E_c = q_0(\Delta x_{in} + \Delta x_{out}) F_{ins}. \tag{3}$$

Although Δx_{out} could be slightly larger since the Wentzel-Kramer-Brillouin (WKB) barrier is smaller, it must be roughly on the same order of magnitude, so we simply assume $\Delta x_{in} = \Delta x_{out} = \Delta x$, which leads to $\Delta E_c = 2\Delta E_T$. Since F_{ins} must not be too large also to prevent oxide breakdown, we take $F_{ins} = 10\ \text{MVcm}^{-1}$, because even many good quality oxides break at higher fields. Together with $\Delta x = 2$ nm, we obtain $\Delta E_T = 2$ eV. Thus, as a requirement for TAT to be observed, both $E_T - E_{c,s}$ and $E_{c,ins} - E_T$ must be smaller than 2 eV and should be roughly in the same range. These assumptions can be considered valid provided that the relaxation energies of the defects are sufficiently small, which is the case for polarons.

III. Conclusion

Using a consistent set of material parameters and a reduced physical defect parameter set, we show that our model can explain TAT from the channel accumulation layer to the insulator conduction band in SiC/SiO_2 n-type MOSCAPs. Our simulations strongly support the original hypotheses presented by Moens *et al.* [6] that border traps close to the interface enable this TAT current. The defect parameters can consistently be converted into two-state PECs to describe both trap-to-reservoir and trap-to-trap charge transfer reactions. Our results suggest that the observed tunneling currents are a result of electron capture and emission at intrinsic defects (polarons), which is supported by our *ab initio* calculations. The same mechanism has been confirmed by our measurements on lateral SiC nMOSFETs. We further demonstrate that a transient charge trapping current in an MIM capacitor using ZrO_2 as an insulator can be explained by charge trapping. In addition, a similar steady-state current via the insulator conduction band as in the SiC/SiO_2 structure is explained by our model. The relatively low relaxation energy required to explain this TAT characteristics suggests the same defect class (polarons) to be responsible for the leakage current. Our *ab initio* calculations for polarons in ZrO_2 structures support this hypothesis with an excellent agreement in the parameters.

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