Journal of Applied Physics

RESEARCH ARTICLE | JULY 14 2022

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Journal of Applied Physics 132, 024302 (2022)
https://doi.org/10.1063/5.0092535

AIP Publishing

Journal of Applied Physics ARTICLE scitation.org/journal/jap

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Cite as: J. Appl. Phys. **132**, 024302 (2022); doi: 10.1063/5.0092535
Submitted: 23 March 2022 · Accepted: 24 June 2022 ·
Published Online: 14 July 2022

S. Ramesh,[1,2,a)] Ts. Ivanov,[2] A. Sibaja-Hernandez,[2] A. Alian,[2] E. Camerotto,[3] A. Milenin,[2] N. Pinna,[2] S. El Kazzi,[2] D. Lin,[2] P. Lagrain,[2] P. Favia,[2] H. Bender,[2] N. Collaert,[2] and K. De Meyer[1,2]

AFFILIATIONS

[1]KU Leuven, ESAT, Kasteelpark Arenberg 10, 3001 Leuven, Belgium
[2]IMEC, Kapeldreef 75, 3001 Leuven, Belgium
[3]Lam Research Belgium, Kapeldreef 75, 3001 Leuven, Belgium

[a)]**Author to whom correspondence should be addressed:** siva.ramesh@imec.be

ABSTRACT

In this paper, dry etched vertical nanowires (VNWs) are used in transmission line/transfer length analysis to study the contacts of gate-all-around devices for future technology nodes. VNW resistors with Mo and Pd based metal stack contacts to p-InGaAs show Schottky behavior, unlike the planar counterpart. The resistance for Mo contact is higher than Pd, however, Pd was found to form an alloy with InGaAs at temperatures as low as 190 °C, and the length of Pd diffusion into the InGaAs increased at smaller NW dimensions, hindering future scalability. The minimum extracted specific contact resistivity (ρ_C) values are $1.6 \times 10^{-5}\,\Omega\,\mathrm{cm}^2$ (Mo) and $4.2 \times 10^{-6}\,\Omega\,\mathrm{cm}^2$ (Pd) for a doping level of $1 \times 10^{19}\,\mathrm{cm}^{-3}$. An apparent dependence of ρ_C on the NW diameter was also observed. This has been attributed to the surface states under the un-gated region of NW devices and found to dominate at smaller diameters. An analytical model to account for such geometrical effects has also been developed and validated with technology computer-aided design simulations. The analysis presented in this paper effectively captures the 3D aspects of an NW contact at nanoscale dimensions and can be applied irrespective of the semiconductor and contact metal used.

I. INTRODUCTION

Metal-semiconductor contact at the source and drain (S/D) junction of a transistor is critical for the ON-state performance of the device, especially for nanowire MOSFETs with nanoscale junction dimensions. Literature studies suggest that the III–V nanowire (NW) devices show the potential to outperform state-of-the-art Si MOSFETs and gate-all-around nanowire field effect transistors (NWFETs).[1–6] For good performance, the series resistance of scaled MOSFETs will need to be well below $100\,\Omega\,\mu\mathrm{m}$.[7] However, contacts to III–V nanowire FETs show high resistance owing to the small contact area.[8] In addition, it is difficult to quantify the series/access resistance for vertical NW (VNW) devices due to the inherent asymmetry in S/D (bottom/top) contacts, unlike lateral MOSFETs,[9] causing the extraction techniques to fail.[10]

Ohmic contacts to planar III–V semiconductors have been studied and analyzed extensively in the literature.[11–13] The resistivity and, hence, the resistance of a metal-semiconductor contact, in general, are dependent on factors such as carrier concentration, surface pre-treatment, and type of metal used. Typically, Mo is used as S/D contact to III–V devices as it has been reported in the literature to consistently produce low resistivity contact.[13] Also, Mo allows a higher thermal budget for III–V processing that improves the intrinsic MOS interface, while other metals such as Ni and Pd form alloy with the InGaAs surface, making the contact formation difficult to control.[12,14] However, contrary to the planar experimental results, Mo contacts show Schottky behavior at nanoscale dimensions,[15] posing serious threat to future scalability of these devices.

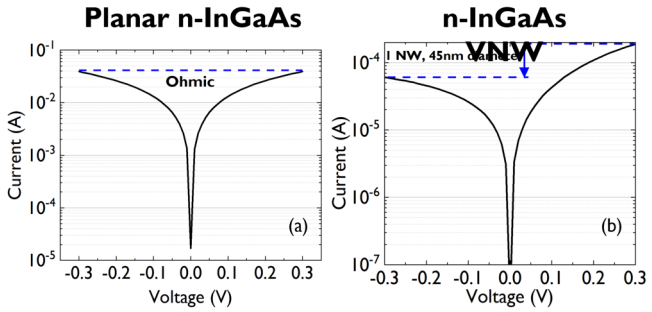

FIG. 1. *I–V* characteristics (from this work) of (a) planar CTLM structure and (b) a uniformly doped VNW. Planar structures do not capture the effects present in NW devices. Non-ohmic behavior and low current in NW resistors due to the geometry and dimensions.

Furthermore, the 3D aspects of the access resistance in vertical devices are not captured in a typical planar circular transmission line measurement (CTLM)-based test structure,[16–18] as shown in Fig. 1. The figure compares current measured from a large planar CTLM structure with that of a single, 45 nm diameter VNW. Both the planar and VNW InGaAs layers are doped n-type with a concentration of $\sim 1 \times 10^{19}$ cm^{-3}. The contact metal used is Mo in both cases. Yet, the non-ohmic behavior in the vertical device is not observed in the planar CTLM structure. Thus, a dedicated reliable test vehicle is needed to characterize these nano contacts and evaluate possible solutions to reduce the impact of contact resistance on future device performance.

In this work, we investigate p$^+$-doped VNW resistors, which are relevant for contacts to VNW-based pMOS and tunnel field effect transistor (TFET) devices. We also demonstrate a transmission line measurement or transfer length method (TLM) on p-type InGaAs VNW arrays fabricated using the top-down approach. We use a VNW resistor test structure developed with a common process flow as that of a VNW MOSFET[18] for this study. A preliminary technology computer-aided design (TCAD) setup has also been developed to understand these nanoscale contacts. The analytical model, developed later in this paper, is independent of semiconductor material and contact metal used. In principle, it can be extended to the contacts of III–V nMOS NWFETs and Si-based nanoscale devices as well.

This paper is organized as follows. In Sec. II, we present the device fabrication, the principle of vertical TLM analysis, and the effect of anneal on Mo contact resistance. The characterization results are shown in Sec. III. Section IV presents the impact of NW dimensions on contact resistivity. In Sec. V, we develop a physical model to explain the steep change in resistance with NW dimensions and verify it with TCAD simulations. Finally, we conclude in Sec. VI.

II. EXPERIMENTAL

A. Device fabrication

The key process steps involved in the fabrication of VNW resistor are presented in Fig. 2. The hard mask (HM) is defined

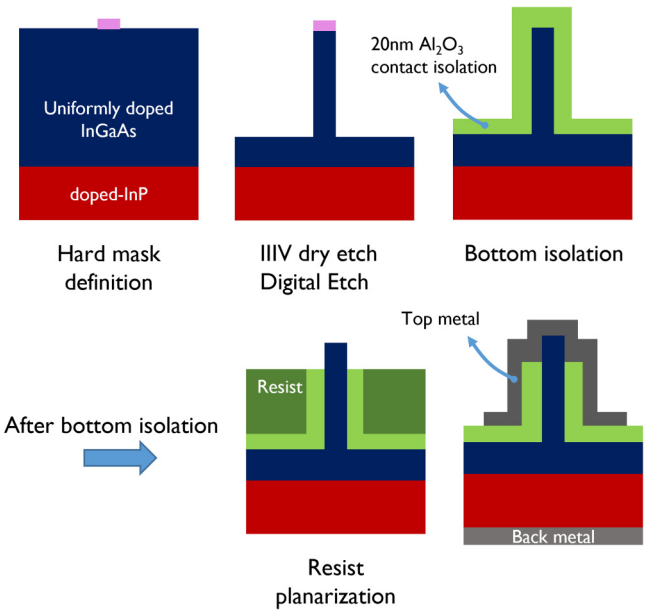

FIG. 2. Key steps involved in the process flow are described.

with e-beam lithography on an 850 nm thick uniformly doped (p-type $\sim 1 \times 10^{19}$ cm^{-3}) $In_{0.53}Ga_{0.47}As$ layer, grown on lattice matched, and doped the InP substrate (2-in.). Next, both HM opening and pillar etch steps are performed in a Lam Kiyo® conductor etch module. After the III–V dry etch, all samples are subjected to a pre-clean in diluted HCl [1 part 37% concentrated HCl and 3 parts de-ionized (DI) water] for 30 s. A thick contact isolation with 20 nm atomic layer deposition (ALD) Al_2O_3 is then performed, and the NWs are planarized with a spin resist.

The resist is then recessed to a desired height in an Oxford Plasmalab 100 etch tool using O_2 chemistry. The O_2 plasma will selectively recess the resist without affecting the Al_2O_3 isolation. The oxide is then recessed from the top of NW and the resist is stripped. Finally, metal stacks with Mo/Al and Pd/Al, with ~70 nm target thickness each, are deposited on the top of NW. The contacts are deposited immediately after a surface cleaning step in diluted HCl as described above. The back-side metallization is performed with, ~50 nm each, Mo/Al stack.

In Fig. 3, we show scanning electron microscopy (SEM) images of NWs after the III–V etch and after the top isolation recess for contact openings with two different contact length dimensions (L_C). L_C represents the length of the NW exposed (i.e., region available for the metal-semiconductor contact) from the top of the NW till the isolation region. The inspections were performed at special SEM structures that have different nanowire diameters, termed as critical dimension (CD), compared to the devices. We could clearly see the 20 nm thick Al_2O_3 isolation deposited on the sidewall and an oxide-free NW surface sticking out of it. A TEM image of the finished VNW resistor with the Mo/Al contact is shown in Fig. 4. Some of the samples were later treated with a

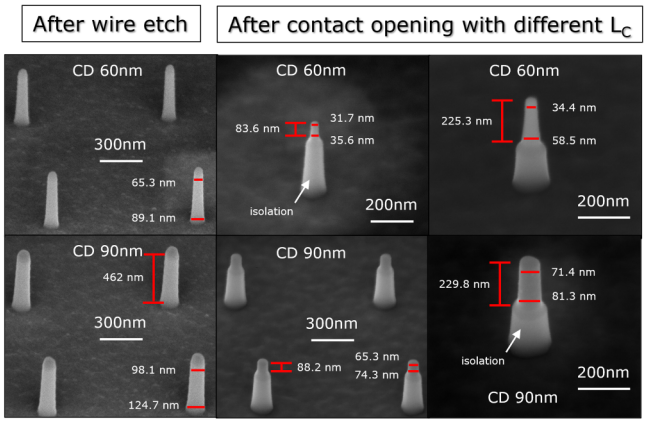

FIG. 3. SEM images (tilted to 45°) of nanowires after wire etch and after two different contact length openings. The inspections were performed at special SEM structures which have different target critical dimensions (CDs) compared to devices. The NW height and length of contact opening are corrected for the tilted angle.

forming gas anneal (FGA) at 300 °C for 5 min. The thermal budget is limited by the metal contact used, and the rationale behind it is briefly discussed later in this section.

By varying the length of NW contact (L_C) in the resistor (see Fig. 5), we can realize a TLM-like analysis. The L_C is varied while keeping the NW height constant. The NW diameter is varied from 60 to 120 nm in design and the number of NW in an array change from 1 to 100. The NW height is measured to be about 460 nm.

Diameters at the NW top and starting point of the oxide isolation are measured, from the SEM inspections shown in Fig. 3, for

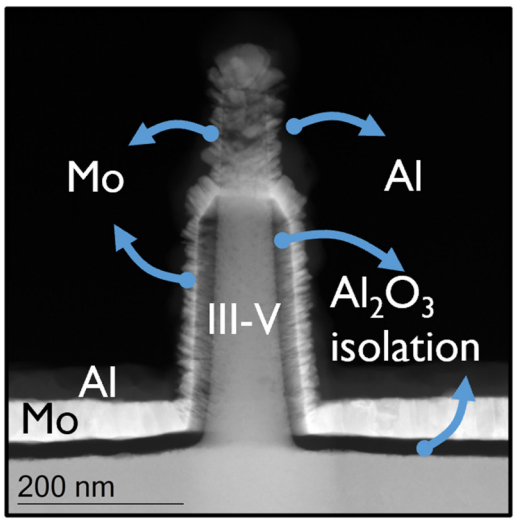

FIG. 4. Tunneling electron microscopy image of a VNW resistor with a contact diameter of 60 nm.

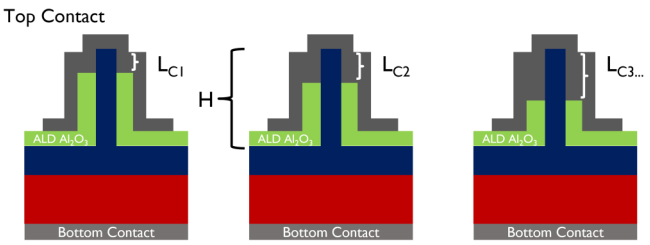

FIG. 5. Schematic of the TLM analysis using VNW; H and L_C are the NW height and contact opening length, respectively.

each L_C and an average of this is used for electrical analysis. Table I lists the estimated diameters of different target critical dimensions (CDs) at various L_C.

B. Transmission line measurement analysis procedure

The current–voltage (I–V) characteristics between the NW top and a doped, wide bottom substrate are used to extract the total NW resistance, as shown in Fig. 6(a). The bias is applied to the top of the nanowires and the ground is connected to the substrate bulk which is connected to the nanowire bottom and act as the bottom contact.

In the analysis presented in this work, the total resistance (R_{total}) is considered as a combination of the NW contact resistance and NW body resistance while the bottom substrate resistance is neglected due to the wide, doped base. The I–V from a voltage range of ±50 mV centered at 0 V applied voltage, as shown in Fig. 6(b), is used to compute R_{total} to avoid the influence of the applied voltage on the contact properties, namely, the barrier height, ϕ_B, and as a result, the contact resistivity, ρ_C. To remove the impact of probe resistance on the measurement, the voltage of the NW top is monitored separately by another probe with high impedance (~zero current pass through it). The monitored voltage and measured current are used to calculate R_{total}.

Resistor analysis using a standard TLM on lateral nanowires (using the substrate transfer technique)[19] and vertical nanowires (using the vapor-liquid-solid (VLS) growth)[20] has been demonstrated in the literature. The contact resistance of a metal-semiconductor (nanowire) contact can be modeled as a distributed resistive network, as shown in Fig. 7.[19]

The current transport within the network can be described using a transmission line model. The resistivity of the semiconductor is given by ρ_S, and L_C is the contact length across which the voltage drop and current through the NW semiconductor are assumed to vary with distance, x. The current is assumed to grow from zero at $x = 0$ to total current at $x = L_C$. The resistance, dR_X, along the length of the smallest segment of NW, dx, across which the voltage drop and current are assumed to be a constant is then given by

$$dR_x = \frac{\rho_S \times dx}{\pi r_{NW}^2}, \quad (1)$$

where r_{NW} is the physical radius of the nanowire.

TABLE I. Estimate of diameters at different contact opening lengths for different target CDs.

L_C (nm)	CD 60 nm (nm)	CD 80 nm (nm)	CD 100 nm (nm)	CD 120 nm (nm)
84	34	60	80	100
117	32	64	84	104
225	47	66	86	106
253	49	71	91	111
317	50	76	96	116

The voltage across this smallest element dx, along the NW length, is given by

$$dV = \frac{-\rho_S \times I(x) \times dx}{\pi r_{NW}^2}. \quad (2)$$

The voltage drop at the interface between metal and the NW surface (under the contact) is assumed to be a constant and v_o and ρ_C are the specific contact resistances at the metal-semiconductor interface. The differential resistance, dR_I, at this interface across the NW cross section of radius r_{NW} and length dx is then given by

$$dR_I = \frac{\rho_C}{2\pi r_{NW} c \times dx}. \quad (3)$$

The current through this interface across the NW cross section of radius r_{NW} and length dx can be written as

$$dI = \frac{2\pi r_{NW} \times [v_o - V(x)] \times dx}{\rho_C}. \quad (4)$$

Combining the above equations and using the total resistance, R_{total}, measured across the NW, i.e., the sum of contact resistance (R_C) and NW body resistance (R_{NW}) under the isolation, we get the following analytical equations:[19,20]

$$R_{total} = R_{NW} + R_C, \quad (5)$$

$$R_C = \frac{4\rho_s L_T}{\pi d^2} \times \coth\left(\frac{L_C}{L_T}\right), \quad (6)$$

$$R_{NW}(h) = \frac{4\rho_s \times (H - L_C)}{\pi d^2}, \quad (7)$$

$$\rho_C = \frac{4L_T^2 \rho_s}{d}. \quad (8)$$

The terms d, ρ_S, and L_T are the NW diameter, bulk resistivity, and transfer length at the contact, respectively. The transfer length (L_T) is defined as a characteristic length over which most of the current flows in the semiconductor under the metal contact before flowing into the contact.

The above equations are numerically solved with L_T and ρ_S as fit parameters. The NW dimensions measured from SEM, tabulated in Table I, are used for the analysis. The specific contact resistivity, ρ_C, is then calculated from the fit values.

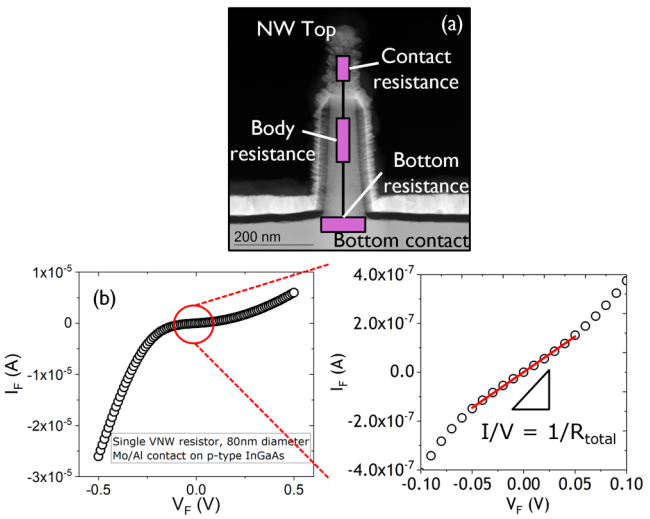

FIG. 6. (a) Schematic of different resistor components of a nanowire and (b) *I–V* of a typical p-doped VNW resistor (single NW and 80 nm diameter), with Mo/Al contact, is shown. Also shown, the range at which the resistance is extracted.

C. Effect of anneal on Mo contact resistance

Figure 8(a) shows the total resistance measured for each design CD at different annealing conditions for Mo contact on p-type InGaAs vertical resistors. The R_{total} reduces after an anneal at 300 °C but slowly increases when the annealing temperature and time are increased, as indicated by the arrows in the figure. This trend of R_{total} vs thermal treatment is also presented in Fig. 8(b) for a design CD of 80 nm. This trend was also observed in the planar CTLM experiments of this work (not shown here). We observed no change in the sheet resistance of the underlying InGaAs layer, indicating that this is, purely, a contact related effect.

This increase in resistance at a higher thermal budget has also been confirmed in the literature for Mo contacts on planar n-InGaAs.[21] Literature studies on the thermal stability of Mo on InGaAs layers, however, quote no "inter-diffusion" or "chemical interaction" at the metal-semiconductor interface.[22] The study also reports that the Mo metal does not degrade as the sheet resistance

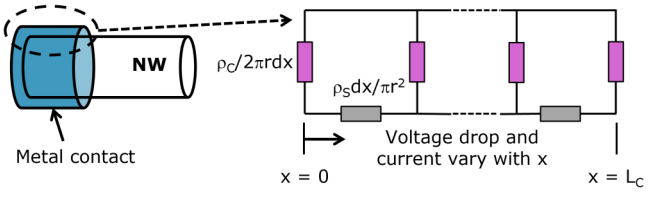

FIG. 7. Schematic of a metal-semiconductor contact to NW expressed as a distributed resistive network.

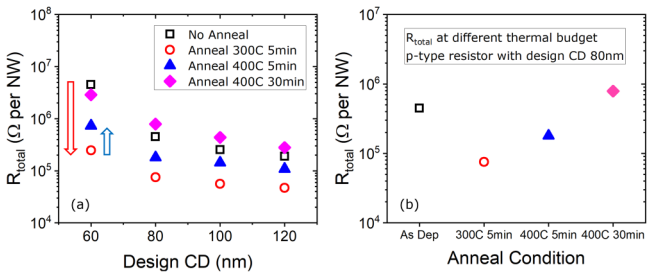

FIG. 8. Effect of annealing temperature on Mo contact to p-InGaAs: (a) measured R_{total} as a function of design diameter and (b) R_{total} for a given diameter as a function of anneal condition.

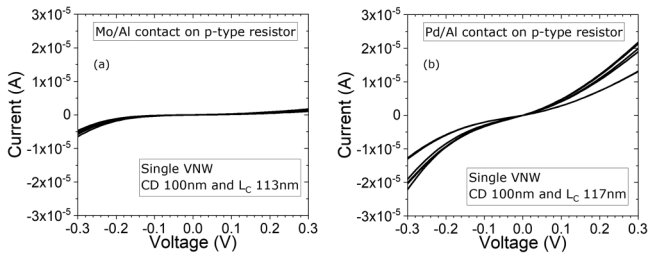

FIG. 9. *I–V* plots of single VNW p-type resistors for (a) Mo contact and (b) Pd contact. The NW design CD is 100 nm (actual diameter ~80 nm) and the contact length, L_C is ~117 nm.

of the metal remains constant over the entire annealing temperature range up to 300 °C.

One hypothesis for this turn-around in total resistance with temperature could be a metal "scavenging effect." It has been reported in the literature[23] that oxidation and reduction of the interface between high-k dielectrics and InGaAs layers are thermodynamically driven by the choice of metal electrodes. The kinetics of the reactions depend on the difference in Gibbs free energy (ΔG) values between metal oxides and III–V oxides. If ΔG is negative, then the InGaAs surface is observed to be oxidized during thermal anneal in a forming gas ambient.[23] However, the interface is clear of native oxides when ΔG is positive.

Mo oxides and III–V native oxides are nearly thermodynamically equivalent, i.e., the difference in their Gibbs free energy is close to zero (but negative).[23] So, it is possible that in our NW resistors, at higher temperatures, oxidation of the III–V surface happens to lead to an increase in resistance. Some literature studies[24] on the thermal stability of III–V native oxides report that the III–V oxides are stable at higher temperatures between 350 and 400 °C compared to a lower thermal budget, thus supporting our hypothesis.

III. ELECTRICAL CHARACTERIZATION RESULTS

A. *I-V* Characteristics and device variability

The *I–V* overlay plots of single VNW p-type resistors (without any thermal treatment) for both Mo and Pd contacts are shown in Fig. 9. The NW design CD is 100 nm, corresponding to an actual diameter of ~80 nm and the contact length, *LC*, is ~117 nm. We could note that Pd contact to InGaAs has higher current compared to Mo. Furthermore, resistors with Mo contact show a strong non-ohmic behavior compared to the ones with Pd contact. We can see from the tables above that the average wire diameter changes for a given design CD with respect to the contact length. So, we will mention the design CD in all the figures for convenience and mention the actual diameter only when needed.

The difference between Mo and Pd contacts is also widely reported in the literature for both n-type and p-type InGaAs layers.[12,25] This is attributed to the presence of a very thin (<1 nm) interfacial III–V oxide layer between Mo and the semiconductor,[12] despite a surface pre-clean before metal deposition. Pd, on the other hand, is known to readily react with InGaAs to form an alloy, even at low temperatures (<300 °C), thus penetrating the native oxide.[26,27] However, it must be noted that the above *I–V* plots were measured for devices that did not receive any high thermal treatment (i.e., ~300 °C). It is possible that the Pd might have reacted with InGaAs during the contact pad patterning step when the sample without and with the resist coating was subjected to a 2 min bake at 190 and 120 °C, respectively. Such instances where Pd diffuses into the III–V layer when the sample experiences a mild increase in the temperature of the environment (~140 °C) have been reported in the literature,[28] thus supporting our hypothesis. This is further elucidated by the contact characteristics of the VNW resistors after annealing, as shown in Fig. 10.

The figure shows the median *I–V* of various VNW resistors before (reference) and after FGA at 300 °C for 5 min. We could see that the resistor with Pd contact [Fig. 10(b)] shows little change after annealing, indicating that intimate contact has already been formed during contact patterning. In the case of Mo [Fig. 10(a)], however, there is an improvement in the current and reduction in non-ohmic behavior after the anneal. The reason for this improvement is already discussed in Sec. II C. Still, the current level is lower than the Pd contact, indicating a high resistivity for Mo contact and, hence, a larger barrier height. In order to realize a clean (oxide-free) contact surface and achieve ultra-low contact resistance with Mo, we need a more stringent III–V surface preparation[24,25,29] or *in situ* fabrication techniques combining III–V growth and metal deposition.[15,21]

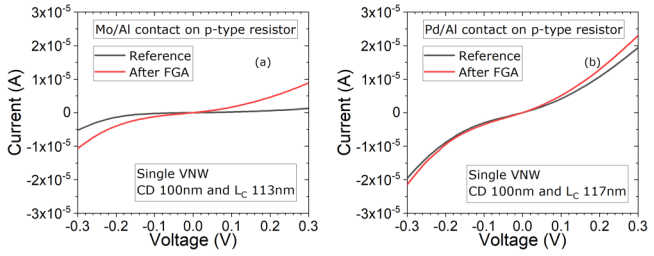

FIG. 10. Effect of anneal on (a) Mo and (b) Pd contacts.

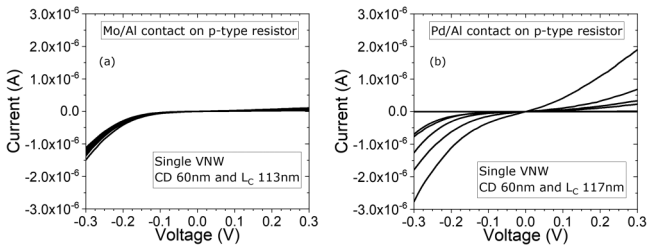

FIG. 11. *I–V* plots of single VNW p-type resistors (without thermal treatment) for (a) Mo contact and (b) Pd contact.

As the NW dimension reduces, the current through the resistor also drops. The *I–V* for resistors with a smaller design CD of 60 nm (actual diameter ~ 30 nm) is shown in Fig. 11. We could note that the current levels have dropped by almost one order of magnitude for both Mo and Pd contacts (owing to the NW dimensions). In addition to this, we see a large spread in the resistor characteristics of the Pd contacts.

The spread could be due to the rough interface between Pd and InGaAs, formed because of their reaction. Figure 12 shows the energy dispersive x-ray spectroscopy (EDS) of the VNW resistor with the Pd/Al contact. The NW design CD is 60 nm (actual diameter ~ 30 nm), and the contact length *LC* is ~117 nm. We could note that the Pd layer is rough and not conformal around the NW contact region, probably due to the reaction with III–V underneath. Mo contacts do not have this issue (not shown here).

From the EDS, we can see that the Pd has completely consumed/reacted with the InGaAs under the contact and the metal has also diffused into the NW body (below the oxide isolation level). The length of Pd diffusing into InGaAs is longer for smaller diameters compared to NW with larger diameters (not shown here). Furthermore, Pd has also reacted with the Al metal capping, which can cause problems with RC delays of real devices due to the change in resistivity of contact vias from the intermixing.

Ni has been suggested as another candidate for metal contact to the S/D junction of III–V MOS devices. However, similar to Pd,

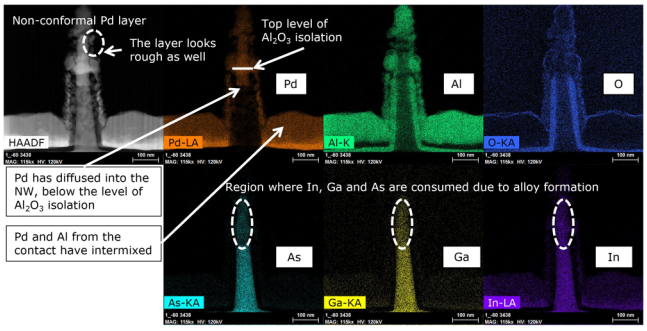

FIG. 12. Energy dispersive x-ray spectroscopy (EDS) of VNW resistor with Pd/Al contact.

Ni is also reported to diffuse and form an alloy with III–V layers.[30–33] Ni forms an ohmic contact and, hence, helps to achieve tremendous improvement in ON-state performance of InGaAs nanowire devices compared to Mo contacts.[14] However, like the Pd case discussed above, the length of diffusion of Ni varies with device dimensions. This has been attributed to a higher diffusion rate (which is surface limited) for narrow dimensions due to the higher surface-to-volume ratio.[34] It was also reported in Ref. 14 that for smaller NW diameters, the Ni contact possibly diffused through the doped S/D junction and reached the intrinsic InGaAs channel region. This resulted in a Schottky contact, asymmetric device behavior, and short channel effects, thus degrading the performance at smaller dimensions.

There are also studies in the literature that use "solid phase regrowth" to dope III–V layers.[35,36] It is a technique in which a metal that readily forms an alloy with III–V, like Pd, is used in combination with Si/S (dopants to III–V) and annealed at different temperatures in two or more stages to incorporate the dopants during the alloy formation. However, this usually results in a very rough interface and can also result in un-wanted alloy spikes that will vary the contact or channel length (as discussed for Ni above).

It is obvious from the studies reported in the literature and from this work that such poor control of (a) alloy formation and (b) diffusion into the semiconductor material will result in a rough contact, high device-to-device variability, and overall degraded device performance. As device dimension is reduced, we need better control over the alloy formation and a smooth interface for a uniform and optimized contact integration with future scalability.

B. The total resistance vs contact length

The total resistance (R_{total}) is calculated in a voltage range of ±50 mV centered at 0 V applied voltage, as already shown in Fig. 6(b), to avoid the influence of the applied voltage on the contact properties. The resistance is normalized to the total number of nanowires (NW #) in an array. The normalized R_{total} of p-type resistors is plotted as a function of NW design CD and NW no. in Fig. 13 for both Mo and Pd contacts. The actual diameters for each design CD at different L_C can be checked from Table I listed above.

The resistance, normalized to the NW no. is consistent across all NW numbers in an array for any given diameter for both contacts. This could mean that we have a stable fabrication process that does not induce any variations in the resistor and so a reliable test vehicle to study the NW contacts is realized. For the Pd contact, at smaller diameters, we could notice a high spread in data, the reason for which is already discussed.

The median, of normalized total resistance, measured for each design CD with Mo and Pd contacts is shown as a function of the contact length in Fig. 14. We could note that there is a one to two orders of magnitude difference in R_{total} between CD 60 nm and the rest of the dimensions at lower *LC*. However, this difference starts to reduce as the contact length increases and the R_{total} begins to converge for all CDs (indicated in the figure).

The decrease in R_{total} at higher L_C is due to the increase in the available contact area as L_C increases. Yet, this reduction is not

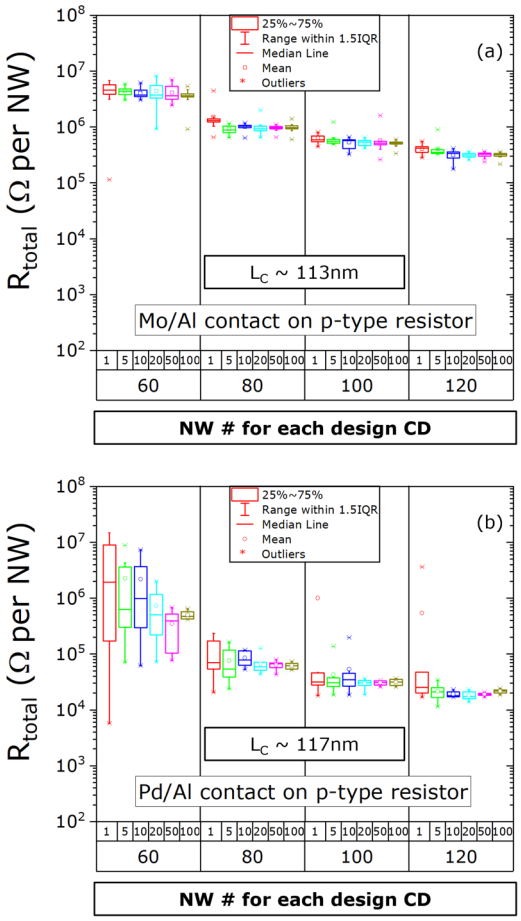

FIG. 13. Normalized resistance (ohm per NW) of p-type resistors as a function of NW # for each design CD is shown for (a) Mo contact and (b) Pd contact.

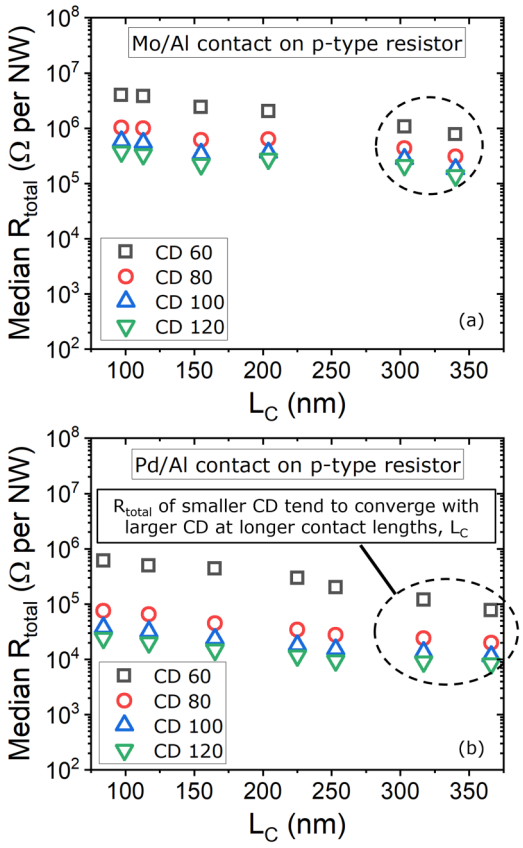

FIG. 14. R_{total} as a function of L_C for NW resistors with (a) Mo and (b) Pd contacts for different design CDs.

abrupt and sufficient to account for an improvement in a real device scenario. Another point to note is that the transition of R_{total} from CD 80 nm to CD 60 nm is steeper compared to the transition observed in rest of the devices.

Equations (5)–(8) described earlier were solved with L_T and ρ_S as fit parameters for the R_{total} data measured. We get a good fit of the model with the experimental data (Mo contact), as shown in Fig. 15. The contact resistivity, for the Pd contact, extracted from the fit is shown in Fig. 16(a). ρ_C is uniform across two decades of NW # in an array for a given diameter. This could, again, imply that both the fabrication process and the extraction procedure induce negligible variations.

The extracted ρ_C as a function of NW design CD (diameter) is shown in Fig. 16(b) for both Mo and Pd contacts to p-type InGaAs NW after an FGA at 300 °C for 5 min. We observe a strong diameter dependence of ρ_C for both metals, while we expect it to remain unchanged for a given doping concentration and metal-semiconductor system (barrier height).

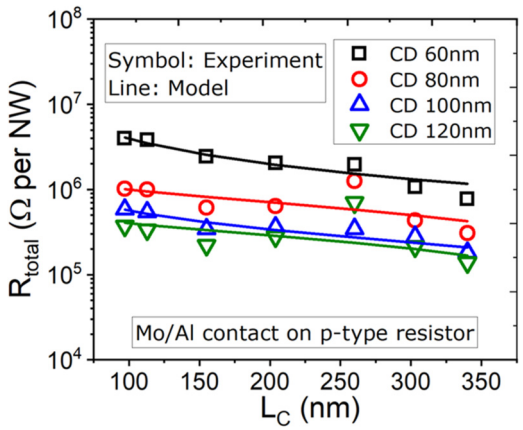

FIG. 15. Experimental R_{total} data and the fit of the model. Data from p-type resistor with Mo contact are shown.

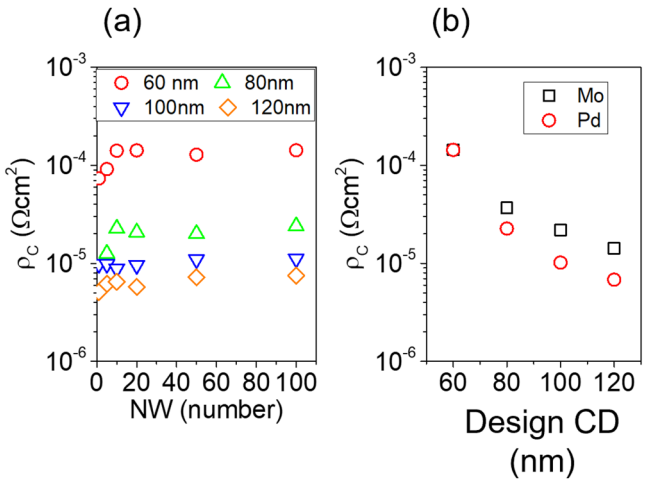

FIG. 16. (a) Specific contact resistance of p-type InGaAs with Pd contact, as a function of NW numbers; uniform values for a given diameter. (b) Strong change in resistivity (ρ_C) with NW diameter for both Mo and Pd contacts; the data are after FGA.

In order to understand the effect of NW geometry and dimensions on the contact resistivity (and hence, resistance), a thorough analysis is presented in Secs. IV and V.

IV. CHANGE IN CONTACT RESISTIVITY WITH DIAMETER

It must be noted that, even though analytical equations (5)–(8) contain a relation between ρ_C and diameter, we expect any difference in the contact area (due to change in diameter) to be taken into account in the fit of L_T while keeping ρ_C unchanged (as to be expected). In order to understand this geometrical effect [observed in Fig. 16(b)], TCAD simulations were performed. The simulations were carried out with Sentaurus^{TM} Device software[37] using a simplified structure as shown in Fig. 17.

The top wire diameter (Dtop) is varied to account for different design CDs and the diameter at the bottom (Dbot) of the wire is kept equal to Dtop, making the slope as 1, in the simulations. Variations in slope are included in the latter part of the simulation experiments, which will be discussed soon. The contact length is taken as $L_C = 120$ nm. The InGaAs layer is assumed to be uniformly doped (p-type) to a concentration of 1×10^{19} cm^{-3}. The Schottky barrier height at the top contact is assumed to be 460 meV for Pd and 520 meV for Mo. It must be noted that the Pd diffusion is assumed to have a negligible contribution to the contact resistance in the simulations, i.e., not the dominant factor affecting the barrier height.

Figure 18 shows the simulated IV curves matching the measurement (after FGA) for single NW resistors with design CD 100 nm (actual diameter ~ 80nm) for (a) Mo contact and (b) Pd contact. The total resistance is then extracted from the TCAD simulations using the procedure explained in Fig. 6(b).

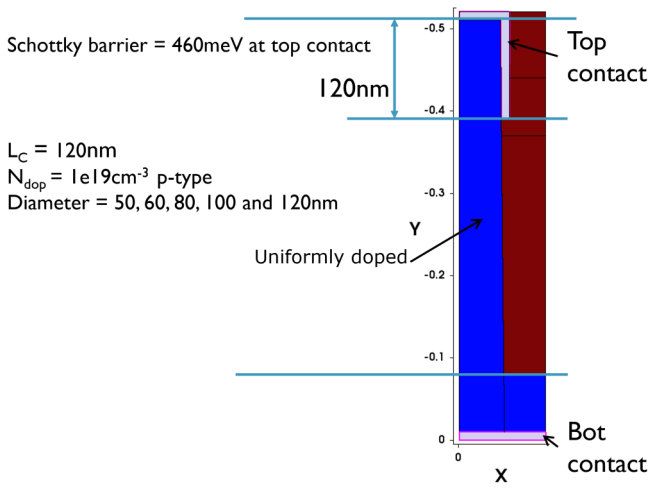

FIG. 17. Schematic of the TCAD generated structure used in the simulations.

A. Hypothesis I: Varying doping concentration

The R_{total} from the TCAD results could not match the data for other dimensions with a fixed set of parameters like constant doping or contact barrier height, ϕ_B, as shown in Fig. 19(a). With variations of <10% in doping, across different CDs, the results show better agreement [see Fig. 19(b)]. The R_{total} for the Pd contact is shown. It must be noted that the design CD is assumed as the NW diameter in this figure, yet, correcting for the actual diameter in this particular case does not change the outcome of the analysis.

This variation in doping with NW dimension could account for the increase in contact resistivity, ρ_C, with decreasing NW diameter. However, the change in doping concentration with diameter is highly unlikely. The NWs in this work are etched top down (at the same time) from a uniformly doped InGaAs layer and, hence, we expect the same doping concentration across all dimensions. So, the above hypothesis is ruled out.

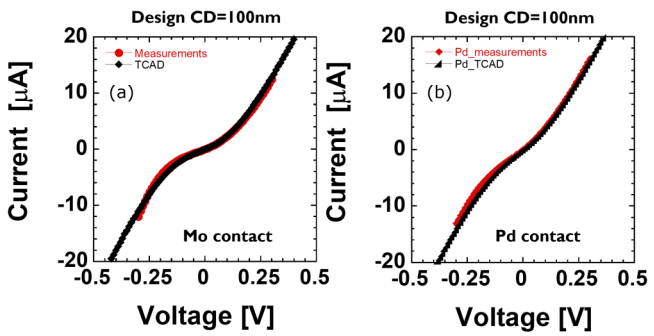

FIG. 18. The simulated curve mimics the measured curve of a single NW resistor with design CD 100 nm (actual diameter ~80 nm) for (a) Mo contact and (b) Pd contact. The data are after anneal (FGA, 300 °C for 5 min).

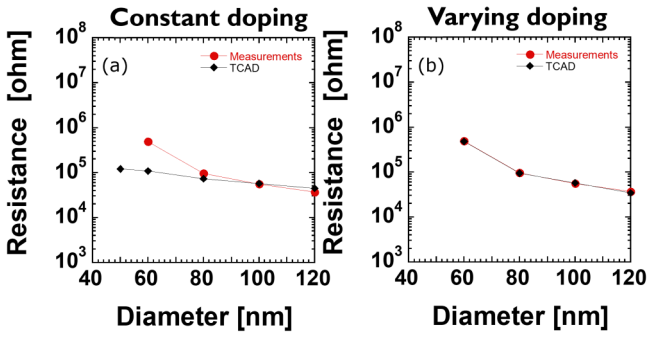

FIG. 19. Comparison of R_{total} from measurements and simulations with (a) constant doping and (b) varying doping levels. The observed trend was not possible to fit in TCAD with one set of parameters. R_{total} for the Pd contact is shown.

B. Hypothesis II: Increase in dopant ionization energy due to dielectric confinement

It has been reported, in bulk semiconductors, that the Coulomb potential of dopant atoms can give rise to bound states within the semiconductor bandgap.[38] A strong screening of this potential by the semiconductor, in turn, results in dopant ionization energies of only a few hundredths of an electron volt, thus keeping the impurities ionized at room temperature.[39,40] However, studies report dopant deactivation (not by quantum confinement) in semiconductor nanowires due to a radius-dependent enhancement of dopant ionization energy caused by dielectric confinement.[39,40] It generally occurs when there is a dielectric mismatch between a nanoscale semiconductor, such as a nanowire, NW (with relative dielectric constant ε_S), and its environment (ε_E).[41] It is like an image force which, when $\varepsilon_E < \varepsilon_S$, significantly affects the screening of the Coulomb potential, thereby affecting the doping efficiency at room temperature. As a result, the dopant ionization energy is reported to increase with decreasing NW radius, hence increasing dopant deactivation, irrespective of the doping species used.[39] This results in increasing NW resistivity with decreasing radius,[40] an effect also reported in this work.

In this work, our resistors have two parts: (a) the NW region wrapped with the thick Al_2O_3 oxide and (b) the NW region wrapped with the contact metal. It has been experimentally confirmed in Si nanowires that when coated with a high-k dielectric, the dielectric mismatch is reduced and the increase in the NW resistivity with decreasing radii is suppressed.[40] Hence, we can ignore the possibility of dopant deactivation in the NW region under the isolation oxide. In the case of NW under the metal contact, we can ignore the contribution of any interface layer to the dielectric mismatch effect, as the layer is expected to be very thin. Furthermore, it has been reported that the dielectric mismatch effect is absent in the case of NW wrapped with metal, and as a result, the active dopant concentration could be relatively higher for an NW wrapped with metal compared to the region of NW covered with, say a low-k dielectric.[42] So, this hypothesis can also be ruled out.

C. Hypothesis III: Uniform loss of dopants at the NW surface

Following a similar line of thought as above, another hypothesis, to account for the variation in resistance with diameter, is a uniform loss of dopants at the NW surface. The schematic of the TCAD structure used is shown in Fig. 20. The NW surface is assumed to have a varying dopant concentration moving from center to edge of the wire as indicated in the figure. The rate of decay in doping concentration from center to edge is kept the same for all dimensions.

A comparison of measured resistance with simulations assuming surface dopant loss is shown in Fig. 21. The dimensions reported in the figure are corrected for the actual diameter. The simulations show good agreement with the R_{total} measured. However, it is important to address the possibility of surface dopant loss in our wires before moving ahead with further conclusions.

There are some studies in the literature that report the segregation of dopant atoms at the edge/surface of III–V nanowires that are grown using bottom-up techniques.[43–45] When the segregation happens, dopant atoms are concentrated at the NW edge (within a few nm), and any surface treatment of the wire that etches the first few nm layers will result in large surface dopant loss.

The first principle study[46] to understand the kinetics of dopant segregation in III–V nanowires reports that the degree of segregation depends on the electronegativity of dopants, the crystal structure of the nanowire, and the presence of surface states or dangling bonds at the NW edge. The study also reports that segregation is thermally activated, i.e., it occurs at high temperatures. Hence, it is a common occurrence in grown wires, as the growth temperatures are sufficiently high. However, this does not apply to wires that are etched and processed at a low thermal budget, such as the ones reported in this work.

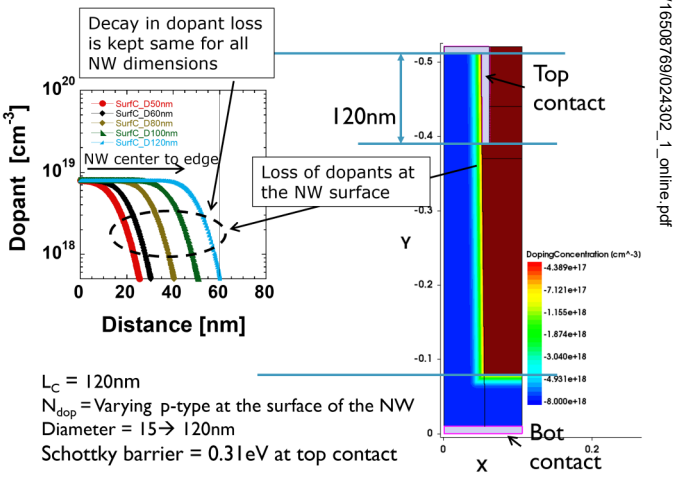

FIG. 20. Schematic of the TCAD generated structure used in the simulations for surface dopant loss.

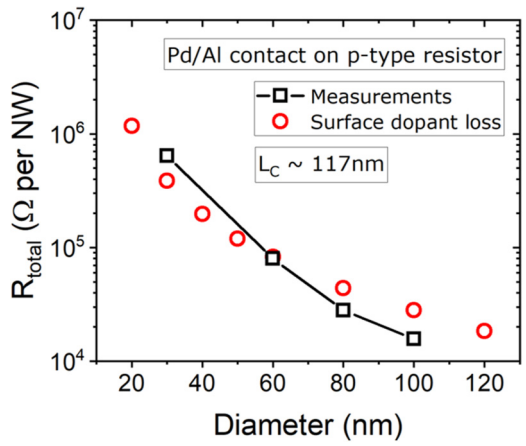

FIG. 21. Comparison of measured resistance with simulations assuming surface dopant loss.

More recently, a reduction in current transport of InGaAs fins, with fin width scaling, that could not be accounted for by the regular change in conduction area (similar to the phenomenon observed in this work) has been reported in the literature.[47] The fins in this study are fabricated by top-down etch technique similar to our nanowires. The study reports a "dead-zone" (about 10 nm wide) being present along the fin surface which reduces the total area available for conduction and, hence, a steep change in current transport with scaling. The occurrence of such a non-conductive region has been associated with a combination of fermi-level pinning, semiconductor surface damage from fin etching, and mobility degradation.[48] However, it has been experimentally demonstrated that loss of dopants on the fin sidewall is not a possible reason for the "dead-zone," given the low thermal budget for processing these fins.[47]

In our study, the thermal budget seen by the wires is $\lesssim 300\,^{\circ}\mathrm{C}$. Thus, based on the literature reports above, which suggest no important loss of dopants, we can fairly assume that surface dopant loss is not occurring in our wires, ruling out this hypothesis.

V. ACCOUNTING FOR THE DEPLETION WIDTH IN THE NANOWIRE

Let us fall back to the analytical TLM equations (5)–(8) for the moment. The equations assume that the metal-semiconductor contact is ohmic. However, this is not what we observe from our experiments, and the depletion region under the contact cannot be ignored. Assuming $W_{dep@contact}$ as the depletion region thickness present in the NW semiconductor surface under the metal contact, we can re-write the term, for the resistance along the NW length, given by Eq. (1) as

$$dR_x = \frac{\rho_S \times dx}{\pi r_q^2}, \tag{9}$$

where $r_q = r_{NW} - W_{dep@contact}$.

On the other hand, the interface resistance between metal and semiconductors given by Eq. (3) will not change because the current has to tunnel from the metal interface through the depletion region to reach the NW center. So, unless there is a physical change in the NW dimensions, this term will not be affected. In addition to the depletion under the contact, there will also be a depletion region, $W_{dep@isolation}$, on the surface of the NW body under the oxide isolation. This could be attributed to the surface states present at the interface of the NW and the oxide.[49] It must be noted that the presence of the interface state density has been extensively studied for InGaAs/oxide interfaces on planar capacitors in the literature.[50]

Equations (5)–(8) do not account for the depletion region formed in the NW semiconductor under the metal contact[51] and the depletion region or "dead-zone,"[47,49] which could form in the NW body under the oxide isolation (see Fig. 22).

Thus, we adapt the TLM equations, to account for the non-conductive regions, as described in Eqs. (10)–(12),

$$R_C = \frac{4\rho_s L_T}{\pi d_q^2} \times \coth\left(\frac{L_C}{L_T}\right), \tag{10}$$

where $d_q = d_{NW} - Wdep_{@contact}$,

$$R_{NW}(h) = \frac{4\rho_s \times (H - L_C)}{\pi d_e^2}, \tag{11}$$

where $d_e = d_{NW} - Wdep_{@isolation}$,

$$\rho_C = \frac{4L_T^2 d_{NW}\rho_s}{d_q^2}. \tag{12}$$

d_{NW} is physical NW diameter, d_q is the effective diameter under contact, d_e is the neutral conduction diameter under isolation, $W_{dep@contact}$ is the depletion region under contact, and $W_{dep@isolation}$ is the depletion under isolation.

The width of the depletion region is calculated by solving Poisson's equation for cylindrical geometry at different NW diameters.[49,52–54] It must be noted that while the current TCAD deck included depletion under the contact (by assuming a Schottky contact), it did not account for the depletion under the isolation due to D_{it}.

Taking these learnings, we added a few improvements to the existing TCAD deck (see Fig. 23). NW tapering caused by III–V dry etch, depletion under contact (already included) and D_{it} at

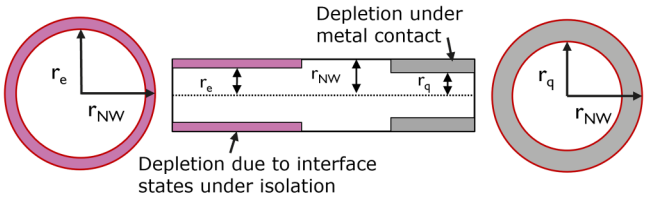

FIG. 22. Depletion region forms in the NW under the metal contact and under the isolation, thus reducing the total available conduction area.

NW-isolation interface are considered. The diameter at the bottom of the wire (Dbot) is calculated with a slope of Dbot = Dtop + 30 nm in the simulations to account for the tapering in the NW. D_{it} at the interface between NW and isolation is included using the profile as shown in Fig. 23.

We are able to make the following observations from this exercise. Figure 24 compares the total resistance obtained from the simulations and measurements. Let us assume that the surface of nanowire body, in contact with isolation, has interface states (D_{it}). Then, to satisfy charge neutrality, there will be an equal and opposite charge present in the body of the nanowire. So, for a positive surface charge (let us suppose), there should be a negative space charge, resulting in depletion of the region under the isolation. By accounting for this body depletion (i.e., D_{it}) we could note that the simulations (with fixed set of parameters) start to concur with the measurements, unlike before, thus, validating our assumption. The data for p-type resistor with Pd contact (after FGA at 300 °C for 5 min) are shown in the figure.

The figure also compares the specific contact resistance (ρ_C) extracted from the TCAD simulations and the TLM analytical equations with and without modifications mentioned earlier. We could note that the TCAD extracted ρ_C is independent of diameter, as expected. In addition to this, ρ_C extracted using the modified TLM equations, which included the depletion under NW contact and body, shows better agreement with TCAD. The analytical fit parameters, from the modified equations, include

- NW semiconductor resistivity, $\rho_S = 0.01–0.012\ \Omega$ cm, which corresponds to a p-type doping of $6–8 \times 10^{18}$ cm^{-3} in $In_{0.53}Ga_{0.47}As$.[55] This agrees with our expected doping concentration of $\sim 1 \times 10^{19}$ cm^{-3}.
- The transfer length, L_T, obtained from the fit varies about 280–340 nm which is high but not surprising for such high resistive contacts.[19]
- The depletion under the contact is calculated to be 5 nm which agrees with TCAD simulations (not shown). The depletion under isolation is assumed to be 20 nm which corresponds to a fixed surface charge density of $\sim 4 \times 10^{12}$ cm^{-2} for given body doping concentration.[49]

The key message from the above exercise is that we are able to identify a reasonable physical model that could account for the steep change in resistance with NW dimensions. The surface states present under the isolation, which usually correspond to the un-gated, access resistance region in real devices, play a crucial role in affecting the overall performance of the NW devices. If this effect is unaccounted for, then it results in an apparent increase in contact resistivity with decreasing NW dimensions. A similar observation of a varying Schottky barrier height with NW diameter in n-type InGaAs NWFETs was observed before.[18] This could potentially lead to misinterpretation of data and the real problem goes unaddressed.

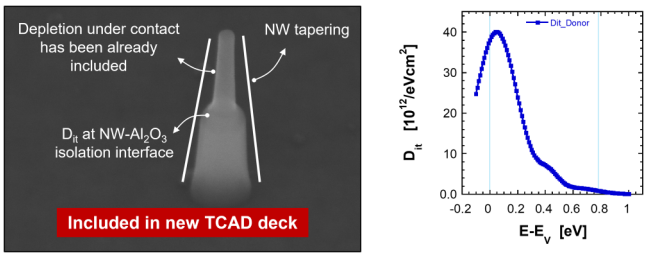

FIG. 23. Effect of NW tapering, depletion under contact, D_{it} at the NW-isolation interface is considered.

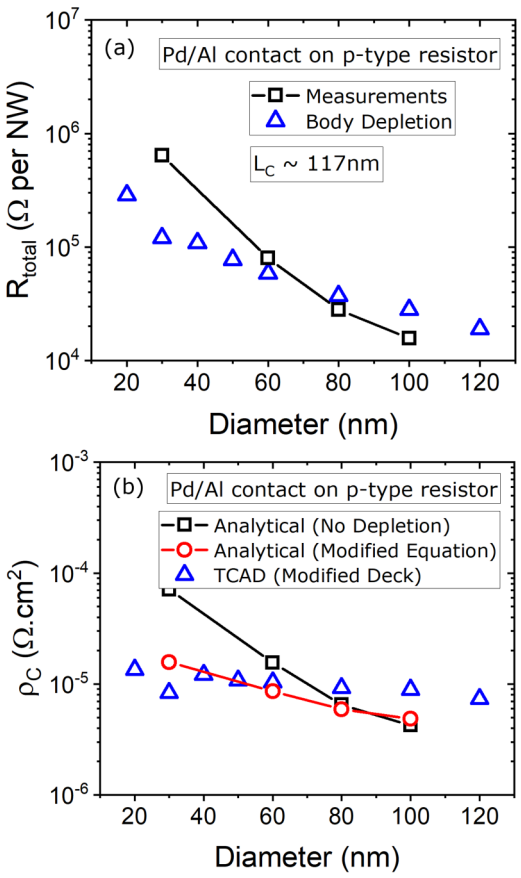

FIG. 24. (a) TCAD (with new deck) results compared to measurements (R_{total}). (b) The specific contact resistance extracted from analytical TLM equations and TCAD simulations. Modified TLM equations agree better with TCAD. The data for p-type resistor with Pd contact (after FGA at 300 °C for 5 min) is shown.

There are studies in the literature, which investigate the influence of NW geometry on depletion width, contact barrier height, ϕ_B, and contact resistivity, ρ_C.[51–54,56] To the best of our knowledge, we understand that these studies lack experimental work, use ultra-scaled dimensions in the model, that is not feasible to achieve at the moment, and provide only qualitative reasoning for the increase in resistance or resistivity at nanoscale dimensions. In this work, we have experimentally validated the influence of NW geometry and provided more tangible reasoning for this effect.

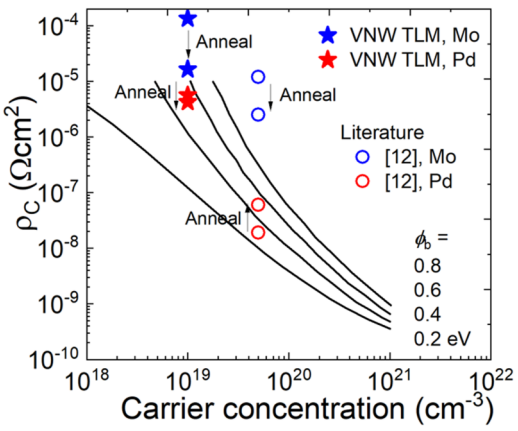

FIG. 25. Benchmark plot with planar contacts. The effect of anneal is depicted by the arrows.

Now that we have established an understanding of the relation between the NW dimension and resistance, let us benchmark the contact resistivity extracted using the above procedure. To be fair, the ρ_C values obtained from VNW resistors with large CD (120 nm, actual diameter ~ 100 nm) are compared with planar data of similar doping and contact metal from the literature.[12] The data from p-type InGaAs resistors are shown in Fig. 25.

We could notice that the ρ_C values, the trend with respect to the metal used and the thermal budget, obtained from our VNW resistors match the literature reports. The theoretical model[13] (solid lines) predicts ρ_C for different barrier heights and carrier concentrations. By comparing the experimental data with the model, we get an estimate of the Schottky barrier at the NW contact. These estimates are in close agreement with the TCAD simulations used for the p-type resistors in this work.

VI. CONCLUSIONS

Schottky barrier height and its origin is a topic of intense debate and long research. We have seen in this work how the properties of a contact change at nanoscale dimensions due to the nanowire geometry. A reliable test vehicle has been developed and successfully demonstrated to capture the 3D effects of the metal-NW semiconductor contact. The vehicle can be used to study contacts to both p- and n-type semiconductors.

In this study, we tested two types of metal contacts, namely, reactive alloy formation and non-reactive, to III–V semiconductors. We observed that the reactive metal resulted in a lower contact resistivity. However, the InGaAs layer, under the contact, was found to be completely consumed/reacted with the metal. The metal also diffused longer into the nanowire body for smaller dimensions. This will lead to an overall degradation, i.e., an increase in device variability and RC delays. From this work, we identified Mo metal contact to be compatible with the thermal budget for III–V processing. Appropriate interface treatment before a metal deposition can help to achieve the target resistivity in these nanoscale contacts.

Surface states (in the non-contacted/un-gated region of real devices) can no longer be ignored in the efforts to improve the contact properties. One of the crucial observations of this study was that the presence of interface states in the un-gated region of the nanowire devices hinders the current conduction through the wires. The interface states form a depletion region in the body of the nanowire, thereby limiting the area of the neutral region available for the current transport. This effect was found to get worse at smaller dimensions. We also supported the study with TCAD simulations and improved the existing analytical model by adding to it the geometrical effects on the current transport.

This study has shed light on the relevant questions that are needed to be answered for solving the current contact issues with nanowire devices. It has opened up a new door to study nanowire contacts which compels us to understand this new stream of dominant effects and their origins. It is pertinent to solve these issues and have stable nanoscale contacts before extending the study to more appropriate interface models. We believe this work will pave the path for future exploration of nanoscale contacts.

ACKNOWLEDGMENTS

The authors would like to acknowledge support through the imec's industrial affiliation program on Beyond Silicon CMOS.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

S. Ramesh: Conceptualization (lead); Data curation (lead); Formal analysis (lead); Investigation (lead); Methodology (lead); Visualization (lead); Writing – original draft (lead); Writing – review and editing (lead). **Ts. Ivanov:** Conceptualization (equal); Data curation (equal); Formal analysis (supporting); Investigation (equal); Methodology (equal); Supervision (equal); Validation (equal); Visualization (supporting); Writing – original draft (supporting). **A. Sibaja-Hernandez:** Resources (lead); Software (equal); Validation (equal). **A. Alian:** Formal analysis (supporting); Methodology (supporting); Validation (equal). **E. Camerotto:** Resources (equal); Validation (supporting). **A. Milenin:** Resources (equal); Validation (supporting). **N. Pinna:** Resources (equal). **S. El Kazzi:** Resources (equal). **D. Lin:** Project administration (equal); Supervision (supporting). **P. Lagrain:** Resources (supporting). **P. Favia:** Resources (supporting). **H. Bender:** Resources (supporting). **N. Collaert:** Project administration (equal); Resources (equal); Supervision (equal); Validation (supporting). **K. De Meyer:** Project administration (lead); Resources (equal); Supervision (lead).

DATA AVAILABILITY

The data that support the findings of this study are available within the article.

TABLE II. Transfer length estimated from the fit of the analytical model with measured R_{total} for different diameters.

Nanowire diameter (nm)	L_T estimated from analytical model without considering body depletion (nm)	L_T estimated from modified model with body depletion (nm)
30	752.9	444.1
60	503.6	405.4
80	371.9	315.8
100	333.8	292.9

APPENDIX: TRANSFER LENGTH CALCULATION

The accurate estimation of the transfer length, L_T, is important for designing advanced semiconductor devices and tuning them for high-performance. However, we may note that we do not have the optimal design (of the test structures in this work) for an error free analysis. Some literature studies report variations in L_T estimation, depending on the design of the structures, for very similar contact resistivity, ρ_C values.

In the Table II, we can note (a) how the L_T varies with diameter and (b) the differences in L_T depending on the extraction model used. We must note that for large diameters (80 and 100 nm), ρ_C extracted from both these models match (see Fig. 24), and yet L_T differs.

We could note that L_T estimated without considering body depletion shows much higher values and increases faster with the decreasing diameter. But the ones estimated from the proposed model show a reduction and change less with diameter. All of these suggest that we need better and more accurate models to capture the effects at nanoscale dimensions.

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