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Scaling study of contact operation at constant current in self-aligned top-gated oxide semiconductor field-effect transistors

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ABSTRACT

An extraction framework that can precisely reflect the metal-semiconductor contact behavior is developed for self-aligned top-gated oxide semiconductor field-effect transistors (SA-TG OS FETs). In contrast to the conventional transfer length method, where the extraction is performed at a constant drain voltage condition, an improved constant current scheme, resilient to bias-dependent series resistance, is employed to enhance the extraction accuracy. This technique enables one to unveil the underlying device physics at the metal-OS interface under top-gated operation. Furthermore, the resistance of contact and extension regions can be accurately differentiated by exploiting the extraction results from the three-terminal FETs and two-terminal resistors using the present framework. Moreover, the significant role of the specific contact resistivity at the metal-OS interface is highlighted as the dominating factor that detrimentally affects the electrical performance of OS FETs.

1. Introduction

AMONG different material systems, oxide semiconductors (OS) offer great potential as a semiconducting channel for monolithic integration on silicon complementary metal-oxide-semiconductor (CMOS) technology [1–3]. However, the performance of OS field-effect transistors (FETs) has often been limited by the metal-semiconductor contact, necessitating a comprehensive understanding of their underlying transport mechanism at the metal-OS interface. The contact resistance (R_c) and the specific contact resistivity (ρ_c) are the essential metrics to evaluate the carrier injection through the metal-semiconductor junction [4]. The accurate determination of R_c and ρ_c is non-trivial to elucidate the underlying device physics, practically offering informative insights in optimizing the transistor performance.

The transfer length method (TLM) has been commonly employed to characterize the series resistance (R_{SD}), in which a set of FETs with various gate lengths (L_g) is needed. Note that the notation of R_{SD} is used to differentiate from R_c, as R_c is a specific parameter that accounts only for the resistance value at the metal-semiconductor junction. In contrast, the R_{SD} is a generic term that incorporates all the resistance components apart from the channel resistance (R_{ch}).

To extract the so-called R_{SD} from TLM, one has to calculate the total resistance (R_o) to L_g within the linear regime, and R_{SD} is determined by extrapolating to the y-intercept of the R_o-L_g plot [4–8]. The above procedure is applicable only when the L_g measured by scanning electron microscope (SEM) or transmission electron microscope (TEM) matches precisely the effective channel length (L_{eff}). This prerequisite is, however, challenging for OS FETs, and the origin can be attributed to i) the deviation created in the photolithography process, ii) the lateral diffusion of hydrogen atoms [9,10], and iii) the creation of oxygen vacancies during the contact-via etching process [11]. Note that the R_{SD} extraction from the y-intercept of the R_o-L_g plot can be problematic if L_g differs from L_{eff}. Alternatively, the convergence point of two adjacent regression lines is taken as the estimated R_{SD}, and the corresponding length is the difference between L_g and L_{eff}. This approach allows one to trace the R_{SD} and L_{eff} that evolve with gate voltage (V_G) if the extrapolation does not intercept reasonably at the y-axis [12–16].

It should be mentioned that the aforementioned methods have mostly adopted a constant drain voltage (V_D) scheme, meaning that the calculation of R_o throughout the whole set of FETs is performed at a fixed V_D condition (*e.g.*, $V_D = 0.1$ V) that targets FET operation in the linear regime. We would like to argue that although the constant V_D setup is intuitive, it is inappropriate to characterize R_{SD}. In the practical scenario, R_{SD} is a function of V_D and V_G, and the constant V_D scheme

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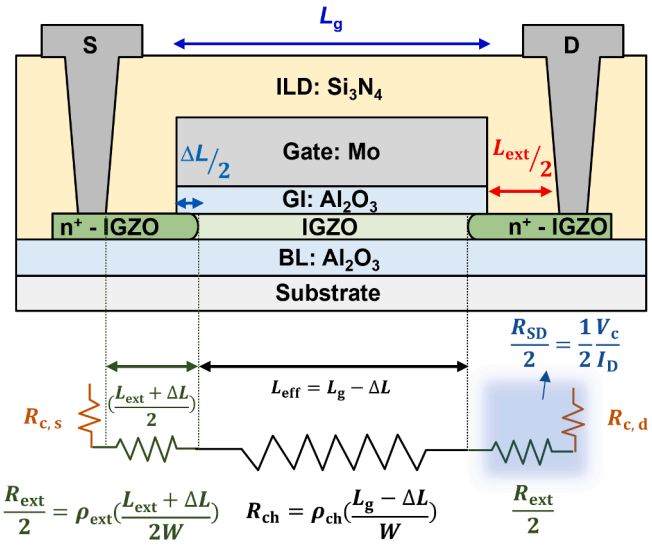

Fig. 1. Schematic and the resistance elements of a SA-TG OS FET.

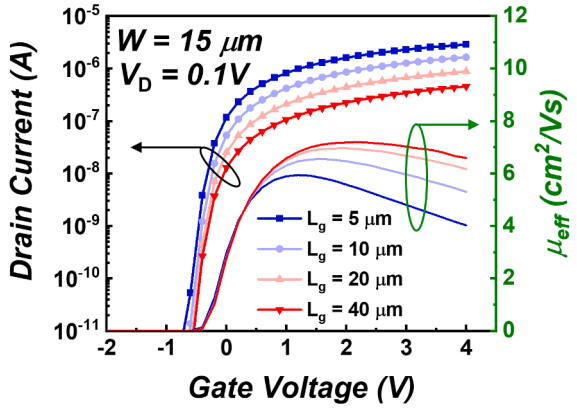

Fig. 2. The I_D-V_G curves and the corresponding μ_{eff} of OS FETs with various L_g at V_D = 0.1 V.

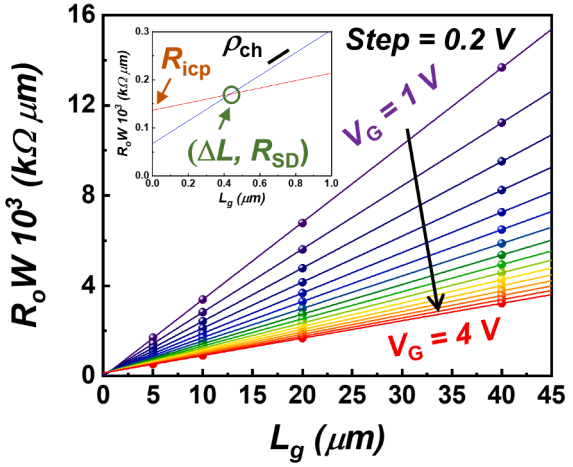

Fig. 3. R_oW versus L_g plot with V_G = 1 V to V_G = 4 V at I_D = 80 nA. The inset graphically defines the physical interpretation of the convergence point from two adjacent V_G values.

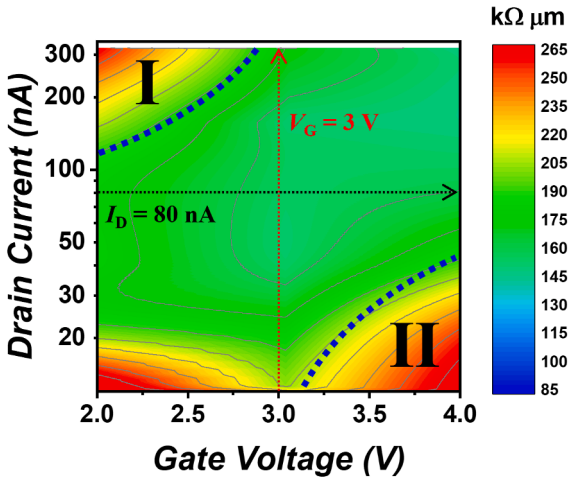

Fig. 4. The extracted contour plan of R_{SD} as a function of V_G and I_D with the color scale bar shown in the right side.

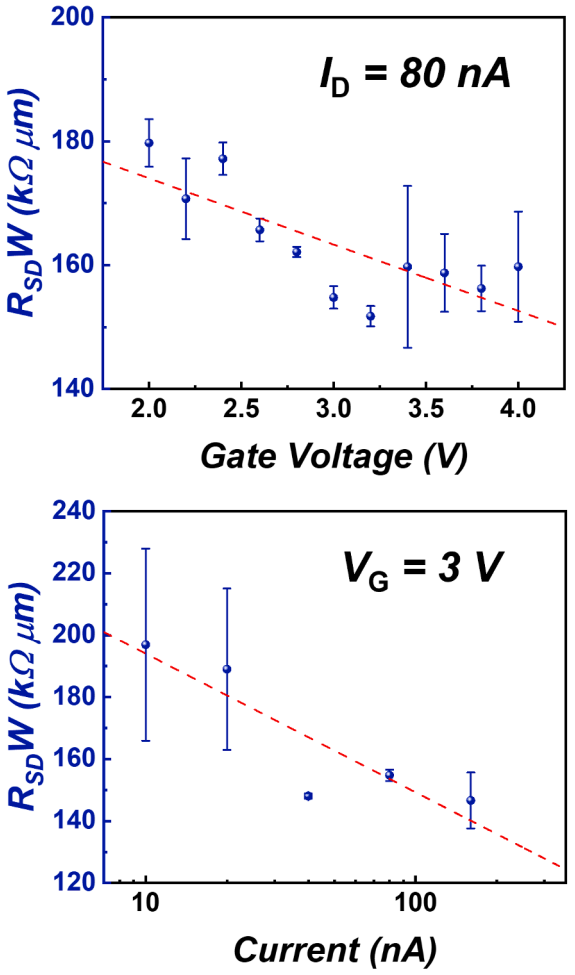

Fig. 5. The extracted R_{SD} from Fig. 4 as a function of (a) V_G with I_D = 80 nA and (b) I_D with V_G = 3 V with estimated errors. The corresponding extraction lines are indicated in Fig. 4.

creates an uneven voltage drop across the contact area (V_c) for FETs with different L_g, self-violating the assumption that the bias-dependent R_{SD} value has to be identical across different L_g in the extrapolation procedure. For instance, V_c can be higher in short L_g (*e.g.*, L_g = 5 μm) than those with long L_g (*e.g.*, L_g = 40 μm) under a fixed V_D condition. It is,

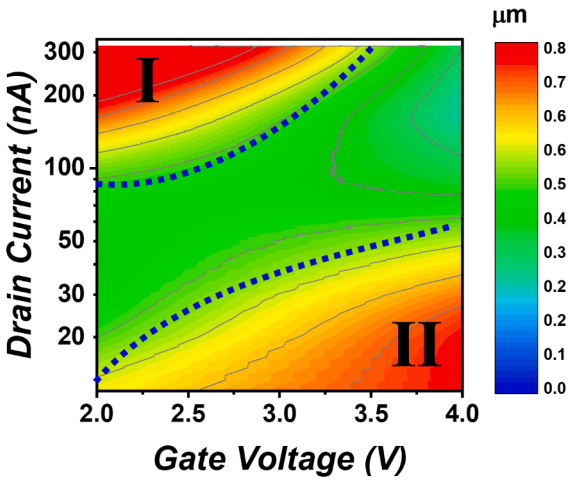

Fig. 6. The extracted contour plan of ΔL as a function of V_G and I_D with the color scale bar shown in the right side.

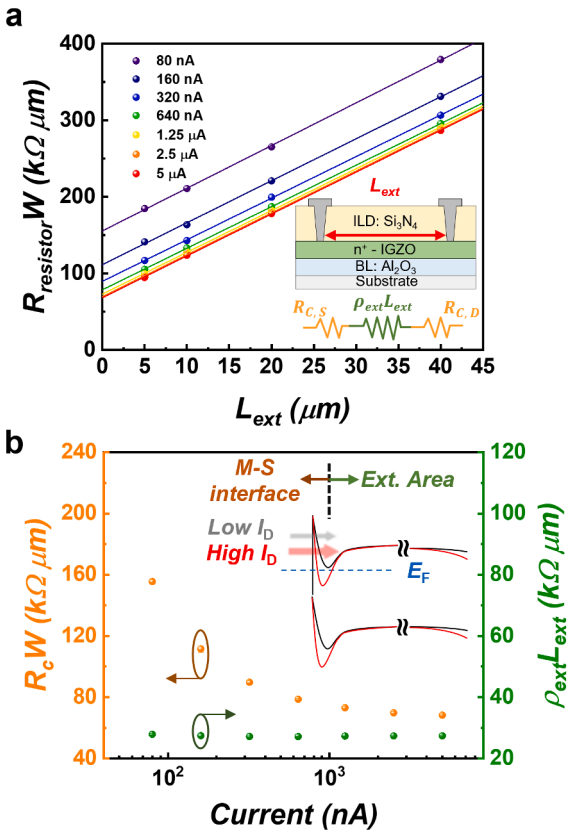

Fig. 7. (a) $R_{resistor}W$-L_{ext} plot under various I_D from 80 nA to 5 μA. Inset shows the schematic of a two-terminal resistor configuration. (b) Extracted R_c and R_{ext} as a function of I_D with $L_{ext} = 10$ μm. Inset depicts the energy band diagram at the metal-OS interface.

therefore, non-trivial to maintain a constant V_c to preserve the accuracy of the R_{SD} extraction [17,18].

Another aspect that has been less explored in self-aligned top-gated (SA-TG) OS FETs is the decomposition of the extracted R_{SD}. The resistance components of R_{SD} comprise of R_c and extension resistance (R_{ext}) for a top-gated configuration, as depicted in Fig. 1, where ΔL is the channel length deviation caused by channel doping (*e.g.*, $\Delta L = L_g$-L_{eff}). It is argued from the fundamental standpoints that decoupling these resistance elements is pivotal in further optimizing the device

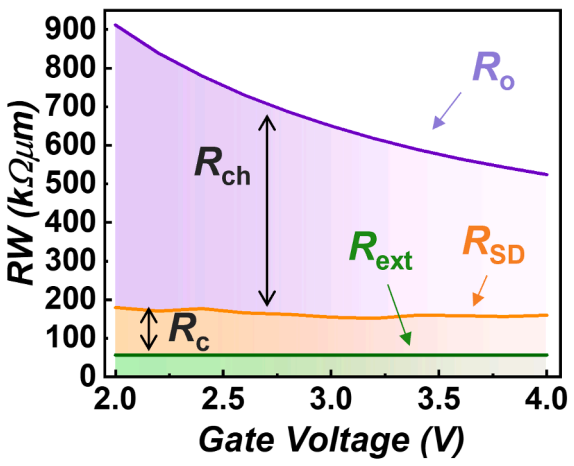

Fig. 8. Decomposed R_{ch}, R_c, and R_{ext} as a function of V_G of a $L_g = 5$ μm OS FET at $I_D = 80$ nA. Green, orange, and purple lines correspond to R_{ext}, R_{SD}, and R_o, respectively. The areas between these lines, from bottom to top, represent R_{ext}, R_c, and R_{ch}, respectively. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

performance and elucidating the carrier conduction mechanism in SA-TG OS FETs.

In this article, a constant current transfer length method (CC-TLM) is employed to account for the bias-dependent R_{SD} behavior in the SA-TG OS FETs [17]. We focus on the SA-TG configuration because it manifests substantial potential for fast switching speed due to the negligible parasitic capacitance compared to the bottom-gated counterparts [19,33]. The extraction results show that R_{SD} can be effectively modulated by the V_G and V_D, whereas a constant ΔL value is obtained. The series resistance elements, namely the bias-dependent R_c and the bias-independent R_{ext}, are subsequently differentiated by incorporating the analysis results of using the two-terminal resistors without requiring additional fabrication steps. It should be noted that a systematic analysis of decoupling the resistance components in SA-TG OS FETs is still missing. Our study further suggests that the specific contact resistivity (ρ_c) is the main obstacle hindering the performance of SA-TG OS FETs, and the R_c is predominately limited by the available contact length (L_{cont}). This work could offer a generic extraction framework to elucidate the underlying contact operation for SA-TG OS FETs, and the extracted parameters may help guide the dimensional design for the devices.

2. Experiment

The SA-TG amorphous indium-gallium-zinc oxide (a-InGaZnO) FETs were fabricated, as shown in Fig. 1. The detailed process parameters are described elsewhere [19]. Notably, a 10 nm a-InGaZnO active layer was deposited on a glass substrate with an aluminum oxide (Al_2O_3) buffer layer (BL). A 20 nm Al_2O_3 gate insulator (GI) layer was formed by atomic layer deposition (ALD), followed by gate metal deposition. A 200 nm silicon nitride (Si_3N_4) was grown as an interlayer dielectric (ILD). The source/drain (S/D) contacts were formed using 10/50/10 nm titanium/aluminum/titanium (Ti/Al/Ti) metal layers. Electrical measurements were performed by Agilent 4156C under the ambient condition at room temperature. All the measured OS FETs share identical channel width (W) of 15 μm.

In the employed constant current method, the applied V_D for each FET with different L_g was automatically adjusted by the source measurement unit (SMU) of the parameter analyzer to adapt for constant current conditions during the V_G sweep. The voltage compliance at the drain electrode is required to prevent permanent damage (*i.e.*, dielectric breakdown). Note that the adjusted V_D tends to overshoot when V_G is adjacent to the threshold voltage (V_T) where the R_{ch} is significant. The

Table 1
Values Extracted From Os Fet At Different Regimes Of Operation.

I_D (nA)	ρ_c (Ωcm^2)	ρ_{ext} (kΩ/□)	ρ_{ch} (kΩ/□)	R_c (k$\Omega\mu$m)	R_{ext} (k$\Omega\mu$m)	R_{ch} (k$\Omega\mu$m)	L_T (μm)	ΔL (μm)	L_{cont} (μm)	L_{ext} (μm)	L_g (μm)	W (μm)
20	*N/A*	*N/A*	77.25	*N/A*	*N/A*	354.58	*N/A*	0.41	5	10	5	15
80	3.73×10^{-3}	5.58	77.18	103.15	58.16	352.71	13.95	0.43	5	10	5	15
320	2.24×10^{-3}	5.43	77.68	90.12	56.61	355.77	8.25	0.42	5	10	5	15

Not applicable (*N/A*). ρ_{ch}, R_c, and R_{ch} are calculated at $V_G = 4$ V.

constant current conditions are carefully selected and monitored to ensure that the applied V_D resides within the linear regime (V_G-$V_T \gg V_D$) throughout the entire extraction region (*e.g.*, V_G = 2 V to 4 V) for different L_g. The overloaded V_D with high input current (*e.g.*, V_G-$V_T \leq V_D$) should be excluded as the measured FETs consequently operate in the saturation regime that is not applicable to the present technique.

3. Improved constant current method

Fig. 2 shows the transfer characteristics (I_D-V_G) and the effective mobility (μ_{eff}) with various L_g at V_D = 0.1 V. μ_{eff} is calculated by the transconductance method (g_m) as.

$$\mu_{eff} = \frac{g_m L_g}{W C_{ox} V_D} \tag{1}$$

where g_m is defined as $\partial I_D/\partial V_G$, W is the channel width, and C_{ox} is the oxide capacitance per unit area determined by the capacitance-voltage (C-V) measurement. Note that the g_m method has been considerably employed in the literature to determine the mobility in FETs, despite the substantial flaw of this technique [4].

On the other hand, the TLM can separately extract R_{SD} and intrinsic charge carrier mobility (μ_{int}) from the I_D-V_G curves with different L_g. This technique presumes that the contact and channel properties are identical across the tested devices in which a linear extrapolation is performed to extract the parameters. The measurements are typically conducted under a constant V_D condition (*e.g.*, V_D = 0.1 V) that implicitly assumes an ideal ohmic contact behavior. This assumption, however, oversimplifies the practical scenario since carrier injection generally shows non-trivial bias dependence [4,20]. Furthermore, the constant V_D condition substantially varies the voltage drop across the contacts for FETs with different L_g and thus makes the extracted R_{SD} dubious.

Therefore, the CC-TLM is employed to mitigate the errors created by the conventional approach, where a consistent voltage drop across the contact regions is ensured for all channel lengths [17]. The applied V_D is automatically adjusted to achieve the constant current conditions throughout the V_G sweep for FETs with different L_g. Fig. 3 shows the R_o-L_g plots under various V_G from 1 V to 4 V at the constant current (I_D) of 80 nA. All the measured OS FETs operate in the linear regime in such conditions, and a reasonable linear extrapolation can be attained under the entire V_G sweep. The total resistance, R_o, is written as.

$$R_o W = R_{SD} W + \rho_{ch}(L_g - \Delta L) \tag{2}$$

ρ_{ch} is the channel sheet resistance. Accordingly, the R_{SD} and ΔL can be extracted from the convergence point of the R_o-L_g plots between two adjacent V_G values, as indicated in the inset of Fig. 3 [12–16,21,22].

The constant current levels are subsequently varied from 10 nA to 320 nA to explore the carrier injection behavior in OS FETs. The contour plan of the extracted R_{SD} as a function of V_G and I_D conditions is shown in Fig. 4, which manifests that the R_{SD} can be effectively modulated by the measured conditions. More specifically, the extracted R_{SD} decreases with both the gate and drain biases, as shown in Fig. 5 (a) and (b), respectively, evidencing the non-ohmic behavior of charge transport in the non-channel region. Notably, the extracted R_{SD} shows less V_G dependency than I_D (*e.g.*, different I_D at identical V_G), which can be attributed to the SA-TG configuration. The absence of direct overlapping of gate and contact electrodes makes the modulation of R_{SD} by V_G less effective than FETs with a staggered configuration. Nevertheless, the observation further highlights the deficiency of the conventional constant V_D method that neglects the V_D-dependent R_{SD}.

It should be noted that the prominent extraction errors observed in the region I of Fig. 4 can be attributed to the unfulfillment of the linear condition (V_G-$V_T \gg V_D$) in long channel FETs. The applied V_D for the long channel FET (*e.g.*, L_g = 40 μm) has to be increased at small V_G conditions to achieve the identical I_D as of the short channel FET (*e.g.*, L_g = 5 μm), inevitably introducing errors in the R_{SD} extraction. For instance, a V_D of 0.15 V is supplied to achieve a I_D of 300 nA with L_g = 40 μm, and the gate overdrive ($V_{OV} = V_G$-V_T) at V_G = 2 V is calculated as ~ 1 V ($V_T \sim 1$ V in Fig. 2). Note that the quantitative criteria to ensure a linear-region operation is defined as (V_G-V_T)/m, where m is a constant that describes the voltage transfer efficiency to the surface potential, ψ_s, as $d\psi s/dV_G = 1+(C_{os}/C_{ox})+(C_{it}/C_{ox})$ [23]. The C_{os} and C_{it} denote the semiconductor and interface trap capacitances, respectively. Assuming the relative dielectric constant of the oxide semiconductor and Al_2O_3 as 16 and 8, respectively, and the interface trap density ($D_{it} = q^{-1}C_{it}$) of ~ 10^{12} $eV^{-1}cm^{-2}$, the m of ~ 5.5 can be calculated [24]. Consequently, the criteria of (V_G-V_T)/m at V_G = 2 V becomes 0.18, similar to the applied V_D condition (V_D = 0.15 V) to achieve a I_D of 300 nA for devices with L_g = 40 μm. In other words, the linear region operation (*e.g.*, V_G-$V_T \gg V_D$) cannot be firmly ensured for L_g = 40 μm at the aforementioned condition, and thus potentially introducing the error during extraction.

On the other hand, the extracted R_{SD} deviates in region II, where a large V_G is applied (*i.e.*, $V_G > 3.5$ V), as the corresponding V_D is very low and exhibits considerable fluctuation. For instance, a V_D of ~ 300 μV is applied to supply a I_D of 10 nA for devices with L_g = 5 μm. However, this applied V_D condition is approaching the resolution limit of our SMUs (*e.g.*, ~ 100 μV). Thus, the extraction within this region could be unreliable and is susceptible to measurement noises. One should note that it is practically challenging to define precisely the extraction margin of regions I and II, so the drawn lines are, strictly speaking, only applicable to guide the eye. Nevertheless, the bias-dependent R_{SD} behavior shown in Fig. 4 demonstrates that the present method is capable of capturing the detailed mechanism of the carrier conduction in OS FETs.

Additionally, L_{eff} is an essential aspect in evaluating the process technology. To this end, ΔL is extracted in which the contour plan is created in Fig. 6. The extracted ΔL virtually exhibits an independent behavior of V_G and I_D within the reliable measurement conditions (see the blue dash lines in Fig. 6). The extraction results in region I and II are not included in the discussion due to the inherent errors mentioned in the above paragraph. However, the extraction of ΔL shows a broader error window than the extracted R_{SD}. (*i.e.*, region II in Fig. 4 and Fig. 6). Note that the ΔL values are calculated from the slope of the R_{icp}-ρ_{ch} curves from two adjacent V_G biases, in which R_{icp} and ρ_{ch} are the fitted y-intercept and slope of the R_o-L_g plot, respectively (see Fig. 3) [21,22]. One plausible explanation is that a slight deviation from the extracted R_{icp} and ρ_{ch} could substantially raise the uncertainty in determining ΔL, given that the first derivative is highly sensitive to errors. In OS FETs, ΔL could be caused by hydrogen originating from the interlayer dielectric layer that diffuses inwards in the channel under the top gate electrode. Indeed, hydrogen atoms act as an n-type dopant for the OS layer that can degenerate the underlying extension region [9,10,25–27]. The values of ΔL remain in the low range ($\Delta L \sim 0.4$ μm) of previously published values ($\Delta L > 1.0$ μm) with silicon dioxide (SiO_2) GI, implying that the low-temperature ALD Al_2O_3 could be a suitable diffusion barrier against

hydrogen atoms [9,10,14–16].

4. Series resistance decomposition

Although the R_{SD} has been characterized in the above section, the resistance components of R_{SD} remain unclear. It is, however, imperative to decouple them to further elucidate the underlying device physics. The R_{SD} comprises of the R_c and R_{ext} as.

$$R_{SD} = R_c + R_{ext} \tag{3}$$

The parasitic metal resistance (R_m) is neglected in (3), which can be justified by the subsequent extraction results of ρ_c (*e.g.*, $R_c \gg R_m$), showing a negligible contribution from R_m. Note that R_c is equivalent to the contact-front resistance in the transmission line theory [4]. A set of two-terminal resistors [see the inset of Fig. 7 (a)] with different lengths is employed to decompose the resistances listed in (3) using the constant current scheme. Such two-terminal configurations are useful for the precise characterization of OS FETs and can be easily integrated as they do not require additional photolithography steps. The resistance of the measured resistors ($R_{resistor}$) can be written as.

$$R_{resistor}W = R_cW + \rho_{ext}L_{ext} \tag{4}$$

Where ρ_{ext} and L_{ext} are the sheet resistance and length of the extension region, respectively. To extract R_c and ρ_{ext}, $R_{resistor}$ with various L_{ext} is plotted under different current conditions, as shown in Fig. 7 (a). Good linear regression can be acquired from the current level of 80 nA to 5 μA, indicating that the R_c and ρ_{ext} can be reliably extracted from the *y*-intercept and slope of (4), respectively. Note that a higher current range is selected than the FET measurements, as a sufficiently large current is needed to produce a stable voltage signal in the resistor configuration due to its high conductivity.

The extracted R_c and R_{ext} as a function of current are shown in Fig. 7 (b). One can clearly observe that R_c decreases with the input current, whereas the R_{ext} exhibits a current-independent behavior. The above results can be explained by the inset of Fig. 7 (b), in which a Schottky-like metal-OS contact is responsible for the observed current-dependent R_c. Subsequently, the carriers conduct through the metallic-like ohmic extension region.

Moreover, Fig. 7 allows one to estimate the ρ_c at the metal-semiconductor interface by the transmission line theory, considering the current crowding effect as.

$$R_cW = \rho_c/L_T coth(L_{cont}/L_T) \tag{5a}$$

$$\approx \rho_c/L_T when 1.5L_T \le L_{cont} \tag{5b}$$

$$\approx \rho_c/L_{cont} when 0.5L_T \ge L_{cont} \tag{5c}$$

L_{cont} and L_T denote the contact and transfer length [4,28,30]. By assuming that the sheet resistances in both the extension ($\rho_{sh,ext}$) and contact ($\rho_{sh,c}$) regions are identical, one can estimate L_T of 13.95 μm and 8.25 μm from the *x*-intercept of Fig. 7 (b) at the current level of 80 nA and 320 nA, respectively. These estimated values are prominently higher than L_{cont} (=5 μm). In consequence, the hyperbolic cotangent term in (5a) can be simplified, and ρ_c is extracted from (5c), which is insensitive to the error arising from the determination of L_T. This yields ρ_c of 3.73×10^{-3} Ωcm^2 and 2.24×10^{-3} Ωcm^2 at the current level of 80 nA and 320 nA, respectively. These values are at least five orders higher than the silicon technology (~10^{-9} Ωcm^2), which urgently requires considerable improvement [31,32]. Note that the extracted ρ_c at $I_D = 80$ nA can be justified by fulfilling $0.5L_T \ge L_{cont}$, whereas the ρ_c value from $I_D = 320$ nA is a rough approximation. To accurately and comprehensively determine the ρ_c values at different current levels, it is necessary to adopt other approaches, such as the contact-end measurement [4,29,30].

As a final step, the resistive elements present in the FET are decomposed at a constant current of $I_D = 80$ nA, as shown in Fig. 8 for an OS FET of $L_g = 5$ μm. In this graph, R_{ext} is calculated from the ρ_{ext} value obtained from the two-terminal resistor multiplied by $L_{ext} + \Delta L$. R_{ch} is calculated from channel sheet resistivity ρ_{ch} obtained from the TLM analysis multiplied by L_g-ΔL. Finally, R_c is obtained from (3), using the R_{SD} values extracted from CC-TLM analysis. Table 1 summarizes the extracted values of various resistive elements from different constant current conditions. Fig. 8 shows unambiguously that R_c occupies most of the resistance portion in R_{SD} (R_c/R_{SD} ~ 65 %), hindering the device performance of the OS FETs. When increasing V_G, R_{SD} expectedly rises to nearly half of R_{ch} at $V_G = 4$ V. It is clear that further downscaling of channel and extension lengths would result in a contact-dominated device as R_c would only rise if L_{cont} is downscaled along with the other FET dimensions.

It should be noted that the aforementioned discussion can only be conducted if one employs the concept of CC-TLM [17] on both three-terminal FETs and two-terminal resistors and in conjunction with Terada's method to extrapolate R_{SD} and ΔL [12]. Furthermore, the analysis stresses the importance of developing strategies to minimize R_c (ρ_c) at the metal-OS interface to benefit from the effort spent on downscaling the SA-TG OS FETs configuration in the sub-μm range (*i.e.*, L_g ~ 0.1 μm).

5. Conclusion

An improved methodology was exploited to accurately account for the bias-dependent R_{SD} in the SA-TG OS FETs. Indeed, the extraction results demonstrated that the R_{SD} can be effectively modulated by both the V_G and V_D, validating the applicability of the present technique for SA-TG OS FETs. Additionally, a two-terminal resistor configuration was employed to precisely differentiate the resistance elements of R_{SD}. This study highlighted that the substantial ρ_c is the dominating factor that considerably limits the device performance of OS FETs. More importantly, the presented analyses could offer a systematic extraction framework to clarify the underlying mechanisms for SA-TG OS FETs, which is practically indispensable to further enhance their electrical performance.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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