Characterization of the Total Charge and Time Duration for Single-Event Transient Voltage Pulses in a 65-nm CMOS Technology

Zheyi Li, *Student Member, IEEE*, Laurent Berti, Jan Wouters, Jialei Wang, *Member, IEEE*, and Paul Leroux, *Senior Member, IEEE*

***Abstract*— This article presents the circuits and heavy-ion irradiation test results of a single-event transient (SET) measurement chip in a 65-nm complementary metal–oxide–semiconductor (CMOS) technology. The measurements contain two parts: total SET ionization charge and SET pulse duration. Transistors with different types and dimensions were implemented as victim devices to evaluate how transistor parameters impact the SET effects. Additionally, SET variation from different supply voltages was also investigated. The test chip has been tested under a heavy-ion beam with an effective linear energy transfer (LET) from 20.4 to 88.35 MeV $\cdot$ cm^2/mg using a 0°–45° incidence angle.**

***Index Terms*— Complementary metal–oxide–semiconductor (CMOS), single-event effects (SEEs), single-event transient (SET).**

I. Introduction

SINGLE-EVENT effects (SEEs) on very-large-scale integration (VLSI) circuits can be caused by energetic particles. When a particle strikes the sensitive regions of a microelectronic device, free charge will be created by ionization. A momentary voltage perturbation will be present if the free charge is collected by the sensitive region of analog circuits or combinatorial logic. This type of voltage perturbation is called a single-event transient (SET) [1]–[3]. If the charge is collected by storage circuits such as static random access memory (SRAM), SET can cause other effects such as single-event upsets (SEUs) and multiple cell upset (MCU) [4], [5].

With the shrinking technology size and increasing operational frequency, the parasitic capacitances become smaller, which causes transistors to be more sensitive to SETs [6], [7]. Thus, in the design phase of the SET-hardened applications or SET characterization chip, one of the important procedures is performing the SET response simulation using an SET electrical current model [8]. This simulation can help find out SET weak points and optimizing the design together with radiation-hardening by design (RHBD) techniques. The current model is based on a double-exponential current pulse which relates to the amount of collected charge and node time constant [9]. Therefore, on-chip characterization of the total SET ionization charge and pulse duration is necessary for achieving a reliable and accurate current model.

The characterization of SET pulses has been performed with a variety of techniques in previous researches [2]. In some works, the SET voltage pulses have been measured directly through oscilloscopes [10], [11]. However, this method is limited by parasitics and loading effects. Multiple latches with delayed signal paths have been implemented for on-chip SET pulsewidth measurement [12]. The bottle neck of this method is that to quantify the pulsewidth, multiple identical hits are needed. Another technique uses a chain of identical cells, which forms a signal delay chain, to quantify the transient pulsewidth by counting the number of flipped cells [13]–[16]. In the 65-nm technology, several articles characterized the SET pulse duration based on this method. The SET pulses are generated in an inverter chain or sequential logic [17]–[20]. However, SET pulses in these works are generated from the inverter chain, which can be disturbed by the "propagation-induced pulse broadening" (PIPB) effect and cause an inaccurate evaluation [11], [21]. For charge measurement, only off-chip measurement on collected charge had been reported in [17]. None of the previous work performed on-chip charge characterization for single transistors in 65 nm.

This article presents an SET test chip in a 65-nm technology. It contains the on-chip SET total ionization charge measurement based on single transistors and SET pulse duration measurement circuits based on a single-stage inverter. Furthermore, the SET characterization results can be collected and compared for various device types, dimensions, and supply voltages.

II. SET Measurement Methodology

A. Victim Devices

In the test chip, eight typical MOSFETs were chosen as victim devices and implemented. The size information of the

Manuscript received 19 October 2021; revised 19 November 2021; accepted 2 January 2022. Date of publication 6 January 2022; date of current version 18 July 2022. This work was supported in part by the European Union's Horizon 2020 Research and Innovation Programme through the framework of RADSAGA under Grant 721624.

Zheyi Li is with the Department of ICLINK, imec, 3001 Leuven, Belgium, and also with the Department of Electrical Engineering (ESAT), KU Leuven, 2440 Geel, Belgium (e-mail: zheyi.li@imec.be).

Laurent Berti and Jan Wouters are with the Department of ICLINK, imec, 3001 Leuven, Belgium.

Jialei Wang and Paul Leroux are with the Department of Electrical Engineering (ESAT), KU Leuven, 2440 Geel, Belgium.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TNS.2022.3141070.

Digital Object Identifier 10.1109/TNS.2022.3141070

0018-9499 © 2022 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See https://www.ieee.org/publications/rights/index.html for more information.

Authorized licensed use limited to: IMEC. Downloaded on August 03,2022 at 08:25:13 UTC from IEEE Xplore. Restrictions apply.

TABLE I
VICTIM DEVICES IMPLEMENTED ON CHIP

Index	Victim Devices	Width	Finger	Length
VD0	Core nMOS	10 μm	10	60 nm
VD1	Core nMOS	10 μm	10	500 nm
VD2	Core DNW nMOS	10 μm	10	500 nm
VD3	Core pMOS	10 μm	10	60 nm
VD4	Core pMOS	10 μm	10	500 nm
VD5	IO nMOS	10 μm	10	500 nm
VD6	IO pMOS	10 μm	10	500 nm
VD7	IO DNW nMOS	10 μm	10	500 nm

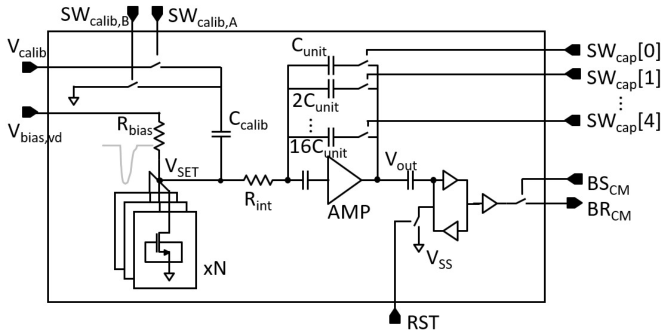

Fig. 1. Block diagram of the n-type SET charge measurement.

victim devices is shown in Table I. Several comparisons can be made between different sizes and types of victim devices as follows.

1) Results between n-type and p-type devices.
2) Results between deep n-well (DNW) and non-DNW devices.
3) Results between $L = 60$ nm and $L = 500$ nm.
4) Results between core devices (thin oxide transistors with 1.2-V normal supply voltage) and input–output (IO, thick oxide transistors with 2.5-V normal supply voltage) devices.
5) Results between different power supplies.

The reverse-biased junction is the most charge-sensitive part of MOSFET. SET worst case happens when a MOSFET is in the OFF-state and a single particle (proton or heavy ion) passes the drain depletion region. Then, a voltage pulse will appear at the drain node [3]. This voltage pulse can be used to quantify the total ionization charge and pulse duration by different measurement circuits. When calculating the sensitive area of the test chip, only the drain size is considered. However, from the SET results demonstrated later in the text, the gate and even the source area also need to be considered.

B. Ionization Charge Measurement Circuits

The collected ionization charge can be measured by integrating the SET voltage pulse at the drain node [22]. The SET charge measurement block based on charge integration for the n-type victim devices is shown in Fig. 1. The SET charge measurement circuits for p-type victim devices have a similar structure.

N OFF-state victim devices (nMOS) are biased by a resistor $R_{\text{bias}} = 1$ MΩ to achieve a high resistance node at V_{SET}. The number of victim devices N was calculated from the expected hit probability and total sensitive area, which is considered to be the drain area of the victim MOSFET. Besides, the parasitic capacitance at V_{SET} is kept at 5 pF to have the same load effect for each type of victim device. The bias voltage of the victim devices $V_{\text{bias,vd}}$ is dedicated and adjustable to evaluate the influence of supply on SET charge characteristics. When an SET occurs at one of the victim devices, the voltage pulse at node V_{SET} is integrated by a voltage integrator. The integrator's feedback consists of five binary-weighted capacitors and series switches. These switches are controlled by digital input bits $\text{SW}_{\text{cap}}[4:0]$. By switching $\text{SW}_{\text{cap}}[4:0]$, the integrator output V_{out} can be changed according to the following equation:

$$V_{\text{out}} = \frac{Q_{\text{SET}}}{C_{\text{unit}} n_{\text{cap}}} = \frac{1}{C_{\text{unit}} \sum_0^4 2^i \text{SW}_{\text{cap}}[i]} \int_0^t \frac{V_{\text{SET}}}{R_{\text{int}}} dt \tag{1}$$

where Q_{SET} is the ionization charge from the SET at node V_{SET} and n_{cap} is the number of activated unit feedback capacitors in the integrator.

After integration, the output voltage is sent to a latch. The latch input is reset to V_{SS} before each measurement. When there is no SET or V_{out} is lower than the latch threshold $V_{\text{th,latch}}$, the block output BR_{CM} remains low. Otherwise, the latch will flip and BR_{CM} will become high. Therefore, by tuning the number of connected capacitors, a threshold charge of the measurement circuit Q_{th} can be set according to the following equation. If Q_{SET} is higher than Q_{th}, BR_{CM} will become high

$$Q_{\text{th}} = V_{\text{th,latch}} C_{\text{unit}} \sum_0^4 2^i \text{SW}_{\text{cap}}[i]. \tag{2}$$

Before the irradiation test, the transfer function between the threshold charge Q_{th} and n_{cap} needs to be characterized. The principle is injecting a known amount of charge into the integrator. From Fig. 1, capacitor C_{calib} is connected to node V_{SET}. The C_{calib} value is measured directly from a network analyzer. During the calibration mode, $\text{SW}_{\text{calib},A}$ is closed and $\text{SW}_{\text{calib},B}$ is open. C_{calib} is connected to V_{calib}. After the circuits are fully reset, $\text{SW}_{\text{calib},A}$ turns off and $\text{SW}_{\text{calib},B}$ turns on subsequently. Since node V_{SET} is a high impedance node, the injected charge equals to $V_{\text{calib}} C_{\text{calib}}$. To calibrate a given capacitor level, by sweeping the voltage V_{calib} from low to high, threshold charge Q_{th} equals $V_{\text{calib}} C_{\text{calib}}$ when BR_{CM} just flips.

There are eight types of victim devices, and each type has its own charge measurement circuits. The measurement circuits (integrator, latch, and switches) have a much smaller sensitive area compared with the victim devices and are built with DNW to avoid SET charge sharing. All the measurement circuits are calibrated before the irradiation test separately, and the results are shown in Table II. $Q_{\text{th,min}}$ and $Q_{\text{th,max}}$ indicate the minimum and maximum threshold charge the measurement can reach, which corresponds to $n_{\text{cap}} = 1$ and $n_{\text{cap}} = 31$, respectively. Q_{step} is the average charge per capacitor level in the transfer function.

Authorized licensed use limited to: IMEC. Downloaded on August 03,2022 at 08:25:13 UTC from IEEE Xplore. Restrictions apply.

TABLE II
CHARGE MEASUREMENT CALIBRATION RESULTS

Victim device	Q_{min} (fC)	Q_{max} (pC)	Q_{step} (fC/level)
Core nMOS L = 60nm	188.24	1.41	40.61
Core nMOS L = 500nm	177.63	1.40	40.69
Core DNW nMOS L = 500nm	162.90	1.39	40.63
Core pMOS L = 60nm	212.21	1.65	47.63
Core pMOS L = 500nm	206.63	1.63	47.30
IO nMOS L = 500nm	274.11	3.81	117.46
IO pMOS L = 500nm	321.88	4.33	133.24
IO DNW nMOS L = 500nm	258.73	3.75	115.98

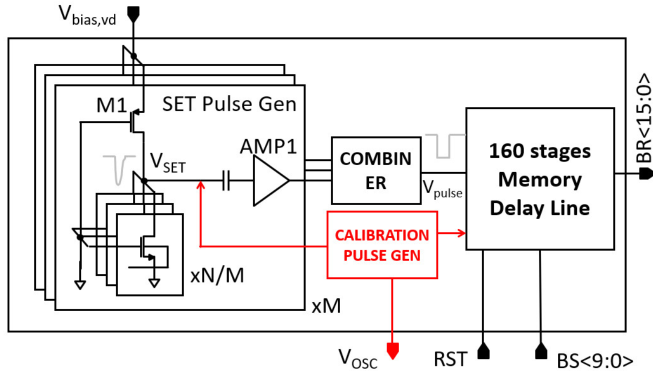

Fig. 2. Block diagram of the n-type SET pulse duration measurement.

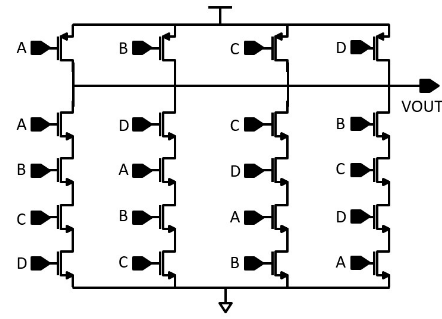

Fig. 3. Balanced NAND gate used in combiner.

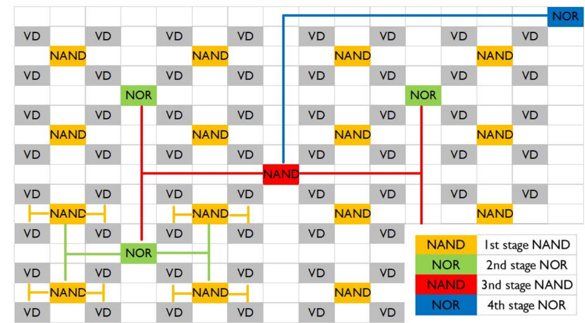

Fig. 4. SET pulse combiner collection tree.

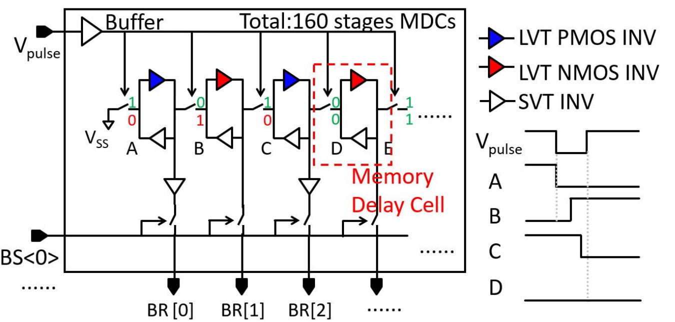

Fig. 5. Block diagram of the MDL.

C. Pulse Duration Measurement Circuits

The pulse duration measurement circuits can be divided into three parts: SET pulse generation blocks, combiner, and memory delay line (MDL). The pulse duration measurement circuits for n-type victim devices are shown in Fig. 2. The measurement circuits for p-type victim devices have a similar structure.

For each type of victim device, N victim devices are scattered into M SET pulse generation blocks. In each generation block, N/M OFF-state victim devices are biased by an ON-state pMOS transistor $M1$. When the ionized particle hits one of the victim devices, the SET voltage pulse at node V_{SET} will be amplified to a square wave by AMP1. The reason for scattering is that the SET pulses are sensitive to the time constant at V_{SET}. M SET generation blocks ensure that the parasitic capacitance at node V_{SET} remains below 100 fF. The benefit of pulse generation blocks compared with the conventional inverter chain used in [17] and [18] is that the SET voltage pulse does not pass an additional inverter chain to reach the measurement circuits. In this way, side effects such as pulse broadening effect are avoided.

Because the victim devices are distributed in M pulse generation blocks, an M-input combiner is used to pick the SET pulse up and send it to the MDL. The combiner has M inputs and consists of four stages four-input NOR and NAND gate. The delay between each input and output is critical to the measurement accuracy. This delay difference should be minimized to have a negligible distortion. Thus, the balanced NOR and NAND gates are used. Fig. 3 shows the balanced NAND gate (same principle for NOR gate), and the redundant nMOS transistors are added to the lower part of the NAND gate to achieve the same parasitic for each input. Besides, the gates are distributed among the victim devices and form a tree structure which is shown in Fig. 4. Like the clock distribution tree, the wire distance from each victim device to the output is identical. As a result, the simulated maximum delay difference is less than 6 ps after the layout.

The MDL shown in Fig. 5, uses the inverter delay as a scale to measure the pulse duration. It is made up of 160 memory delay cells (MDCs), and each MDC contains a latch and a switch. The input switch in each MDC is controlled by the SET pulse signal V_{pulse} from the combiner output. Before the pulse duration measurement, the inputs of odd and even MDC stages are reset to high and low, respectively. When the pulse signal arrives (V_{pulse} changes from high to low), the switches between the latches will be closed and V_{SS} will

Authorized licensed use limited to: IMEC. Downloaded on August 03,2022 at 08:25:13 UTC from IEEE Xplore. Restrictions apply.

TABLE III
CALIBRATION RESULTS OF THE MDL AND CAPTURE CIRCUITS

MDL resolution	19.42 ps/step
MDL detection threshold	38.9 ps
MDL range	3.14 ns
n-type capture circuit delay	233 ps
p-type capture circuit delay	252 ps

start to propagate through the MDL. When the pulse ends, these switches will open and V_{SS} stops propagating. The MDL average stage delay is optimized using the low threshold pMOS and nMOS inverter MDC alternately. Finally, the pulse duration can be calculated by multiplying the number of flipped cells and the average inverter delay. The measurement circuits (bias transistor $M1$, AMP1, combiner, and MDL) have a much smaller sensitive area compared with the victim devices and are built with DNW to avoid SET charge sharing.

Before proceeding with the irradiation test, the pulse duration circuit is calibrated by a known pulse which is sent from the pulse generation circuit (see Fig. 2). This known pulse is first sent to the MDL to characterize the average stage delay of the MDL. Then, an identical pulse is sent to node V_{SET}. The readout difference of the MDL is the delay of the pulse capture circuit (amplifier AMP1 and combiner). The pulse generation circuit is based on a 1601-stage configurable ring oscillator. The oscillator has two operating states: the closed-loop state and open-loop state. When the ring oscillator is in the closed-loop state, the average delay of the inverter $T_{\text{inv,osc}}$ in the oscillator can be derived by measuring the oscillation frequency. Then, the oscillation loop is cut off by opening the inter-stage switch. Then a 1600-stage inverter chain is formed. A pulse with the duration of $T_{\text{inv,osc}} \cdot m$ can be generated by connecting an m-stage (m is an odd number) inverter chain's input and output with a NOR gate. In this way, a known duration pulse is generated.

The detailed calibration results are shown in Table III. MDL is characterized first and the average stage delay is 19.42 ps/step with a detection range from 38.9 ps to 3.14 ns. Then, the delays of the n-type and p-type AMP1 together with the combiner circuits are derived and the results are 233 and 252 ps, respectively.

III. SET EXPERIMENTAL RESULTS

A. Test Chips and Heavy Ion Test Conditions

The test chip was manufactured in a commercial 65-nm technology and bonded to a special package. The package [shown in Fig. 6(a)] has a window on top, from which the heavy ion beam can access the die directly without any thinning. The size of the die is 6.73 mm^2, and the die photograph is shown in Fig. 6(b). The SET charge and pulse duration measurement were implemented on a single die and well-isolated by DNW. The test chips were irradiated with heavy ions at the heavy ion facility (HIF) in UCLouvain, Ottignies-Louvain-la-Neuve, Belgium. Two chips were tested at room temperature and exhibited consistent results. During the test, over 20 000 SET events were observed on each chip. The irradiation conditions are shown in Table IV. In this test,

TABLE IV
IRRADIATION CONDITIONS USED DURING THE TEST

Ion	LET $(MeV{\cdot}\text{cm}^2/mg)$	Angle	LET_{eff} $(MeV{\cdot}\text{cm}^2/mg)$
Nickel	20.4	0°	20.4
Nickel	20.4	45°	28.9
Xenon	62.5	0°	62.5
Xenon	62.5	45°	88.4

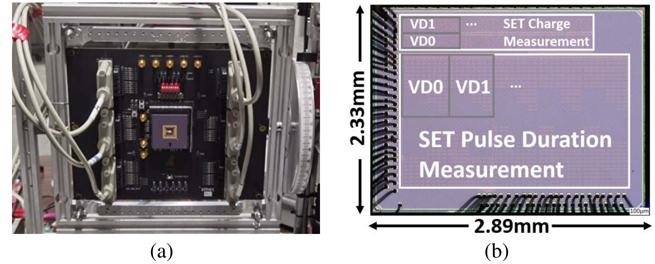

Fig. 6. Test setup and die photograph: (a) test chip and board, and (b) die photograph.

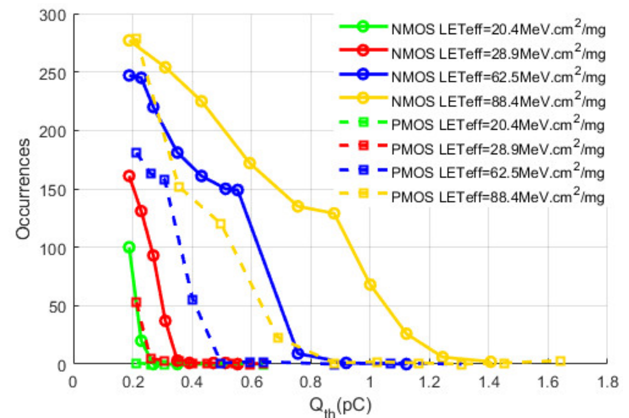

Fig. 7. Measurement results of core nMOS and pMOS with $L = 60$ nm and 1.2-V supply voltage.

nickel and xenon are used with different incidence angles (0° and 45°) to obtain a different effective LET. Further information about the HIF parameters and particles can be found in [23].

B. Ionization Charge Measurement Results

Since the measurement circuits do not quantify the ionization charge directly, it compares the Q_{SET} with Q_{th}. Thus, in each irradiation condition, the measurement was repeated with different Q_{th} to get the full view of distribution. The same effective fluence $\text{Fluence}_{\text{eff}} = 1.5 \times 10^6$ ions/cm^2 was reached in each measurement by changing heavy ion flux and test time.

1) Core Devices' Measurement Results: As shown in Table II, three types of core nMOS and two types of core pMOS transistors are implemented on chip. The measurement results of minimum length (60 nm) core nMOS and pMOS are shown in Fig. 7. When SET ionization charge is higher

Authorized licensed use limited to: IMEC. Downloaded on August 03,2022 at 08:25:13 UTC from IEEE Xplore. Restrictions apply.

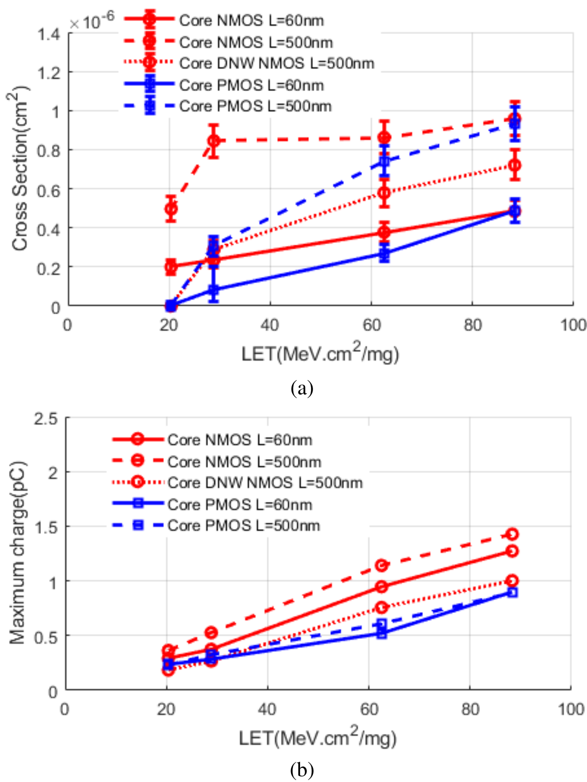

Fig. 8. Core victim devices' measurement results with 1.2-V supply voltage: (a) unit device cross section and (b) maximum collected charge.

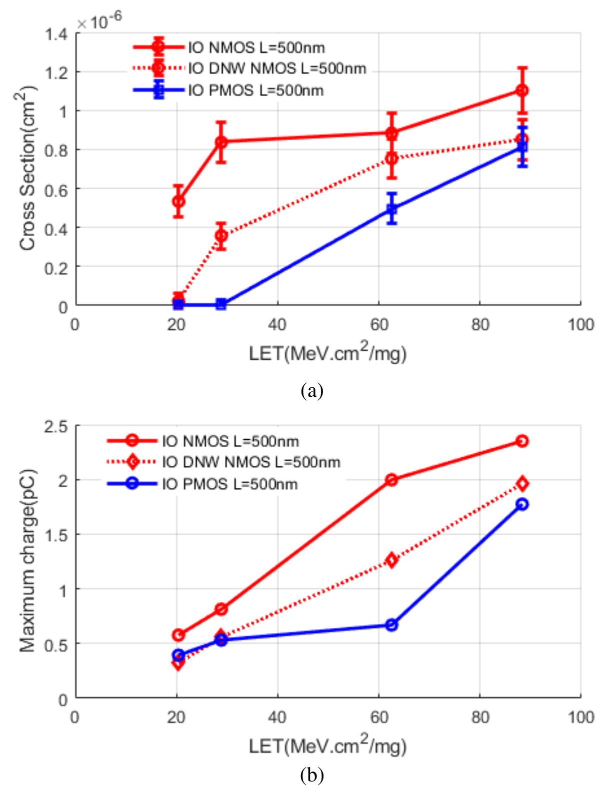

Fig. 9. Charge measurement results of IO devices with 3.3-V supply voltage: (a) unit device cross section and (b) maximum collected charge of all IO victim devices.

than Q_{th}, there will be one reading at the output and this will be considered as one occurrence. At a maximum effective LET of 88.39 MeV$\cdot$cm^2/mg, nMOS and pMOS victims show 277 and 279 occurrences at the minimum Q_{th}, respectively. The higher Q_{th} is set, the lower number of occurrences will get. The number of occurrences at the minimum Q_{th} is used to calculate the unit device cross section (Occurrences @$Q_{\text{th,min}}$/Fluence$_{\text{eff}}$/No. Devices). Then, the unit device cross section of the each nMOS and pMOS transistor is 4.85×10^{-7} and 4.88×10^{-7} cm^2, respectively. However, when Q_{th} is higher, the occurrences of pMOS drop much faster than it does for nMOS. Finally, the maximum collected charge can be read when the occurrences are close to zero. In this case, the maximum charge of pMOS and nMOS transistors is 1.274 and 0.898 pC, respectively. At the lower effective LET case, not only the maximum collected charge but also the unit device cross section of the pMOS devices are lower than for nMOS devices. At the lowest effective LET, the critical charge of pMOS at node V_{SET} does not reach the value to trigger latch even at the minimum Q_{th}.

Similar analyses are applied to all the core victim devices. The unit device cross section and maximum collected charge of all the victim devices at different effective LET are shown in Fig. 8. The error bars in cross section plot, Fig. 8(a), indicates the 95% confidence interval. When effective LET increases, all the unit device cross sections of core devices increase and show a trend of convergence at high effective LET. In general, the unit device cross section is larger than the expected unit device drain area. Specifically, the gate and even source area need to be taken into account. When heavy ions do not directly hit the drain reverse-biased junction but other places like substrate, the charge diffusion in the silicon substrate or the local p/n-well also contributes to charge collection [2]. The amount of diffusion charge depends on the ionization radius of the heavy ions in silicon and the distance between the hit location and the drain node. From [24], 210 MeV Cl (LET $=$ 11.4 MeV$\cdot$cm^2/mg) particles have an ionization radius upto 1 μm in silicon. Therefore, if the distance between the hit point and the drain is less than the ionization radius, ionization charge will be collected through diffusion. This is supported by the results of the devices with different gate length, but identical drain area, where the longer length devices show a larger unit device cross section in Fig. 8(a). It is further observed that pMOS devices show a smaller or equal unit device cross section than nMOS devices at all effective LET. For DNW nMOS devices, the unit device cross section is reduced when compared with non-DNW nMOS devices. The reason is that the part of the charge generated in the p-well region is collected by DNW before it can be collected by nMOS drain [25]. Furthermore, the charge below the p-well/DNW junction cannot be collected by nMOS drain because of the triple-well collection to the n-well tap [25], [26].

The maximum collected charge of all the victim devices at different effective LET is shown in Fig. 8(b). The maximum collected charge increases with effective LET, but does not show a convergent tendency. Similar to the unit device cross section observation, the pMOS devices exhibit a smaller

Authorized licensed use limited to: IMEC. Downloaded on August 03,2022 at 08:25:13 UTC from IEEE Xplore. Restrictions apply.

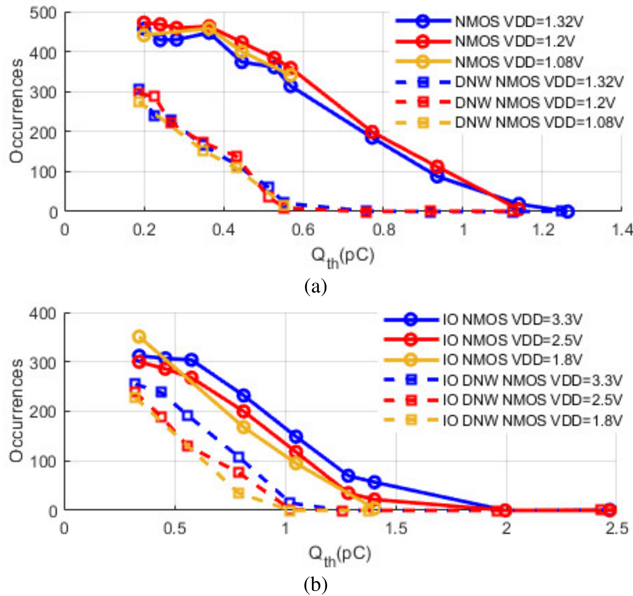

Fig. 10. Charge measurement versus different supply voltages: (a) Core victim devices with VDD = 1.08, 1.2, and 1.32 V and (b) IO victim devices with VDD = 1.8, 2.5, and 3.3 V.

collected charge compared with nMOS devices, which is consistent with the off-chip charge measurement in [17]. Additionally, the longer channel length devices feature a larger amount of collected charge.

2) IO Devices' Measurement Results: Three types of IO devices were also investigated in this test chip. The same method is used to calculate the unit device cross section and maximum collected charge which are shown in Fig. 9(a) and (b), respectively. The same trend can be found with the core devices. It is worth noting that the maximum collected charge for IO devices is larger than for core devices when both lengths are 500 nm. This can be explained by the bias voltage which is higher for IO devices. Consequentially, a thicker depletion region is formed because of higher reverse bias voltage. A larger fraction of the ionized charge will fall inside the depletion region and be collected [27].

3) Measurement Results With Different Supply Voltage: Different supply voltages were applied to both core and IO devices to characterize the supply voltage effects on SET ionization charge collection. A supply voltage of 1.08, 1.2, and 1.32 V was applied for core devices. Fig. 10(a) shows the results that the curves at different supplies are close to each other and there is no significant difference. For IO devices, results at the supply voltages of 1.8, 2.5, and 3.3 V are shown in Fig. 10(b). Except for the minimum Q_{th}, the occurrences of the same Q_{th} are higher for higher supply voltage. Additionally, the maximum collected charge also increased at higher supply voltage. This confirms the expectation that a higher supply voltage will cause more charge to be collected for the same transistor.

C. Pulse Duration Measurement Results

With the pulse duration measurement methodology, the duration distribution can be obtained directly from the readout.

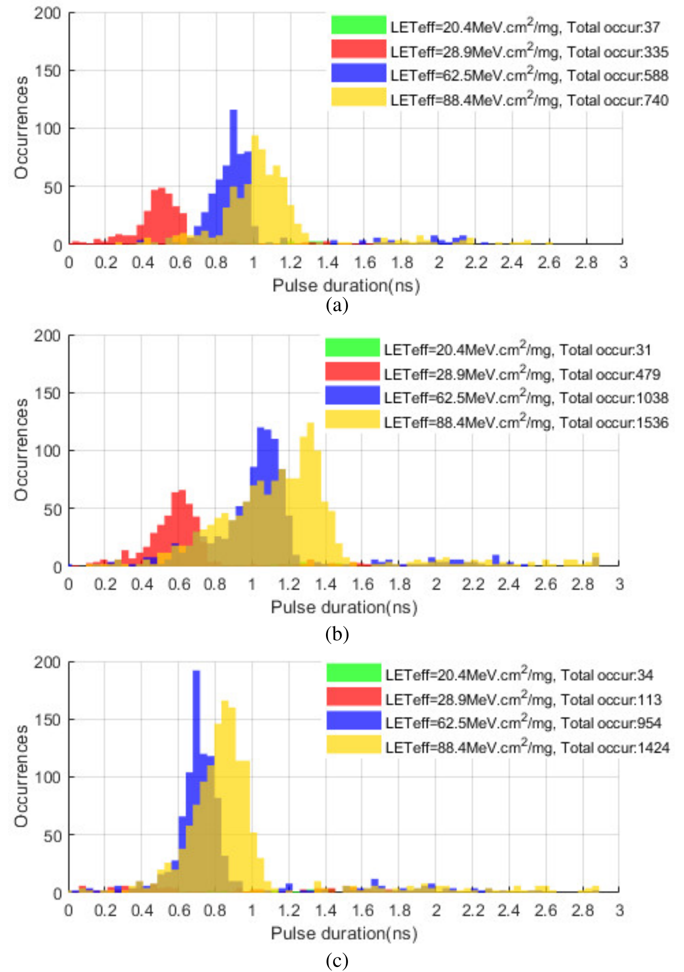

Fig. 11. Core nMOS pulse duration distribution with 1.2-V supply voltage: (a) core nMOS with 60-nm channel length, (b) core nMOS with 500-nm channel length, and (c) core DNW nMOS with 500-nm channel length.

The pulse duration measurement of all eight types of victim devices was explored under the same effective fluence $\text{Fluence}_{\text{eff}} = 6 \times 10^6$ ions/cm^2 and compared. However, transistors instead of resistors are used to bias the victim devices in pulse duration measurement. As a result, n-type and p-type victim devices have a different recovery current when SET happens. It is hard to make a fair duration comparison between n-type and p-type victim devices. Therefore, the duration measurement results are compared only within the same type of victim device.

1) Core Devices' Measurement Results: The SET pulse duration measurement results of core nMOS with channel lengths of 60 and 500 nm and core DNW nMOS with a channel length of 500 nm are shown in Fig. 11. One SET pulse measurement reading is considered as one occurrence. The y-axis indicates the number of occurrences at each pulse duration (x-axis). The total number of occurrences is also marked in the legend of each sub-figure in Fig. 11. Several common patterns can be found in all three sub-figures: First, when the effective LET $= 20.4$ MeV $\cdot$ cm^2/mg, the maximum voltage drop is not sufficient to trigger the amplifier and there is no clear distribution plot. Second, a higher effective

Authorized licensed use limited to: IMEC. Downloaded on August 03,2022 at 08:25:13 UTC from IEEE Xplore. Restrictions apply.

LET heavy ion can cause a higher most frequent duration, a wider duration distribution range, and the total number of occurrences. This is expected since a higher effective LET heavy ion can introduce more ionized charge into the circuit and causes a longer time to recover to the original voltage. Though most duration readout forms a bell-shaped distribution when effective LET $\geq$ 28.9 MeV $\cdot$ cm^2/mg, sporadic high duration events happened outside the bell shape. The reason for these high duration events is that double hits happened in one measurement period. The effect of the channel length on SET duration can be acquired by comparing Fig. 11(a) and (b). A longer channel can cause a longer duration since the total transistor area is increased. When the heavy ion hits the gate area, or even the source area, there will be some charge collected by the drain by diffusion. This result is consistent with the results from charge measurement. When DNW is applied to the n-type transistor [see Fig. 11(c)], the total number of occurrences is reduced for each effective LET. Besides, the most frequent duration and the distribution range are reduced. This can be explained from two points mentioned earlier in the section on the charge measurement results: the DNW collected part of the ionization charge through local p-well/DNW junction and isolates the charge below DNW keeping it from being collected [25], [26].

The duration measurement results of the core pMOS victim devices are shown in Fig. 12. The unit device cross section is derived (Occurrences/Fluence$_{\mathrm{eff}}$/No. Devices) and shown in Fig. 12(a). If the measurement results exhibit a bell-shaped distribution, the most frequent pulse duration (square in figure) and upper/lower boundary (horizontal bar in the figure) are plotted in Fig. 12(b). Similar duration trends can be found when the effective LET and channel length vary. It is noteworthy that compared with the unit device cross section results from ionization charge measurement in Fig. 8(a), duration measurement cross section results show the same magnitude but slightly lower values. This is explained by the fact that in the duration measurement circuit, the victim devices are widely distributed in M ($M > 100$) blocks and the boundary space of the victim devices in each block contributes more sensitive area.

2) IO Devices' Measurement Results: The SET pulse duration measurement results of IO devices are demonstrated in Fig. 13. From the pulse duration range in Fig. 13(b), the same trend but lower pulse duration can be found compared with the core devices measurement results. IO devices have a higher supply voltage. Thus, the recovering current is higher compared with the core devices with the same dimension. However, the unit device cross section results in Fig. 13(a) do not present consistency when compared with the unit device cross section results from charge measurement. When the effective LET $\geq$ 28.9 MeV $\cdot$ cm^2/mg, DNW devices show a larger unit device cross section compared with non-DNW devices. It indicates that the DNW makes the victim devices more sensitive at high effective LET situations in pulse duration measurements. The similar SET performance degradation caused by DNW was also reported in [28]. This phenomenon can be caused by the potential rise in the p-well followed by the injection of electrons into the p-well from the

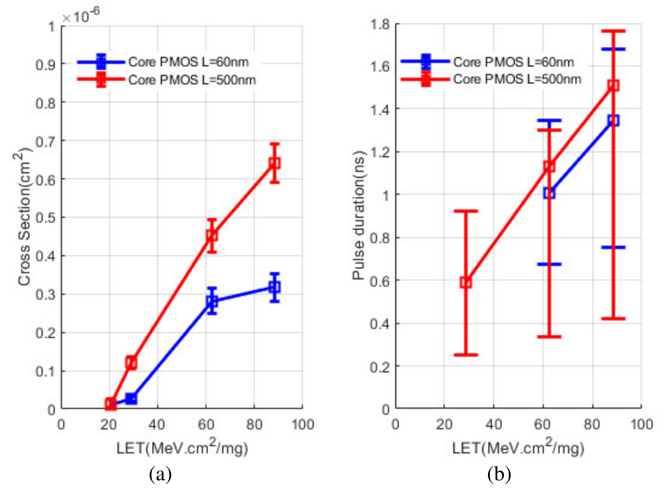

Fig. 12. Core pMOS duration measurement results with 1.2-V supply voltage: (a) unit device cross section and (b) pulse duration range.

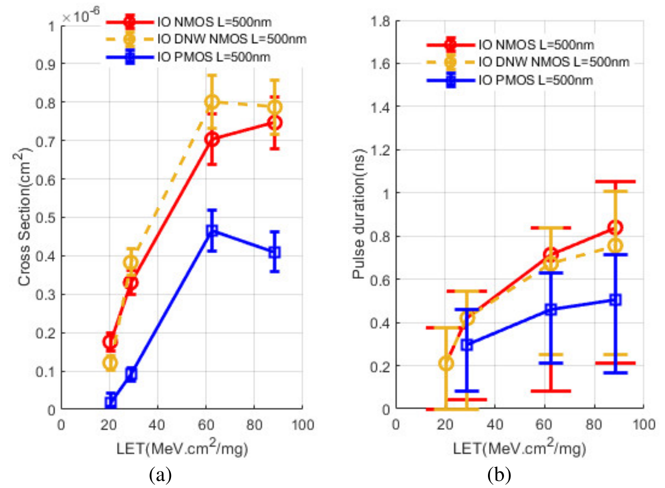

Fig. 13. IO nMOS and pMOS duration measurement results with 3.3-V supply voltage: (a) unit device cross section and (b) pulse duration range.

source [29]. When the ion strike happens on the DNW nMOS transistor, ionized electrons and holes will be generated in the local p-well. The deposited electrons will drift into the n-well and holes are left in the p-well. The accumulation of holes raises the potential of the local p-well [30]. If the local p-well parasitic capacitance is small, this raise of potential will finally cause the forward biasing of the source-p-well and injection of the electrons into the p-well. Though most of the injected electrons will be collected by DNW (negligible electric field between drain and p-well). Still, there will be some electrons that drift to the drain, extending the pulse duration [29]. In the charge measurement circuit, the measurement block contains N victim devices and they share one large local p-well. But for the duration measurement, only N/M ($M > 100$) devices share one small local p-well. The p-wells in the charge measurement circuits have a less potential raise when an SET happens. Therefore, DNW only presents the advantage of reducing charge collection for charge measurement.

3) Measurement Results With Different Supply Voltages: Different supply voltages were also applied during SET duration measurement. Since the results do not show a clear difference when applying a 1.08, 1.2, and 1.32 V supply

Authorized licensed use limited to: IMEC. Downloaded on August 03,2022 at 08:25:13 UTC from IEEE Xplore. Restrictions apply.

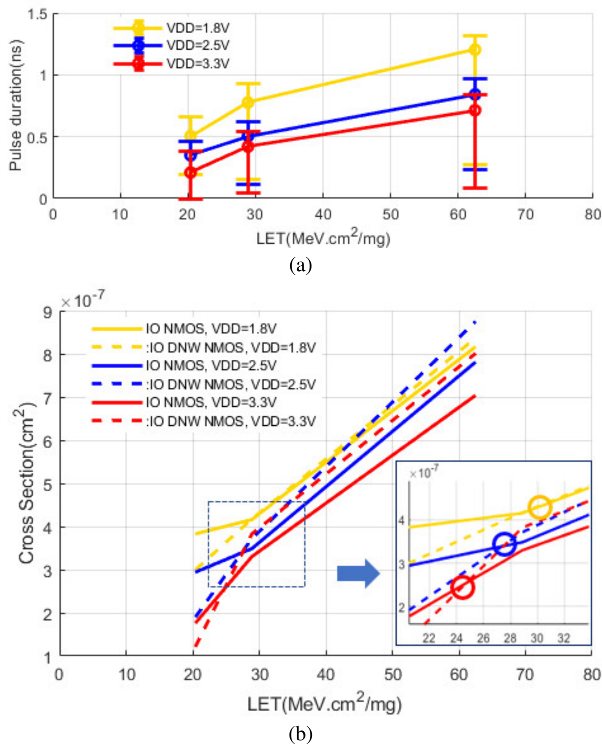

Fig. 14. IO nMOS duration measurement results at different supply voltages: (a) IO nMOS duration range and (b) IO nMOS and DNW nMOS unit device cross section.

voltage to core victim devices, only the SET duration of IO nMOS and the unit device cross section of IO nMOS and IO DNW nMOS are shown in Fig. 14. From Fig. 14(a), it can be seen that not only the most frequent duration value but also the distribution range are reduced when a higher supply voltage is applied. Although a higher supply voltage will cause a thicker reverse junction depletion region and more charge will be collected, the recovery current is also raised because of the higher supply voltage. As a result, the pulse duration is reduced at a higher supply voltage. A similar conclusion can be obtained from IO DNW nMOS and IO pMOS results. Similar to charge measurement, a lower unit device cross section can be found at a higher supply voltage in Fig. 14(b). It is worth noting that when comparing IO DNW and non-DNW nMOS unit device cross section results, the DNW only helps reduce the cross section at low effective LET since the forward biasing between the local p-well and the source will cause a longer pulse at high effective LET. It can also be seen that the unit device cross section intersection point of IO nMOS and IO DNW nMOS is also affected by the supply voltage. The intersection point moves to the low effective LET side when a higher supply voltage is applied. The reason is that when forward biasing is formed because of left holes, a higher supply voltage will cause a higher voltage difference between the source and the drain and more electrons will drift through the source-p-well-drain path.

IV. Conclusion

A 65-nm test chip for characterizing SET ionization charge and pulse duration has been designed and tested under a heavy-ion beam. The heavy-ion test results are very valuable to achieve an accurate SET current modeling for SET-related application design. In this chip, eight typical core and IO transistors are implemented as victim devices. The effects of DNW, channel length, and supply voltages are implemented and investigated. The measurement results indicate that pMOS transistors show less charge collection compared with nMOS transistors. DNW devices exhibit a lower total ionization charge collection compared with non-DNW devices. But in duration measurement results, the DNW reduces the pulse duration only at low LET situations. At high LET situations, the DNW can extend the pulse duration because of the local p-well-source forward biasing. Furthermore, the channel and source area of the devices should also be considered as the sensitive region owing to charge contribution of diffusion. At higher supply voltages, more charge can be collected, but the recovery current also increases at the same time. The pulse duration is reduced in the end.

Acknowledgment

The authors would like to thank their colleagues Bastien Vignon, Guillaume Pollissard, Geert Thys, Ben Delronge, and Qiuyang Lin for technical discussion and support.

References

[1] M. J. Gadlage *et al.*, "Single event transient pulse widths in digital microcircuits," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3285–3290, Dec. 2004.

[2] V. Ferlet-Cavrois, L. W. Massengill, and P. Gouker, "Single event transients in digital CMOS—A review," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 3, pp. 1767–1790, Jun. 2013.

[3] P. E. Dodd and L. W. Massengill, "Basic mechanisms and modeling of single-event upset in digital microelectronics," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 583–602, Jun. 2003.

[4] J. Wang, J. Prinzie, A. Coronetti, S. Thys, R. G. Alia, and P. Leroux, "Study of SEU sensitivity of SRAM-based radiation monitors in 65-nm CMOS," *IEEE Trans. Nucl. Sci.*, vol. 68, no. 5, pp. 913–920, May 2021.

[5] Q. Wu *et al.*, "Supply voltage dependence of heavy ion induced SEEs on 65 nm CMOS bulk SRAMs," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 4, pp. 1898–1904, Aug. 2015.

[6] J. M. Benedetto, P. H. Eaton, D. G. Mavis, M. Gadlage, and T. Turflinger, "Digital single event transient trends with technology node scaling," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3462–3465, Dec. 2006.

[7] R. C. Baumann, "Radiation-induced soft errors in advanced semiconductor technologies," *IEEE Trans. Device Mater. Rel.*, vol. 5, no. 3, pp. 305–316, Sep. 2005.

[8] S. Verhaegen, W. Sijbers, G. Pollissard, L. Bertil, G. Franciscatto, and G. Thys, "DARE SET simulation flow integrated in virtuoso ADE L/XL design environment," in *Proc. Int. Workshop Analogue Mixed-Signal Integr. Circuits Space Appl. (AMICSA)*, Leuven, Belgium, Jun. 2018, pp. 1–3. [Online]. Available: https://indico.esa.int/event/222/contributions/2110/attachments/1760/2056/AMICSA2018_DARESET SimulationEnvironment_Paperv2.pdf

[9] G. C. Messenger, "Collection of charge on junction nodes from ion tracks," *IEEE Trans. Nucl. Sci.*, vol. NS-29, no. 6, pp. 2024–2031, Dec. 1982.

[10] V. Ferlet-Cavrois *et al.*, "Direct measurement of transient pulses induced by laser and heavy ion irradiation in deca-nanometer devices," *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, pp. 2104–2113, Dec. 2005.

[11] V. Ferlet-Cavrois *et al.*, "New insights into single event transient propagation in chains of inverters—Evidence for propagation-induced pulse broadening," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2338–2346, Dec. 2007.

[12] P. Eaton *et al.*, "Single event transient pulsewidth measurements using a variable temporal latch technique," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3365–3368, Dec. 2004.

Authorized licensed use limited to: IMEC. Downloaded on August 03,2022 at 08:25:13 UTC from IEEE Xplore. Restrictions apply.

[13] J. A. Maharrey *et al.*, “Heavy-ion induced SETs in 32 nm SOI inverter chains,” in *Proc. IEEE Radiat. Effects Data Workshop (REDW)*, Boston, MA, USA, Jul. 2015, pp. 10–14.
[14] B. Narasimham *et al.*, “On-chip characterization of single-event transient pulse widths,” *IEEE Trans. Device Mater. Rel.*, vol. 6, no. 4, pp. 542–549, Dec. 2006.
[15] T. Makino *et al.*, “LET dependence of single event transient pulse-widths in SOI logic cell,” *IEEE Trans. Nucl. Sci.*, vol. 56, no. 1, pp. 202–207, Feb. 2009.
[16] T. D. Loveless *et al.*, “On-chip measurement of single-event transients in a 45 nm silicon-on-insulator technology,” *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 2748–2755, Dec. 2012.
[17] M. Glorieux *et al.*, “Detailed SET measurement and characterization of a 65 nm bulk technology,” *IEEE Trans. Nucl. Sci.*, vol. 64, no. 1, pp. 81–88, Jan. 2017.
[18] R. Harada, Y. Mitsuyama, M. Hashimoto, and T. Onoye, “Measurement circuits for acquiring SET pulsewidth distribution with sub-FO1-inverter-delay resolution,” in *Proc. 11th Int. Symp. Quality Electron. Design (ISQED)*, San Jose, CA, USA, Mar. 2010, pp. 839–844.
[19] J. Chen, J. Yu, P. Yu, B. Liang, and Y. Chi, “Characterization of the effect of pulse quenching on single-event transients in 65-nm twin-well and triple-well CMOS technologies,” *IEEE Trans. Device Mater. Rel.*, vol. 18, no. 1, pp. 12–17, Mar. 2018.
[20] M. J. Gadlage *et al.*, “Alpha-particle and focused-ion-beam-induced single-event transient measurements in a bulk 65-nm CMOS technology,” *IEEE Trans. Nucl. Sci.*, vol. 58, no. 3, pp. 1093–1097, Jun. 2011.
[21] Y. Chi *et al.*, “Characterization of single-event transient pulse broadening effect in 65 nm bulk inverter chains using heavy ion microbeam,” *IEEE Trans. Nucl. Sci.*, vol. 64, no. 1, pp. 119–124, Jan. 2017.
[22] B. Razavi, “Introduction to switched-capacitor circuits,” in *Design of Analog CMOS Integrated Circuits*. Boston, MA, USA: McGraw-Hill, 2000, ch. 12, pp. 439–443.
[23] Cyclotron Resource Centre, UCLouvain. *Parameters and Available Particles*. [Online]. Available: https://uclouvain.be/en/research-institutes/irmp/crc/parameters-and-available-particles.html
[24] P. E. Dodd *et al.*, “Impact of ion energy on single-event upset,” *IEEE Trans. Nucl. Sci.*, vol. 45, no. 6, pp. 2483–2491, Dec. 1998.
[25] H. Puchner, D. Radaelli, and A. Chatila, “Alpha-particle SEU performance of SRAM with triple well,” *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3525–3528, Dec. 2004.
[26] P. Roche and G. Gasiot, “Impacts of front-end and middle-end process modifications on terrestrial soft error rate,” *IEEE Trans. Device Mater. Rel.*, vol. 5, no. 3, pp. 382–396, Sep. 2005.
[27] G. Abadir, W. Fikry, H. Ragai, and O. Omar, “A device simulation and model verification of single event transients in $n^{+}-p$ junctions,” *IEEE Trans. Nucl. Sci.*, vol. 52, no. 5, pp. 1518–1523, Oct. 2005.
[28] G. Gasiot, D. Giot, and P. Roche, “Multiple cell upsets as the key contribution to the total SER of 65 nm CMOS SRAMs and its dependence on well engineering,” *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2468–2473, Dec. 2007.
[29] T. Roy, A. F. Witulski, R. D. Schrimpf, M. L. Alles, and L. W. Massengill, “Single event mechanisms in 90 nm triple-well CMOS devices,” *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 2948–2956, Dec. 2008.
[30] S. DasGupta *et al.*, “Effect of well and substrate potential modulation on single event pulse shape in deep submicron CMOS,” *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2407–2412, Dec. 2007.

Authorized licensed use limited to: IMEC. Downloaded on August 03,2022 at 08:25:13 UTC from IEEE Xplore. Restrictions apply.