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A 7-Bit 7-GHz Multiphase Interpolator-Based DPC for CDR Applications

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***Abstract*— This paper presents a 7-bit digital to phase converter (DPC) for high speed clock and data recovery (CDR) applications which is capable of generating multi-phase clocks at 7-GHz frequency. Fabricated in a standard 65-nm CMOS technology, the design introduces a modified phase interpolator (PI) and a quadrature phase corrector (QPC) to reduce the effect of the circuit imperfections on the DPC's resolution and linearity. Employing a 14-GHz quadrature reference clock, the DPC achieves DNL/INL of 0.7/6 LSB respectively while consuming 40.5 mW power from 1.05 V supply.**

***Index Terms*— Digital to phase converter (DPC), clock and data recovery (CDR), phase interpolator (PI), wireline and optical communication.**

I. Introduction

THE continuous demand for higher data rates pushes broadband wireline and optical communication systems toward the extensive use of multi-lane transceiver architectures [1], [2]. In such applications, the clock and data recovery (CDR) block requires multi-phase clocks with phase adjusting capability which if implemented digitally, can be realized by using digital to phase converters (DPCs [3]). Common DPC architectures use variable-delay cells or phase interpolators (PIs) [4] for the fine tuning of the output clock phases within the required accuracy. Although fine tuning stages based on the variable-delay cells offer lower differential nonlinearly (DNL) and integral nonlinearity (INL), the provided delay range is limited and not well-defined [5].

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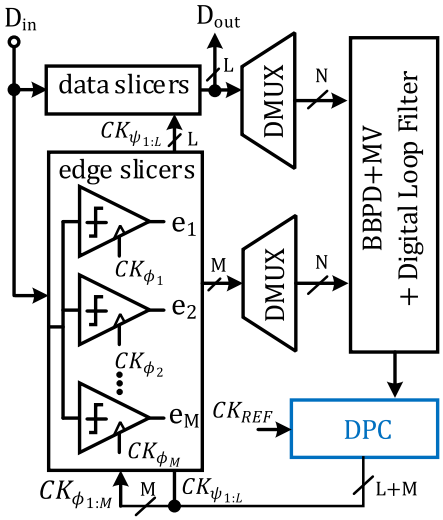

Fig. 1. Block diagram of a high speed DPC based CDR with interleaved input channels [1].

On the contrary, PIs inherently have a fixed delay range determined by the two inputs phase differences. However, the linearity is strongly restricted by the input phase differences and the PI's time constants which are the main sources of the DNL/INL degradation. Despite these drawbacks, the PI can operate efficiently at multi-GHz frequencies as it lends itself well to the current mode logic (CML) implementation. Furthermore, the semi-sinusoidal nature of the waveforms lessens the effect of the PI's time constants (compared to a square waveform) which improves the linearity [6]. The multi-phase requirement entails another issue; any mismatch within the DPC's output clock phases i.e. relative phase skew, can result in the non-uniform sampling of data transitions leading to more jitter generation in CDR. The main objective of this work is to systematically analyze these effects and present a multi-phase DPC circuit to mitigate them. Although our treatment of the subject targets DPC's usage in a certain category of high speed CDRs, the proposed techniques can be effective in other applications [7] as well.

II. DPC Modelling

Fig. 1 shows the general configuration of a DPC based CDR. To reach to the required speed the CDR incorporates

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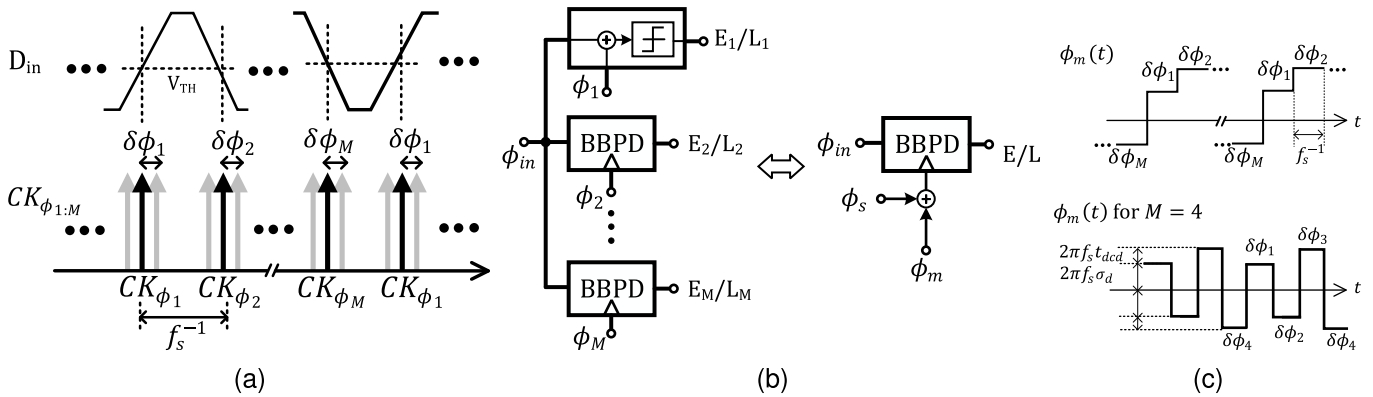

Fig. 2. (a) sampling of data transitions by edge slicers, the phase skew results in non-uniform sampling (b) modelling of parallel BBPDs operating at $f_{s/M}$ with a single PD block operating at f_s, addition of ϕ_m to the ideal sampling phase, ϕ_s, to account for the effect of phase skew between clock phases. ϕ_m waveform is periodic with minimum frequency of f_s/M (c) ϕ_m waveform used in our simulations ($M = 4$) and $f_s = 28$ GHz.

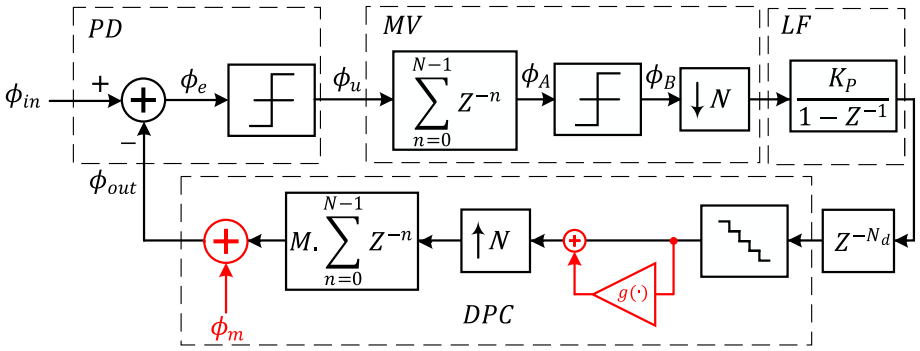

Fig. 3. CDR model and the non-idealities introduced by DPC.

a time interleaved analog front end and multi-phase sampling clocks. By performing bang-bang phase detection, the digital loop filter updates the DPC input code to align the clock and data. If the loop filter contains standard digital cells it is usually clocked at lower frequencies than the input samplers which demands further de-multiplexing. In this case the final phase detection result is generated using decimation via majority voting (MV) or boxcar filtering [8]. To study the effect of DPC nonlinearity and phase skew at the system level, we apply some modifications to the architecture of Fig. 1 and obtain a behavioral model for the CDR. As depicted in Fig. 2(a)−(b) the multi-phase array of PDs is replaced by a single channel PD operating at frequency of f_s.The skew in clock phases are modeled by the addition of phase error ϕ_m with minimum frequency of f_s/M wherein M is the number of input edge samplers. The amplitude of ϕ_m, represented by $\{\delta\phi_1, \delta\phi_2, \ldots, \delta\phi_M\}$ ensemble [Fig. 2(c)], depends on the delay variation due to the random mismatches in clock paths, σ_d, and also duty cycle distortion, t_{dcd}.

Fig. 3 illustrates the CDR's system level block diagram. The linear quantizer models the resolution of the DPC and the function in the parallel path takes into account the nonlinearity errors. The majority voting (MV) is performed by a moving average filter with a window length of N, followed by a quantizer [5]. The down-sampling block features the total de-multiplexing by factor of N in the loop.[1] The DPC's output operates at f_s while the input code is updated after every N cycles, to model the rate transition, an up-sampling block is combined with a moving average filter which insert $N-1$ input replica between the received values from the loop filter.[2] The gain of this filter, which is also M, represents a conversion factor since the DPC output and the input data sweep the phase with different frequencies. The DPC's jitter due to the reference clock is merged with the input, and can be neglected as in CDRs ϕ_{in} is usually the dominant source of jitter.

In our example we use the following set of design parameters based on the physical realization of a 28-Gbaud CDR in 65-nm CMOS with eight front-end sampling channels operating at 7 GS/s of which four are dedicated to edge samples ($M = 4$). The clock phases are running at 7 GHz controlled by a 7-bit DPC which also sets the clock frequency of the backend digital section to 1.75 GHz ($N = 16$). For the sake of simplicity in our analysis, only the proportional path gain, K_P, is being considered. The digital section requires

[1] Although the location of the PD and MV blocks w.r.t the de-multiplexer in the feedforward path is the reverse of what appears in the real implementation, from system level perspective it serves the same purpose.

[2] Unlike [9] here the whole CDR is modeled using discrete-in-time blocks so there is no need to apply zero-order-hold (ZOH) filtering for discrete mode to continues mode conversion.

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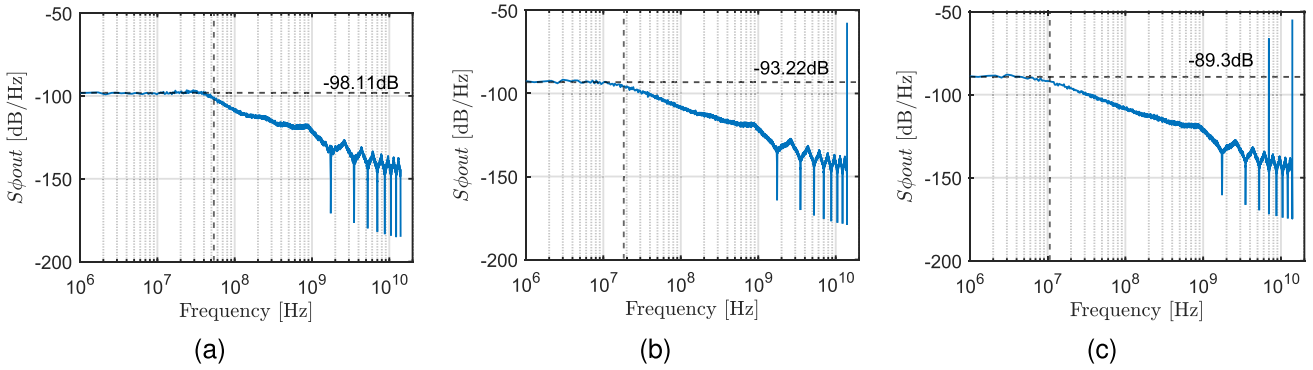

Fig. 4. ϕ_{out} power spectral density (a) $\sigma_d = 0$, $t_{dcd} = 0$ (b) $\sigma_d = 5$ ps, $t_{dcd} = 0$ thus one spur at 14 GHz (c) $\sigma_d = 5$ ps, $t_{dcd} = 0.025T_{CK}$ ($T_{CK} \approx$142 ps) resulting in additional spur at 7 GHz. Default parameters are $\sigma_{\phi_{in}} = 100$ mUI (-105 dB/Hz), $K_p = 5$ mUI and $N_d = 8$.

eight clock cycles to render a valid output therefore the imposed delay in the loop, N_d, is 8. As N_d is large, to avoid limit cycles, the update rate of the DPC's input is reduced by choosing low values for K_P in the form of redundant bits. Now we concentrate on two different scenarios in which the input jitter, ϕ_{in}, is a random white noise with Gaussian distribution:

a) *In the presence of only phase mismatches at the output of the DPC*, supposing that the random delay mismatches are uncorrelated, ϕ_m may be expressed by a periodic waveform as shown in Fig. 2 (c) where the adjacent levels take magnitude of $2\pi f_s \sigma_d$ with opposite signs to represent a worst-case condition. The DCD would cause additional deviations by affecting the differential clock phases and can be taken into account by relative shifting of the corresponding levels in ϕ_m with an amount equal to $2\pi f_s t_{dcd}$. In this case with $f_s = 28$ GHz, ϕ_m's spectrum contains tones at 7 GHz and its harmonics. As the spurs are out-of-band (nullified by the moving average's zero frequencies), the loop fails to correct for such errors hence the recovered sampling clock, f_s shows strong phase modulation which reduces the available sampling margin to meet certain bit error rates. Fig. 4 illustrates $S_{\phi_{out}}$, the spectral density of output phase, ϕ_{out}, for different ϕ_m values. In addition to the generation of out-of-band tones, the overall response at lower frequencies changes drastically. This happens because of the nonlinear nature of the bang-bang loop; ϕ_m minimizes the PD's sensitivity to the random components in ϕ_e and the combined gain of PD and MV, $K_{EFF} = K_{PD} \cdot K_{MV}$, drops as shown in Fig. 5. Consequently, the amount of generated jitter inside the loop increases so does the total output rms jitter, $\sigma_{\phi_{out}}$, due to the random components of ϕ_{out} [Fig. 5]. In Fig. 5 to extract K_{EFF} the following set of expressions from [9], [10] and [11] has been used in conjunction with the nonlinear simulation results:

$$K_{PD} = \frac{E[\phi_{e,N}(nT_s)\phi_u(nT_s)]}{E[\phi^2_{e,N}(nT_s)]}$$
$$K_{MV} = \frac{E[\phi_A(nT_s)\phi_B(nT_s)]}{E[\phi^2_A(nT_s)]} \quad (1)$$

wherein $T_s = f_s^{-1}$, $\phi_{e,N}$ represents the random jitter in ϕ_e while ϕ_u is the BBPD's output including random and deterministic jitters. ϕ_A and ϕ_B are the input and output of

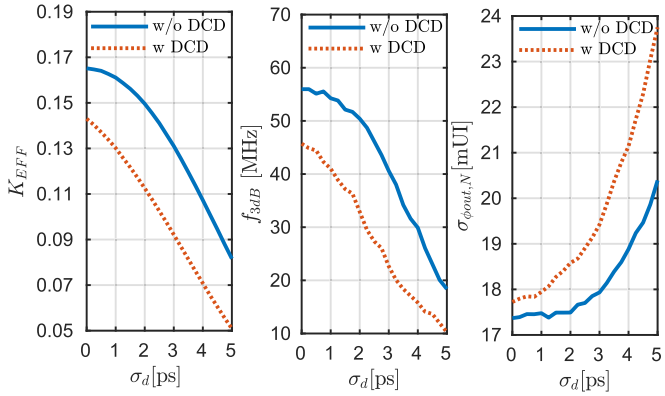

Fig. 5. Effective gain of PD and MV, the loop's jitter transmission bandwidth and output rms jitter (due to random components) vs σ_d with and without DCD ($t_{dcd} = 0.025T_{CK}$ and $T_{CK} \approx 142$ ps, other loop parameters are based on Fig. 4).

the MV's 1-bit quantizer, respectively. It should be noted that unlike ϕ_e which contains both random and deterministic values, ϕ_A is a pure random signal without spurs. This is expected since N/M is an integer and therefore, the spurs always coincide with the zero frequencies introduced by the moving average filter.

b) *In the presence of DPC nonlinearity*, g(·) can be expressed in the form of $g(x) = \epsilon x + INL(x)$, with ϵ representing the gain error. As ϵ is a linear error, it can simply be corrected by adjusting K_P therefore will be ignored here. We use an arbitrary INL profile[3] as depicted in Fig. 6(a). Having its argument received from the quantizer, $g(x)$ produces a non-uniform quantization noise which corresponds to the DNL error. By inserting or removing of the quantizer, we can readily differentiate the INL and DNL effects. Because of the loop's high pass response to DPC's noise, at low frequencies the DNL has little impact in comparison to the large jitter generated by the BBPD and MV blocks whereas at high frequencies it introduces excessive phase dithering, raising the noise floor, Fig. 6(b). Although the impact of the INL is suppressed by the large loop gain, it makes the loop dynamics be dependent

[3]The INL profile is based on equation (8) for a unit PI cell with $\phi = \pi/4$ and $\eta = 0.1$.

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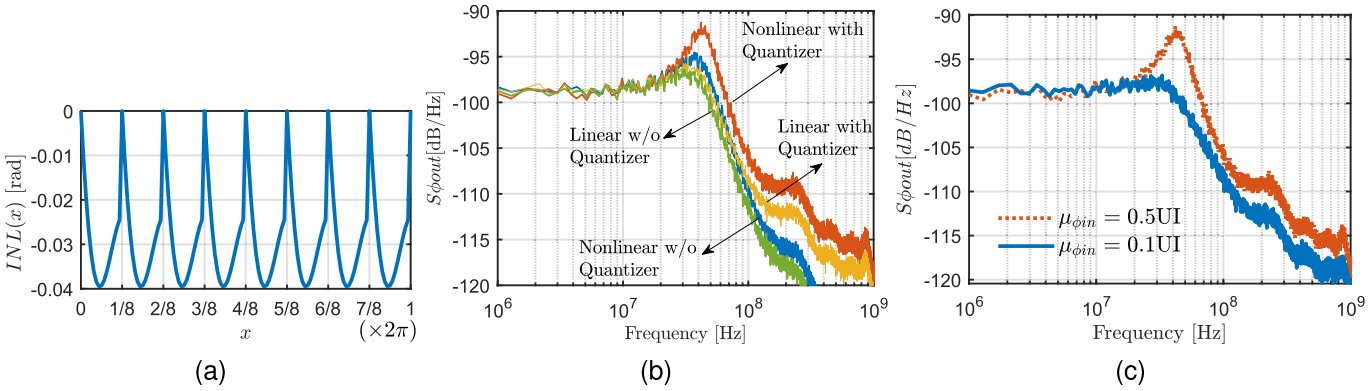

Fig. 6. (a) INL profile for DPC nonlinearity, (b) changes in ϕ_{out} spectral density due to the INL and DNL effects (by enabling/disabling the quantizer and nonlinearity block) (c) ϕ_{out} spectral density for $\mu_{\phi_{in}} = 0.1$UI and 0.5UI including INL and DNL effects. Default loop parameters are used.

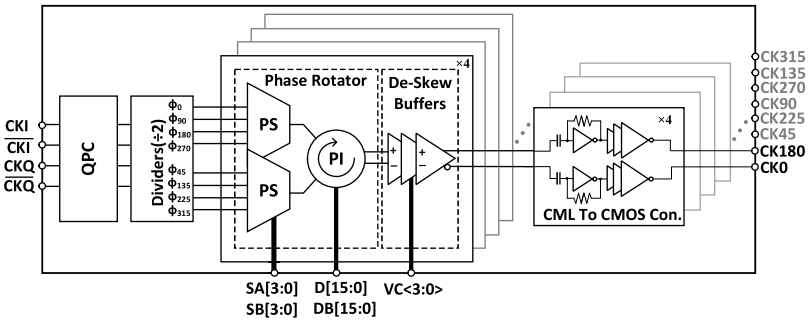

Fig. 7. DPC block diagram.

on static phase shifts in the input, $\mu_{\phi_{in}}$.[4] To explain this we note that since the loop is type one, the steady state error of a step input is zero i.e. $\mu_{\phi_{out}} = \mu_{\phi_{in}}$. To satisfy this constraint, the input of the $g(\cdot)$ block has to settle around a certain value, which alters the effective gain of the DPC as the input code varies, this phenomenon is shown in Fig. 6(c).

The above observations reveal how CDR dynamics deteriorate due to the non-idealities of a multi-phase DPC. In the following section we will investigate the source of the aforementioned imperfections and improve the performance by employing different techniques at circuit level.

III. DPC Architecture and Building Blocks

The DPC block diagram is shown in Fig. 7. It receives CKI, $\overline{CKI}$, CKQ and $\overline{CKQ}$ as the main references and outputs eight evenly spaced phases from $CK0$ to $CK315$ at half the input rate. The code inputs including SA, SB, D and DB control the phase shifting of the output clocks while the reference voltage, VC, is used for relative phase adjustments.

A. Phase Rotator (PR)

The PR block consists of two phase selectors (PS)s followed by a phase interpolator (PI). The PSs multiplex and output two adjacent clock phases, $V_\varphi (= V_{PS} e^{j\varphi})$ and $V_\psi (= V_{PS} e^{j\psi})$ based on the input code. Then the PI generates the clock phase, $V_\theta (= V_{PI} e^{j\theta})$, by using the weighted sum of the φ and ψ phases:

$$V_\theta = A_{PI} \cdot (\alpha \cdot V_\varphi + \beta \cdot V_\psi) \tag{2}$$

wherein A_{PI} is the PI's voltage gain and the normalized weights α and β are controlled by the digital input code. By assuming φ as the reference phase and $\phi = (\psi - \varphi)$, then the code to phase characteristic function of the PI can be quantified as:

$$\theta = \arctan\left(\frac{\beta \sin\phi}{\alpha + \beta \cos\phi}\right) \tag{3}$$

Ideally, θ should sweep the phase difference between the two inputs in uniform steps with $\theta_{LSB} = \phi / 2^{N_{PI}}$ in which N_{PI} is the PI's resolution.[5] The α and β parameters can be estimated using the inverse form of (3) similar to predistortion techniques, however this complicates the mapping of the digital codes to the weights. By allocating some margin for systematic errors, simpler functions like $\alpha + \beta = 1$, can be used to generate the weights. The resulted error has a code dependency which translates to nonlinearity in the PI's characteristic function. To improve the linearity, ϕ should be decreased which is limited by the number of available clock phases at the PR input. In our design, we use eight phases to cover the 360° phase rotation so $\phi = 45°$. For the PI section

[4]This scenario could be present during initial lock acquisition at start up or any momentary phase glitch, driving the CDR loop to correct for the offset created by the phase step at the input.

[5]To simplify the expression, we ignore the offset in θ caused by the frequency dependent phase shift from A_{PI}.

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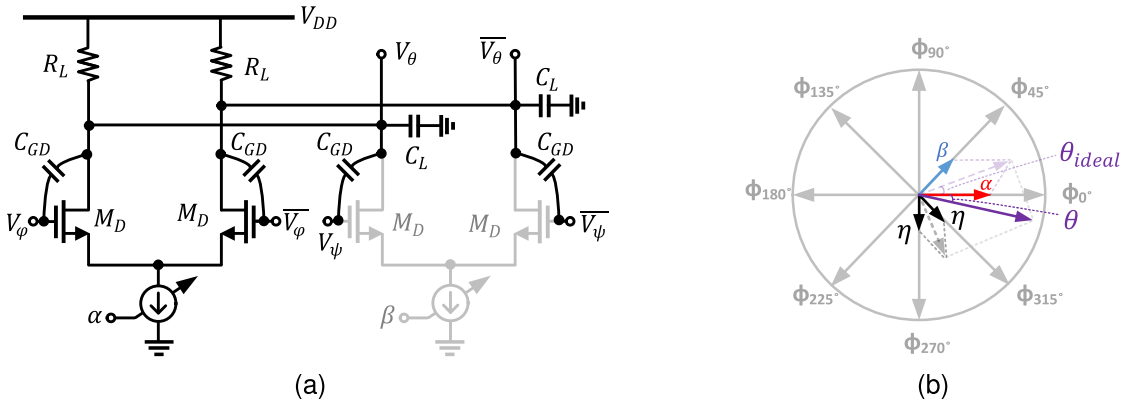

Fig. 8. (a) PI unit cell's circuit, clock feedthrough by means of C_{GD} results in limited range. (b) addition of $-j\eta$ to the interpolation coefficients to model the effect, the input phases are $\varphi = \phi_{0^\circ}$ and $\psi = \phi_{45^\circ}$.

$N_{PI} = 4$, which includes 16 steps with a nominal step size of approximately 2.8° and a maximum systematic error of 0.45°.

At multi gigahertz clock frequencies, f_{CK}, the weights α and β usually are implemented by using weighted current sources based on the current-steering topology and are merged with the input phases φ and ψ in a CML structure to synthesize (2). Due to the amplitude saturation in CML circuits, harmonics of φ and ψ must be considered in (2) which makes the phase linearity of the PI be dependent on the cell's output time constant τ_{out}. As explained in [12] to suppress such an effect, the input time spacing, $\phi/2\pi f_{CK}$, at most should be equal to τ_{out}. In other words:

$$\frac{\frac{\phi}{2\pi f_{CK}}}{\tau_{out}} \leq 1 \tag{4}$$

Since $\phi = \pi/4$ and assuming that $f_{BW} = 1/2\pi\tau_{out}$ then following can be derived:

$$f_{CK} \geq \frac{\pi}{4} f_{BW} \tag{5}$$

stating that the introduced nonlinearity subsides at higher f_{CK} as long as the harmonics fall beyond the circuit bandwidth, f_{BW}. Therefore, the circuit behavior can still be examined by considering only the fundamental tone. Referred as type-I, the most common CML based PI circuitry is shown in Fig. 8(a) which is a dual-input differential amplifier with a current steering DAC as the tail current source. Based on the input code the total amount of available current is divided between the two input pairs. Thermometer coding is preferred since it guarantees monotonicity in the presence of mismatch inside the unit cells and obviates phase glitches. Symmetrical loading is used to avoid any conversion of common mode noises, coupled from supply and substrate, into differential ones which results in excessive jitter [13]. The main disadvantage of the type-I is the large phase steps during boundary switching which arises from the phase feedthrough due to the gate-drain capacitance C_{GD} [14]. Through these capacitive paths some amount of input phases always appears at the output even though the associated weight is set to zero. This limits the available sweep range in every octant and can be referred as offsets in the main coefficients. By assuming $f_{CK}(=\omega_{CK}/2\pi)$ is close to f_{BW} and neglecting the higher order harmonics, (1) becomes:

$$\begin{aligned} V_\theta = {} & A_{PI}\cdot(\alpha + \frac{1}{A_{PI}}\cdot\frac{Z_L}{Z_L+Z_{GD}})\cdot V_\varphi \\ & + A_{PI}\cdot(\beta + \frac{1}{A_{PI}}\cdot\frac{Z_L}{Z_L+Z_{GD}})\cdot V_\psi \end{aligned} \tag{6}$$

wherein $Z_{GD} = 1/j\omega_{CK}C_{GD}$ and $Z_L = R_L \parallel (1/j\omega_{CK}(C_L + C_{GD}))$. Since $A_{PI} = -G_m(Z_L \parallel Z_{GD})$ represents the main path gain and G_m is the effective input pairs transconductance hence the offset terms become:

$$\frac{1}{A_{PI}}\cdot\frac{Z_L}{Z_L+Z_{GD}} = -\frac{1}{G_m Z_{GD}} = -j\frac{\omega_{CK}C_{GD}}{G_m} \tag{7}$$

which implies that the amount of introduced offset is inversely proportional to the ratio of feedthrough path admittance and the input pairs effective transconductance. Note that the offset terms are phasors leading α and β by 90° in phase resulting in excessive deviation of θ as shown in Fig. 8(b). Using (3) if $\eta = \omega_{CK}C_{GD}/G_m$ then:

$$\theta = \arctan\left(\frac{\beta\sin\phi - \eta(1+\cos\phi)}{\alpha + \beta\cos\phi + \eta\sin\phi}\right) \tag{8}$$

(8) indicates that θ's sweep range is smaller than ϕ which squeezes the octants at the PI's output. Consequently, the maximum phase step occurs at the boundaries where the octants are switching. Using equation (8) the gain error and INL/DNL of the PI is plotted for various values of α and η in Fig. 9. By ignoring the offsets in θ as η increases so does the amount of nonlinearly which is intensified at higher frequencies. A common solution is to isolate the input from the output as per the alternative architecture, type-II, which changes the order of the input transistors forming a cascode structure and removes the direct capacitive path between input and output. The type-II, however suffers from one main drawback: the code to phase characteristic is more nonlinear due to the strong dependency of the input capacitance to the codes [14].

Let us reconsider the architecture of the type-I PI, it appears that the offsets in (6) can be canceled by adding some negative terms. A feasible approach is to exploit the differential nature of the CML circuits. If the inputs and outputs of each differential pair are cross connected using capacitors,

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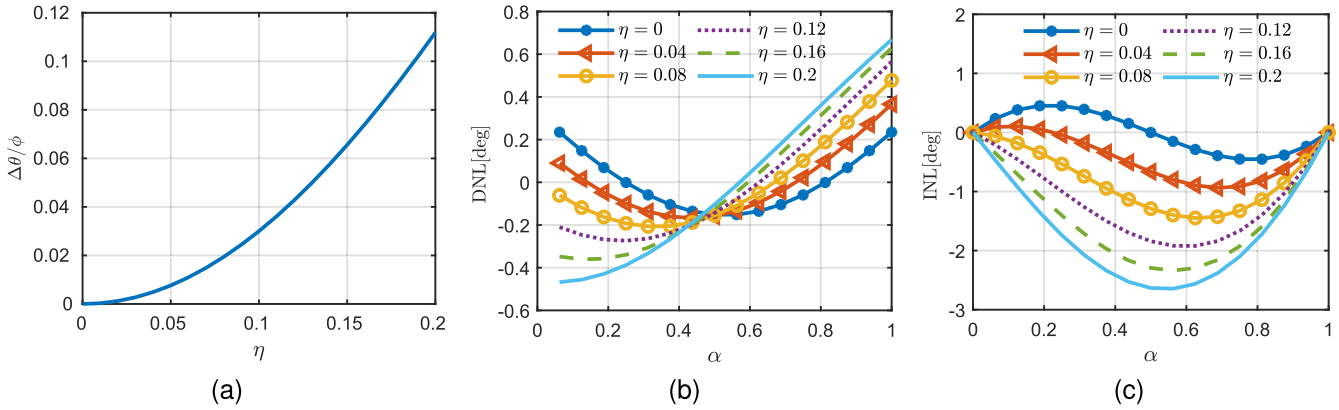

Fig. 9. The effect of clock feedthrough η on the (a) gain error, (b) DNL and (c) INL of a single PI cell based on equation (8) by assuming $\phi = \pi/4$.

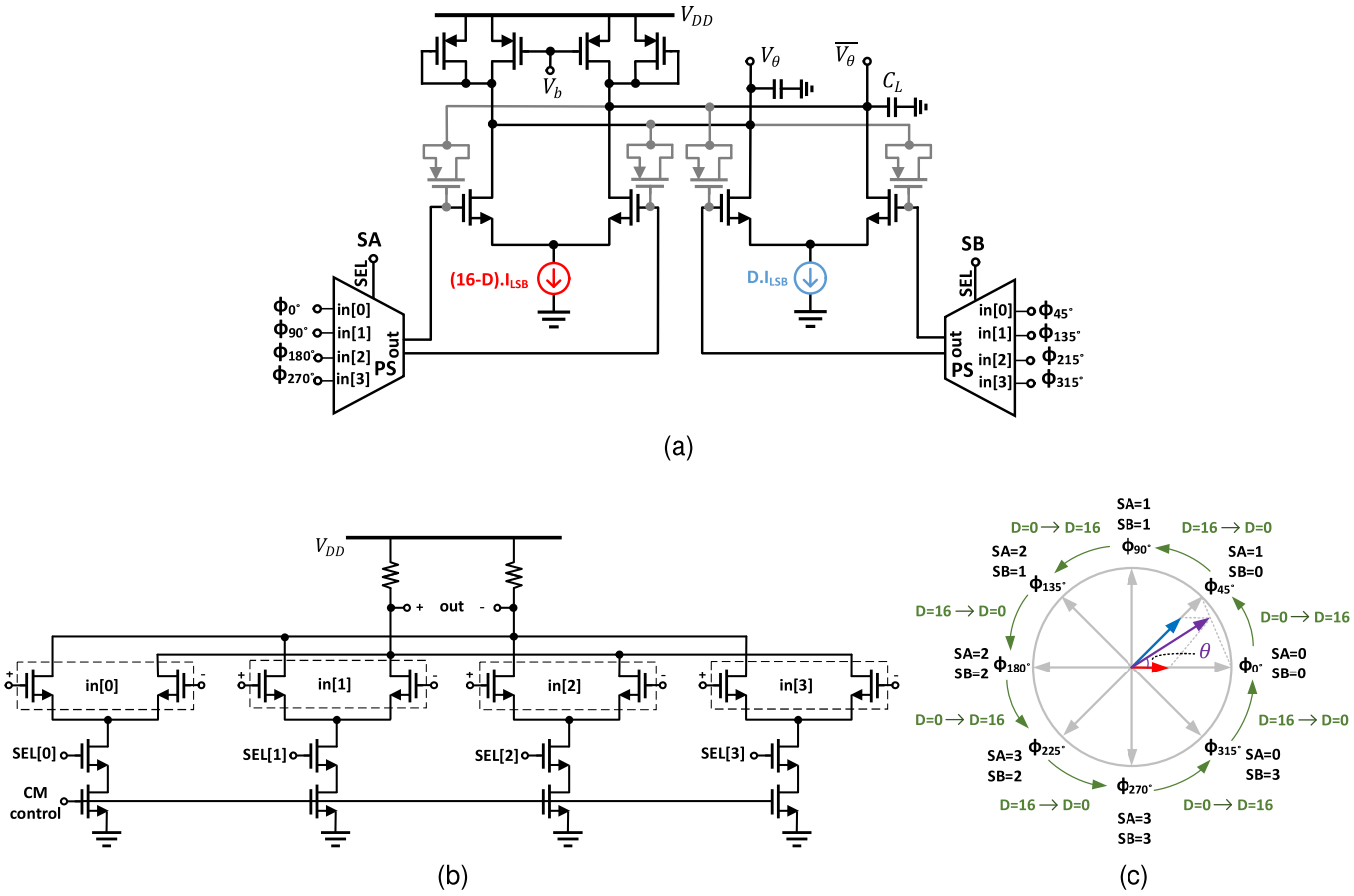

Fig. 10. (a) PR with the modified PI, (b) PS circuitry and (c) the logic sequence controlling PR's output phase.

as shown in Fig. 10(a) the circuit is able to suppress the phase feedthrough. Through performing transient simulations at transistor-level based on Fig. 10(a) with clock frequency of 7 GHz, $\Delta\theta = \theta_{max} - 45^\circ \approx 3.5^\circ$ is observed while under the same conditions in the modified circuit $\Delta\theta \approx 2.5^\circ$. It should be noted that during input clock crossings the displacement current due to the large capacitance of the tail current sources, causes further distortion of the output phase. Similar analysis can be carried out to model that effect but we skip over it here.

In Fig. 10(b) each PS circuit multiplexes eight inputs i.e. four differential clocks and selects the phase based on the input code. The circuit uses "1 of n" logic for the bits in SA and SB registers and the activated switches steer the current to the related differential pair. Asynchronous state changes in SA, SB, D and DB registers should be prevented since it would induce phase glitches.

Dynamic errors could still occur during boundary switching as it prompts momentary phase deviations in V_φ and V_ψ hence in V_θ. To decouple such phase disturbances from V_θ, the PR

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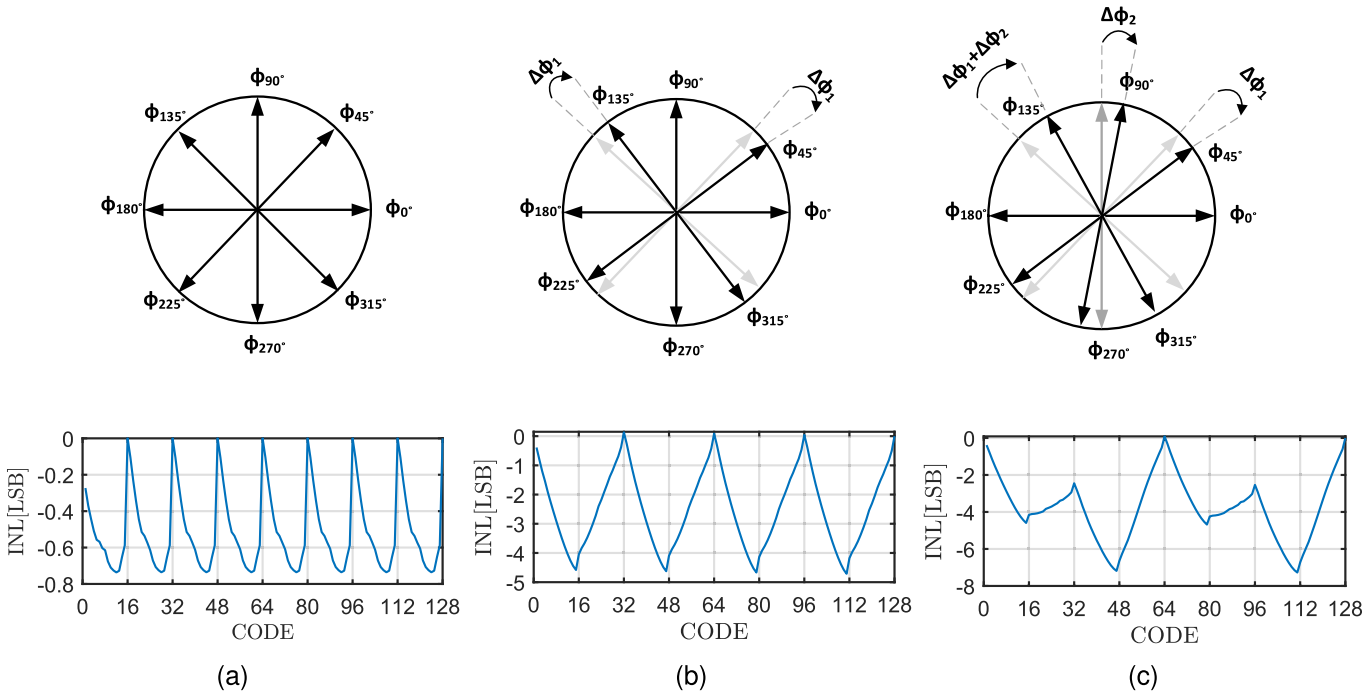

Fig. 11. PR's INL profiles from the transient simulation with (a) ideal input phase, (b) phase imbalance due to the I/Q mismatch $\Delta\phi_1 = 12.5°$ (@ 7 GHz) (c) phase imbalance due to the I/Q mismatch and duty cycle distortion resulted from preceding stages $\Delta\phi_1 = 12.5°$ and $\Delta\phi_2 = 6.25°$ (@ 7 GHz).

uses a decoder by which the simultaneous switching of V_φ and V_ψ is avoided. Instead of shifting V_φ and V_ψ by 45° during every octant traversing, only the phase associated with zero coefficient ($\alpha = 0$ or $\beta = 0$) is rotated by 90° while the other phase remains unchanged. To keep the phase rotation in the same direction, the coefficients register, D has to reverse the counting course in every boundary transition. The method is illustrated in Fig. 10(c).

The simulation results for the INL of the PR is shown in Fig. 11 (a). With the residual error of $\Delta\theta \approx 2.5°$ in the single PI cell, the gain error ($\Delta\theta/\phi$) with $\phi = 45°$ is 0.05. By looking for the corresponding η value (≈ 0.125) in Fig. 9(a) and using Fig. 9(c) the related maximum INL is roughly $-2°$. Since $\theta_{LSB} = 2.8°$ then the predicted maximum INL of $-0.71\,LSB$ is close to the simulation results in Fig.11 (a).

B. Quadrature Phase Corrector (QPC)

The PR uses eight clock phases which are generated by using divided-by-two version of the quadrature inputs. As (8) implies θ is dependent on ϕ and uneven octants in the PR's input cause deviation of ϕ from nominal value of 45°, which introduces discontinuity in octant boundaries and deteriorates the overall linearity of the PR. One of the main sources for this static error is the I/Q phase mismatch at the input reference [15]. For detailed evaluation of the effects, the transient simulation of PR is repeated by assuming that $\Delta\phi_1$ represents the input I/Q phase mismatch as shown in the phasor diagram of the Fig. 11(b). It should be noted that since the reference signals are passing through the dividers, the input I/Q phase mismatch manifests itself as the relative rotation of the two phasor sets of $\{\phi_{0°}, \phi_{90°}, \phi_{180°}, \phi_{270°}\}$ and $\{\phi_{45°}, \phi_{135°}, \phi_{225°}, \phi_{315°}\}$ at PR input. The resulted INL is plotted for $\Delta\phi_1 = 12.5°$(5 ps @ 7 GHz). In addition to I/Q phase mismatch, duty cycle distortion (DCD) may shift the phases inside each of the phasor sets by $\Delta\phi_2$ as illustrated in Fig.11(c) leading to further degradation in the linearity. For this case, the INL profile is computed with $\Delta\phi_1 = 12.5°$ and $\Delta\phi_2 = 6.25°$. To reduce the impact of I/Q phase mismatch, a simple quadrature phase corrector (QPC) with a new approach is presented.

The phasor diagram in Fig.12(a) describes the method. By considering V_{Iin} as the reference phasor, we let the phase of V_{Qin}, ϕ_{IQin}, deviate from its ideal value, 90°, by an amount of ϕ_{err}. The QPC should generate quadrature signals with the phase of ϕ_{IQout} being independent of ϕ_{err}. We surmise that simultaneous rotation of the related I/Q phasors at the output with respect to ϕ_{err} may correct such error. This functionality can be implemented by blending the phases akin to performing phase interpolation with equal weights. Applying this concept in every quadrant results in a new I/Q constellation composed of V_{Iout} and V_{Qout}. As shown in Fig. 12(a) any presence of ϕ_{err} pulls both V_{Iout} and V_{Qout} the same direction hence keeping ϕ_{IQout} undisturbed. The relation between ϕ_{IQout} and ϕ_{err} becomes:

$$\begin{aligned}\phi_{IQout} &= \pi - \arctan\left(\frac{k\cos\phi_{err}}{1 + k\sin\phi_{err}}\right) \\ &\quad - \arctan\left(\frac{k\cos\phi_{err}}{1 - k\sin\phi_{err}}\right) \\ &= \pi - \arctan\left(\frac{k\cos\phi_{err}}{1 - k^2}\right) \end{aligned} \tag{9}$$

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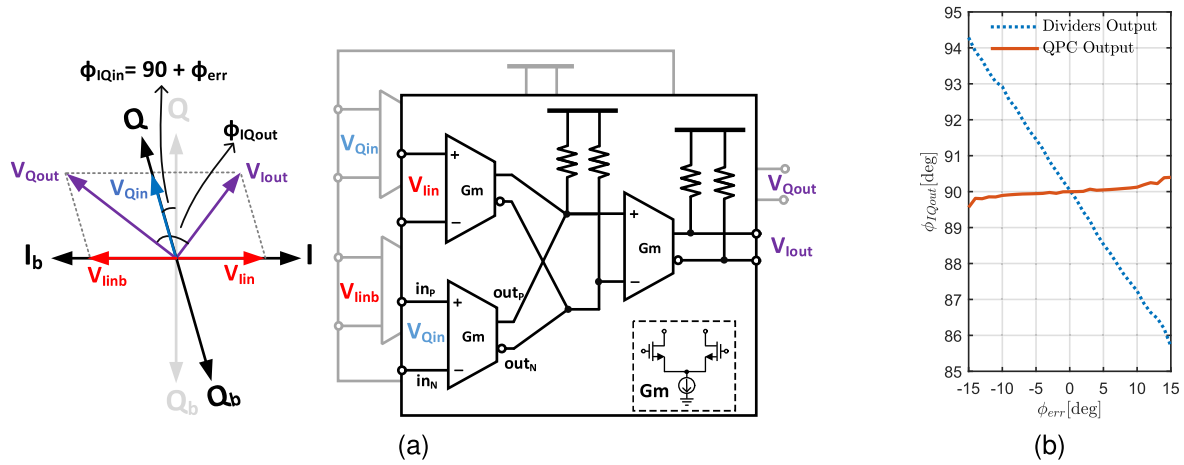

Fig. 12. (a) Phasor diagram and schematic of the QPC. (b) Transient simulation shows the phase at the output of QPC and dividers vs the amount of input's I/Q mismatch.

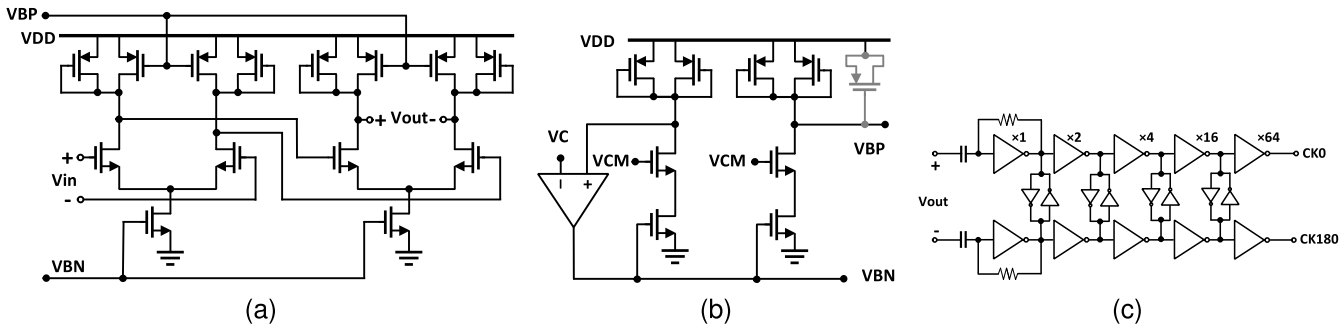

Fig. 13. (a) de-skew buffers, (b) delay controlling circuit and (c) CML to CMOS converter.

where $k = |V_{Qin}|/|V_{Iin}|$. If $k = 1$, then $\phi_{IQout} = 90°$, regardless of ϕ_{err} value, meaning that the full desensitization is achieved. This is also evident from Fig. 12(a) since $V_{Iinb} = -V_{Iin}$, then V_{Iout} and V_{Qout} resemble the result of addition and subtraction of two vectors (with equal magnitude and an arbitrary angle) which are always perpendicular.

The circuit featuring the QPC is shown in Fig. 12(a). The amplitude difference between V_{Iout} and V_{Qout} can influence the subsequent phase interpolation however the dividers preceding the PR restore the amplitudes to the same level.

Based on simulations [Fig. 12(b)] the QPC operation follows the predictions made by (8) though the main limitation comes from the output phase sensitivity to the input swings in the dividers as the amplitude difference between V_{Iout} and V_{Qout} can reach to 16%. Despite this drawback the combination is still capable of attenuating the input phase imbalance.

As (9) suggests, any deviation of k from its ideal value due to the amplitude mismatch between V_{Iin} and V_{Qin} could result in additional phase errors in ϕ_{IQout}.Validated by simulations, $\pm 5\%$ variations in k, offsets the ϕ_{IQout} curve by an amount less than $\pm 3°$. In addition the degradation on the reduced sensitivity of ϕ_{IQout} to ϕ_{err} is negligible with the maximum 1° change in ϕ_{IQout} while ϕ_{err} spanning the range of $\pm 15°$.

The architecture of the QPC indicates that its operation is susceptible to random mismatches. According to Monte Carlo simulations, the standard deviation of ϕ_{IQout} is approximately 4°. Although equipping the QPC with a trimming circuitry could improve the performance, such feature was not considered in this version of the design.

C. De-Skew Buffers and CML to CMOS Converters

To generate rail to rail clocks, CML to CMOS converters have been added to the design as shown in Fig. 13. The CML output DC voltages are removed by the AC coupling capacitors; the CM level is redefined through the feedback resistors and biasing of the first inverters at trip points (self-biased inverters). The following chains of four inverters buffer up the clock signals to gain the required driving strength. Any unequal rise and fall times can shift the clock crossings from the midpoint which can cause DCD. To avoid this DCD, cross coupled inverter pairs are inserted between the two single-ended sides of the differential phases [16]. Altogether the four PR blocks provide eight clock phases with a phase spacing of 45°. Any mismatch can cause phase misalignment at the output. To compensate the skew, buffers are implemented in the form of variable delay lines consisting of two differential stages, hence the independent trimming of the delays in each PR stage can be used to de-skew the relative phase mismatch between the four clock phases.

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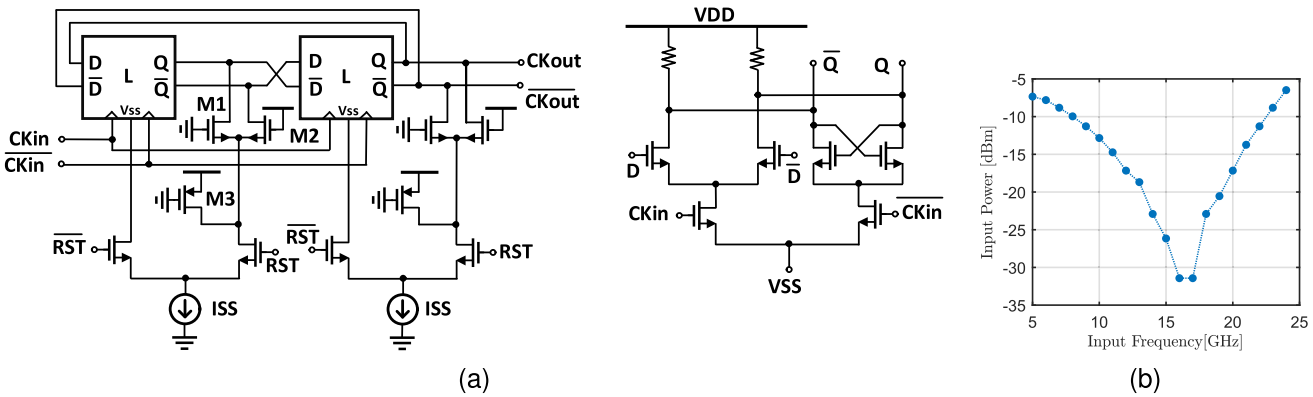

Fig. 14. (a) frequency divider with synchronous reset and (b) the simulated sensitivity curve.

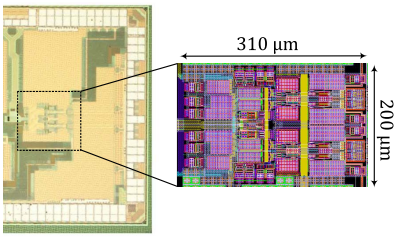

Fig. 15. DPC chip micrograph.

D. Dividers

To generate the eight clock phases ($\phi_{0^\circ}, \phi_{45^\circ}, \cdots, \phi_{315^\circ}$), differential quadrature inputs with the frequency of $f_{REF} = 2f_{CK}$, are fed to divide-by-two frequency dividers. The frequency divider architecture is based on the static frequency divider in which a single flip-flop, in the form of master-slave CML D latches, is inserted in a negative feedback loop. One of the main requirements for the dividers in this design, is to generate a true phase sequence at the output. If the node voltages inside the divider are not defined properly at startup, the divider output can fall out of phase by 180°. Applying a synchronous resetting mechanism guarantees the proper ordering of the output phases. This is accomplished by using resettable CML latches as shown in Fig.14(a) in which RST initializes the outputs of the master and slave latches with opposite high ($\approx V_{DD}$) and low ($\approx V_{DD} - V_{swing}$) voltage values. Dummy transistor M_1 is added to keep the output nodes balanced. Small sizes for M_1 and M_2 are chosen to avoid extra loading at the output which, with large V_{GS}, can lower the output voltage available for the tail current source I_{SS} during reset operation. For this reason, M_3 is used to source extra current, keeping enough voltage headroom. The simulated sensitivity curve for the dividers is plotted in Fig.14(b).

IV. Experimental Results

The DPC has been fabricated in 65-nm CMOS technology, Fig. 15. The active area is 0.062 mm^2 and the chip is mounted directly on a printed circuit board (PCB) using die-on-board wire-bonding. The test setup is shown in Fig. 16. The IQ signal generated by applying a single phase clock at 14 GHz to the quadrature hybrid which is followed by the delay lines (DLs) to output differential signals. Fig. 17 illustrates the output phase range when the codes are shifted from 16 to 32.

To measure the small time steps with high sensitivity a frequency domain method based on the phase modulation of the clock edges with a periodic signal is used [17]. In the output spectrum, the power of the first spur relative to the carrier, SCR [in dBc], is proportional to the amount of delay t_d added to the clock. The relation between t_d and SCR can be described as:

$$t_d = \frac{T_{CK}}{2} 10^{\mathrm{SCR}/20} \tag{10}$$

SCR is measured as the control signal is pulsed between CODE[n] and CODE[n+1] then the code is incremented to CODE[n+1] and is pulsed between CODE[n+1] and CODE[n+2]. The task is repeated for 128 consecutive codes. The observed errors during measurement, like uncertainty in sideband readings, are well below the accuracy threshold for the DNL measurement, however as the INL computation is based on the cumulative sum of the DNL samples, then the resulted errors can be perceptible, leading to systematic gain error in the DPC's code to phase transfer. To evade this issue, we consider that the DPC incurs no gain error after shifting by 128 codes as it outputs the same phase i.e. the outputs for CODE[0] and CODE[128] are exactly one clock period apart.[6] In addition, the introduced errors are independent of the input codes hence the average error can be extracted from the measured time steps for the sequence of 128+1 consecutive codes. By using this method, the induced gain error is removed and the INL can be calculated using:

$$\mathrm{INL[n]} = \sum_{n=1}^{128} (\mathrm{DNL[n]} - \overline{\mathrm{DNL}}) \tag{11}$$

wherein $\overline{\mathrm{DNL}}$ is the mean of DNL profile over 129 codes.

Normalized DNL and INL are plotted in Fig. 18 for different input frequencies indicating wide frequency range

[6]Depending on the equipment, the overall measurement time must be kept short to avoid errors associated with low frequency phase drifts of the input reference clock.

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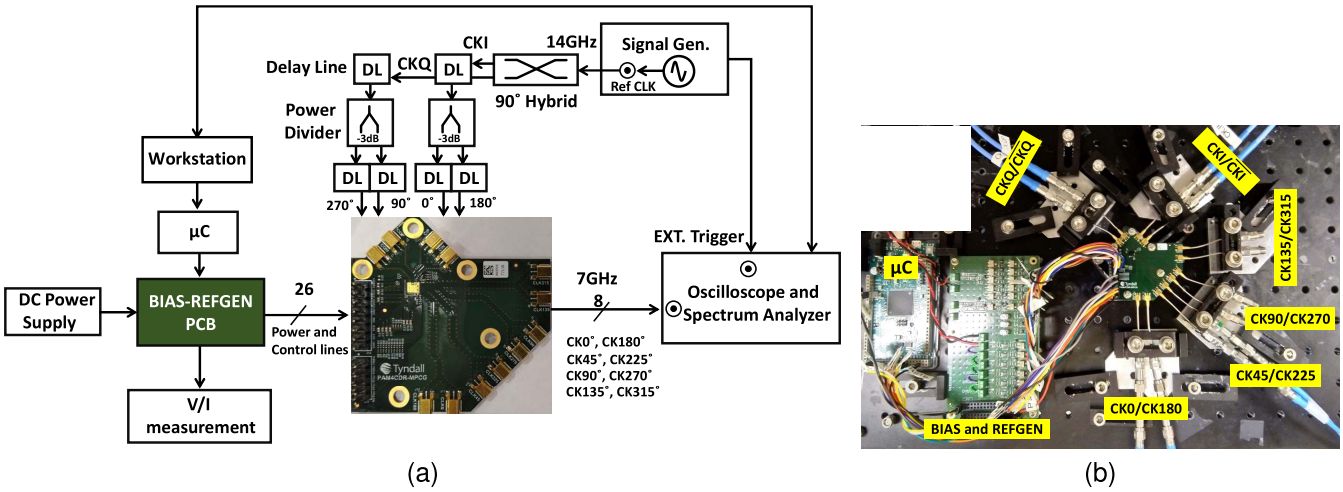

Fig. 16. (a) block diagram and (b) view of the test setup.

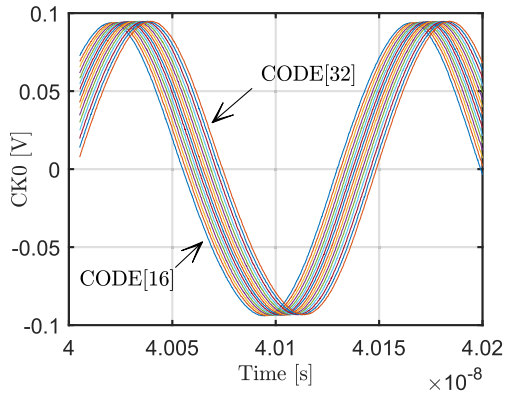

Fig. 17. Measured CK0 output (taken from the high speed CML PAD drivers) as the code shifted from 16 to 32 covering one octant.

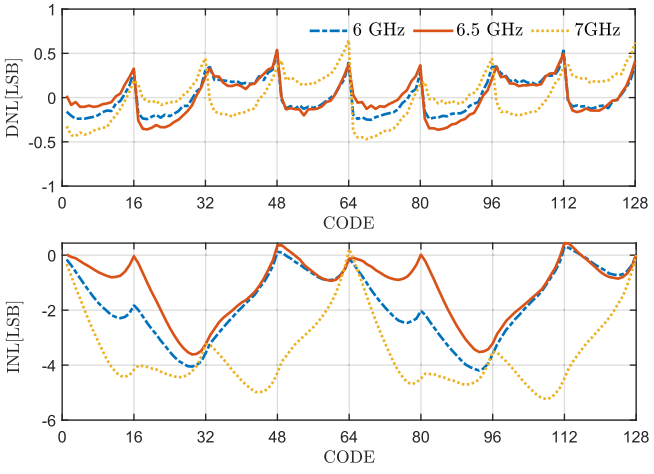

Fig. 18. Measured DNL and INL profiles for CK0 at different output frequencies ($1LSB = T_{CK}/128$).

of operation. The INL and DNL profiles for the four output clock phases at the design frequency of 7 GHz are illustrated in Fig. 19. In all the measurements the output of CODE[0] is considered to be the reference phase. Comparing

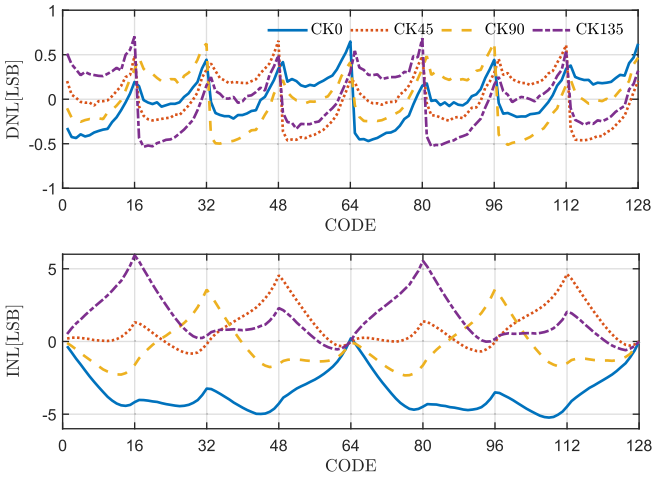

Fig. 19. Measured DNL and INL for the output phases at the targeted design frequency of 7 GHz ($1LSB \approx 1.1$ ps).

the results with the prediction made by the simulation in Fig. 11 reveals that the input to the PR core suffers from phase mismatches due to the residual I/Q imbalances and duty cycle distortion introduced by the preceding blocks especially the dividers.

With no direct access to the output of the QPC block, an indirect approach is employed to measure the I/Q phase mismatch tolerance. The testing is based on the amount of change in the output phase shift with respect to the deliberate phase imbalance at the input while the code is swept one octant, for instance, from CODE[0] to CODE[16] and it is equivalent to the vertical shift in the INL of CODE[16]. The results are shown in Fig. 20 for ±10 ps time mismatch around the nominal I/Q value. The associated change in the INL is 6.4 ps, corresponding to approximately 70% of attenuation.

The de-skew buffers can provide delay ranges of 40 ps at the frequency of 7 GHz as the controlling voltage, VC, varies from 0.3 V to 0.7 V (see Fig. 21.) The amount of RMS jitter

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TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR ART

	This work	[5]	[6]	[18]	[19]	[20]	[21]
CMOS Technology	65nm	28nm	65nm	28 nm	65nm	65nm	28nm FDSOI
Supply	1.05 V	1.1 V	1.2 V	1 V	1.2 V	1.2 V	1.2 V
Frequency	6 -7 GHz	2 GHz	0.5-1.5 GHz	0.3 GHz	10 GHz	5-8 GHz	2-11 GHz
Resolution	7 bits	11 bits	8 bits	10 bits	7 bits	7 bits	7 bits
DNL	0.7 LSB	1.25 LSB	0.52 LSB	-	0.3 LSB*	0.77 LSB	0.5 LSB
INL	6 LSB	4.9 LSB	1.33 LSB	1.86 LSB	3 LSB*	1.76 LSB	1.1 LSB
Multi-phase output (#)**	Yes (8)	No	No	No	Yes (4)	Yes (2)	Yes (8)
Output phase de-skew	✓	×	×	×	×	×	×
Power consumption	40.5 mW	19.8 mW	4.3mW	11.06 mW	N/A	22.95 mW	< 33.6 mW
Active Area	0.062 mm^2	0.009 mm^2	0.06 mm^2	0.047 mm^2	N/A	0.0426 mm^2	0.028 mm^2

*only simulation results are provided for the phase rotator section.
** power consumption is directly proportional to the number of output phases.

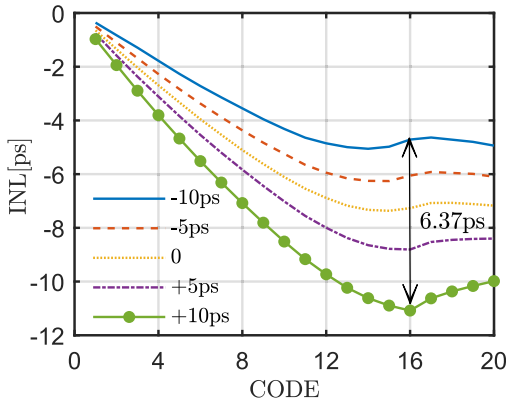

Fig. 20. The QPC performance is tested by addition of intentional mismatches at the input while looking at the INL shifts at CODE=16.

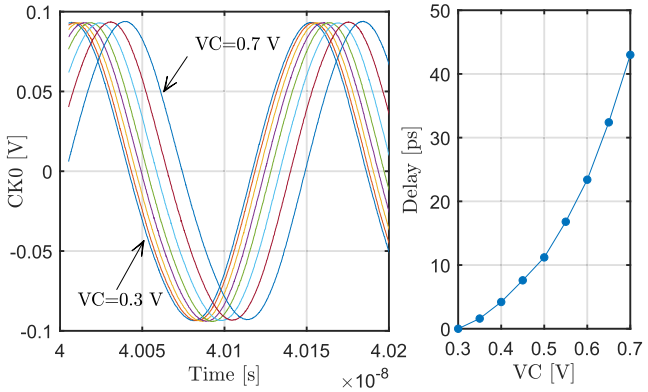

Fig. 21. Adjusting the phase of CK0 using controlling voltage VC, the resulted delay shows the wide de-skewing range of the output buffers.

at the input and output of the circuit is 200 fs and 600 fs, respectively. With the output jitter demonstrating Gaussian distribution, the jitter contribution of the block is around 565 fs. Using a spectrum analyzer the dividers output self-oscillation frequency was measured to be approximately 6 GHz.

At 14-GHz input frequency, the DPC consumes 161 mW power of which 81 mW is drawn by the main core and the rest by the output drivers from 1.05 V and 1.2 V voltage supplies

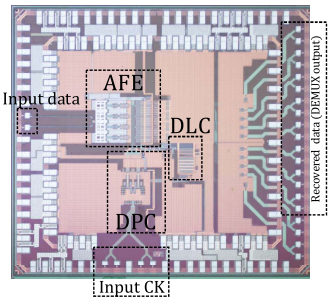

Fig. 22. CDR die micrograph incorporating the DPC (active area = 0.67 mm^2).

respectively. The CML to CMOS converter contributes 50% to the core power consumption since this circuitry is not part of the main DPC's function, the actual DPC block power dissipation is around 40.5 mW. Table I summarizes the performance of the DPC and compares it with that of prior art. The power consumption is higher in comparison with [5], [6] and [18] mainly due to the operating frequency and the number of the output phases. In terms of linearity, although the DPC's may not demonstrate favorable INL, the achieved DNL is within the fine range. [19], [20] and [21] feature higher clock frequencies, while the last one benefits from more advanced CMOS technology the first two provide less number of outputs. Furthermore, the proposed DPC, offers timing de-skew, allowing relative adjustment of the output phases.

V. APPLICATION TO CDR

The presented stand-alone DPC has been incorporated in implementing a high speed CDR as the back-end part of an optical receiver which is fabricated in 65-nm CMOS technology as shown in Fig. 22 with the active area of 0.67 mm^2. The CDR architecture is based on Fig. 1 in which the analog front end (AFE) is sampling the input data by means of the clock phases provided by the DPC. The digital loop controller (DLC) encompassing all the PD, MV, LF and decoder blocks adjusts the clock phases through the DPC input code. Although the CDR is mainly designed to

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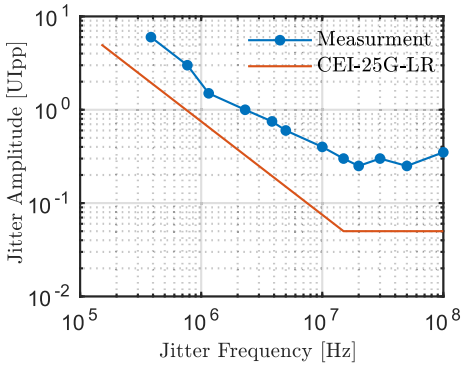

Fig. 23. Measured JTOL of the CDR.

operate with a pules-amplitude-modulation (PAM4) input, for the purpose of this paper we have only included the test results for NRZ data. The measured jitter tolerance (JTOL) for the CDR is depicted in Fig. 23 while only the proportional path gain with $K_P \approx 16$ mUI is activated. The input data rate was limited by the measurement equipment, hence the test was performed with a 25-GBd PRBS7 pattern and by setting the DPC's reference clock to 12.5 GHz. As it shown, the CDR's 1-UI JTOL bandwidth is around 2 MHz meeting the requirements of the jitter tolerance mask specified by CEI-25G-LR.

VI. Conclusion

A high speed DPC for the CDR application has been presented. By employing a systematic approach, the effects of the main imperfections such as phase skew and nonlinearity were analyzed. Then, to ameliorate those non-idealities, different circuit techniques were invoked. Using a fabricated chip in 65-nm CMOS technology the effectiveness of the methods has been investigated and the DPC demonstrates DNL/INL of 0.7 LSB/6 LSB while it is providing 8 clock phases at 7 GHz frequency and dissipating 40.5 mW of power from a 1.05 V supply.

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