ESD HBM Discharge Model in RF GaN-on-Si (MIS)HEMTs

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***Abstract*— Gallium nitride (GaN) technologies have become an essential role in commercial advanced RF systems, which accompany emerging RF electrostatic discharge (ESD) reliability challenges. As opposed to ESD clamp transistors in *LV* CMOS technologies, a mis-correlation between standard-defined human body model (HBM) ESD robustness and commonly used TLP failure current was observed in GaN (MIS) high electron mobility transistors (HEMTs). Using transient HBM *I–V* characteristics, a novel discharge model is proposed to explain the transient discharge mechanism. The TCAD and SPICE simulations confirmed that the observed mis-correlation between TLP and HBM is attributed to 2-dimensional electron gas (2DEG) resistance modulation in response to HBM ESD transient voltage waveforms. The HBM waveforms under full transient duration in terms of rising and falling edges are further discussed. Eventually, the failure mechanisms in the TLP IVs and the HBM transient IVs can be well correlated in GaN (MIS)HEMTs.**

***Index Terms*— Electrostatic discharge (ESD), gallium nitride (GaN), high electron mobility transistor (HEMT), human body model (HBM), radio frequency (RF).**

I. INTRODUCTION

GALLIUM nitride (GaN)-on-Si technology with 3-D monolithic heterogeneous integration technique is a promising candidate to enable the low cost and optimal high performant RF/mmWave front-end modules (FEM) in 5G applications [1], [2]. Wide bandgap with high electric field breakdown [3], high electron mobility [4], and high saturation velocity [5], [6] in 2-dimensional electron gas (2DEG) channel of the GaN high electron mobility transistors (HEMTs) provide superior lateral breakdown voltage and output power in RF/mmWave power amplifier (PA) designs [7]. Currently, the RF GaN transistor technology is mainly based on the Schottky HEMT. However, the GaN Schottky HEMTs suffer from high gate leakage due to the metal-semiconductor gate structures, which has an impact on the power-added efficiency (PAE) of the PA [8]. Thus, metal-insulator-semiconductor MIS-HEMTs [9], [10] are proposed to alleviate the gate leakage issue. In spite of the advantages of these GaN devices, they are known to suffer from well-studied reliability concerns, such as ON-resistance (R_{ON}) dispersion [11]–[13], time-dependent dielectric breakdown (TDDB) [14], [15], bias temperature instability (BTI), and hot carrier degradation (HCD) [16]–[18]. However, the investigations of the electrostatic discharge (ESD) reliability of RF GaN technology are still in a nascent stage.

A 50-Ω transmission line pulse (TLP) tester is commonly used to investigate device *IV* characteristics under a hundred-nanosecond ESD-like transient duration in the CMOS IC industry [19]. The previously reported ESD studies of GaN-based Schottky diodes [20] and (MIS)HEMTs [21]–[24] were evaluated by 50-Ω TLP testers. In [21], additional DC experiments on transconductance (g_m), OFF-state drain current (I_D), and gate-to-source current (I_{GS}) are essential to obtain an accurate failure current (I_{t2}) in the TLP I–V characteristics. Once the gate biases were applied to define the ON-state and OFF-state stress conditions in TLP experiments, the corresponding failure mechanism was revealed. The ON-state failures belong to power-dependent failures, whereas the OFF-state failures are electric-field-dependent failures in accordance with the failure analysis (FA) [22]. A more detailed analysis of ESD TLP failures in HEMT devices combined with the piezoelectric field, carrier trapping, and self-heating effects were studied [23]. Besides, ESD failure comparisons of RF MIS-HEMTs and HEMTs were primarily discussed in [24]. Although the 50-Ω TLP results can provide the device failure current levels, the commercial human body model (HBM) ESD robustness had been rarely certified in any of the prior

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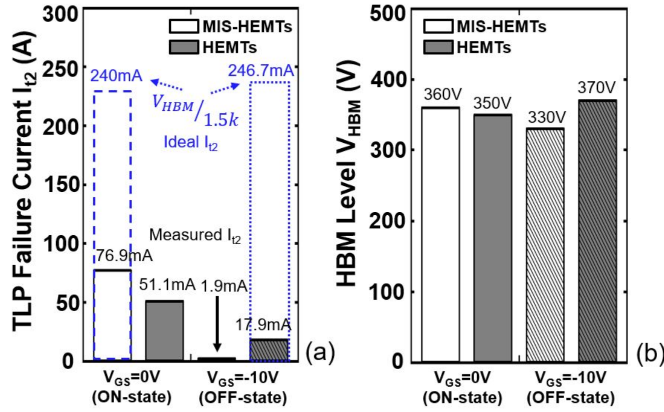

Fig. 1. (a) Measured TLP I_{t2}, and (b) measured HBM robustness (V_{HBM}) in GaN MIS-HEMTs and HEMTs at ON-state and OFF-state comparison. All the measured TLP I_{t2} have mis-correlation issue to the measured V_{HBM}. The ideal I_{t2} values which can use 1.5 kΩ factor are illustrated by blue columns. For ON-state stress, the TLP I_{t2} are limited by channel driving capability in saturation region, whereas for OFF-state stress, the TLP I_{t2} are the channel leakage of the devices, which causes worse correlation [24].

works [21]–[23]. Our previous work [24] has disclosed that the I_{t2} from 50-Ω TLP cannot be directly correlated with the standard-defined HBM robustness by the empirical correlation ($V_{HBM} = I_{t2} \times \sim 1.5$ kΩ). The results are depicted in Fig. 1.

In this article, in-depth investigations of the HBM discharge physical mechanism in RF GaN (MIS)HEMTs are conducted. Transient HBM I–V characteristics [25], [26] are used to propose a new transient discharge model, with a novel resistance modulation, which can successfully describe the transient discharge mechanism in the GaN (MIS)HEMTs. Moreover, the root cause of the mis-correlation between the TLP I_{t2} and HBM ESD robustness in the RF GaN (MIS)HEMTs is fundamentally linked to the discrepancy between LV CMOS technologies and RF GaN technologies. Finally, the updated correlation between TLP I–V and HBM I–V characteristics of GaN (MIS)HEMTs can be proposed and shown in this article.

II. RF GaN-on-Si (MIS)HEMT Technology

The MIS-HEMT and HEMT device structures are manufactured in 200 mm GaN-on-Si wafers [27]. A 2.2 μm GaN-based buffer, a 300 nm GaN channel, a 1 nm AlN spacer, and a 15 nm AlGaN barrier are grown sequentially on a high-resistivity Si (111) substrate and capped *in situ* with 5 nm SiN. An additional Al_2O_3 layer is deposited before the follow-up of the S–D formations. The *T*-shaped gate structure is made of a metal stack of 40 nm TiN/20 nm Ti/250 nm AlCu/20 nm Ti/60 nm TiN, such that the length of field plate metal toward the drain contact can be varied. The gate metal stack is deposited on the SiN capping layer in MIS-HEMTs directly, whereas the SiN layer in the channel region is etched out before depositing the gate metal in the case of HEMTs (to form a Schottky contact), as shown in Fig. 2(a) and (b). The geometric sizes in the experiments are fixed at $W = 100$ μm,

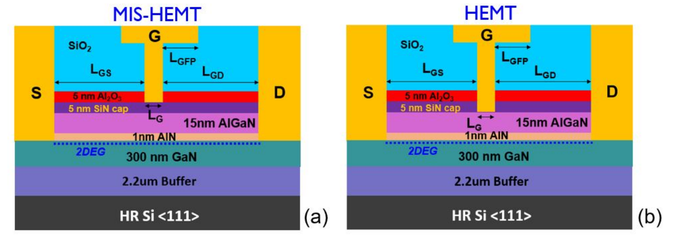

Fig. 2. Cross-sectional views of GaN-on-Si (a) MIS-HEMT and (b) HEMT [27].

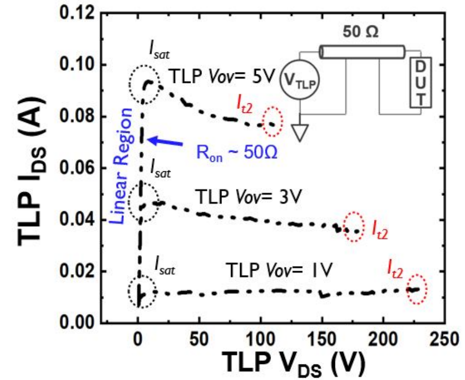

Fig. 3. 100 ns 50 Ω TLP I–V results for V_{OV} of 1, 3, and 5 V. The V_{OV} is equal to (V_{GS}–V_{th}). The V_{GS} is the gate-to-source voltage, and the V_{th} is the threshold voltage which is −5V in the MIS-HEMTs. The source and substrate biases are grounded. In linear region, the ON-resistance (R_{ON}) is ∼50 Ω. The current level in saturation region is determined by the channel driving capability. The I_{t2} are lower than the initial I_{sat} [24], [28].

$L_G = 1$ μm, $L_{GD} = 1.75$ μm, $L_{GS} = 1.5$ μm, and $L_{GFP} = 0.5$ μm.

III. TLP Versus HBM

The inserted figure in Fig. 3 shows the simplified 50-Ω TLP setup. The TLP source is a square wave with 100 ns pulsewidth. The voltage and current values in the TLP I–V are averagely calculated in each measured voltage and current waveform with the sampling window from 70% (70 ns) to 90% (90 ns) of the pulsewidth. Hence, the TLP I–V curves can be depicted in Fig. 3. On the other hand, the HBM source is principally made of a 100 pF capacitor and a 1.5 kΩ resistor, as shown in the inserted figure in Fig. 4(a). The HBM tester originally will only offer pass/fail levels for industrial qualification. However, in this article, the proposed transient HBM I–V [25] can provide additional information as compared to TLP I–V in GaN (MIS)HEMTs. The full transient HBM I–Vs are depicted from the voltage and current waveforms at a certain pre-charge voltage. Thus, the full time domain information is included in the transient HBM I–V curves.

The corresponding 50-Ω TLP I–V characteristics of the MIS-HEMTs with different overdrive voltages (V_{OV} =1, 3, 5 V) are shown in Fig. 3 [28]. Before current saturation, the R_{ON} in the linear region of the transistor is similar for the different V_{OV}. In the saturation region, the TLP saturation

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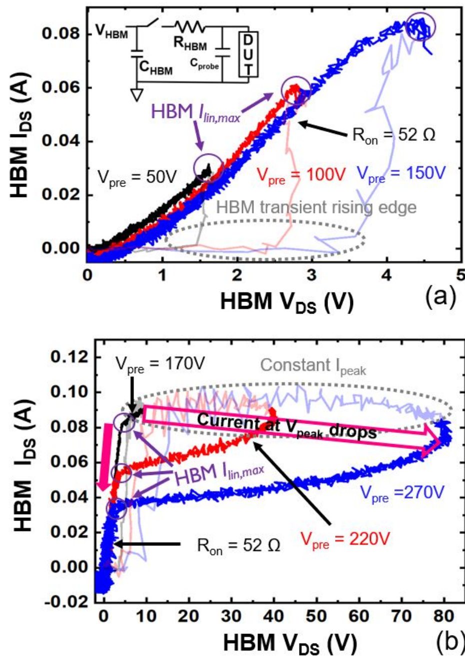

Fig. 4. (a) HBM transient I–V curves with the V_{pre} of 50, 100, and 150 V. The three HBM I–V curves all have a linear R_{ON} of 52 Ω which is like TLP linear R_{ON}. (b) HBM transient I–Vs with the V_{pre} of 170, 220, and 270 V. The HBM transient rising edges induce the high V_{DS} of ∼40 and ∼80 V in V_{pre} of 220 and 270 V, respectively. Afterward, both V_{DS} and I_{DS} are progressively decreased in a saturation region. When $V_{DS} < V_{OV}$ (5 V), the device operates again in the linear region. Moreover, the larger V_{pre} has a lower $I_{lin,max}$ [28].

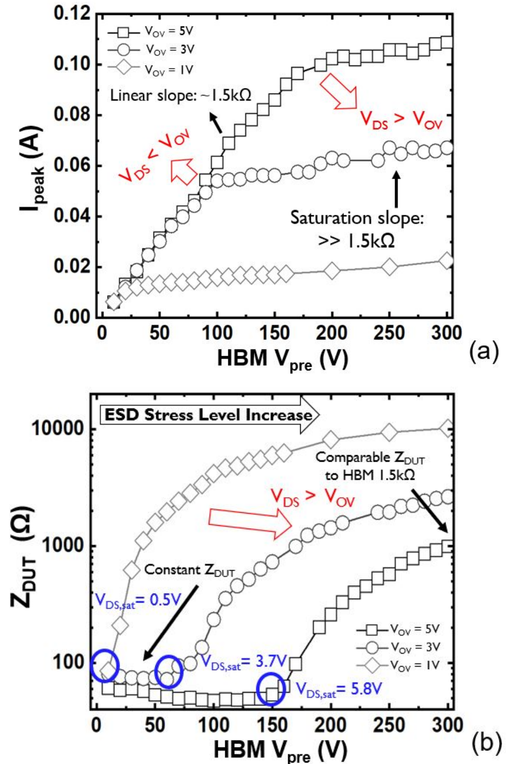

Fig. 5. HBM V_{pre} versus (a) HBM transient I_{peak} and (b) corresponding Z_{DUT}. Z_{DUT} are extracted from the HBM transient peak voltage (V_{peak}) and I_{peak}. In the linear region ($V_{DS} < V_{OV}$), the I_{peak} is linearly increased while Z_{DUT} maintains constant, whereas in the saturation region ($V_{DS} > V_{OV}$), I_{peak} is independent of V_{pre} and Z_{DUT} is consequently raised by increasing V_{pre}. Different V_{OV} determined the V_{pre} deviation of the turning points to increase the Z_{DUT} (blue circles) [28].

currents follow the individual DC channel driving capability at each V_{OV}. The current collapse is observed as the drain voltage (V_{DS}) increases and the higher driving current facilitates the current collapse effect [29], [30]. This results in the I_{t2} level lower than the initial saturation current (I_{sat}). However, these I_{t2} levels (∼10 to 80 mA) cannot match the measured >300 V HBM ESD robustness (V_{HBM}) based on the empirical correlation between HBM and TLP (Fig. 1). Consequently, the HBM transient I–V characteristics are used to understand the root cause of this mis-correlation.

The HBM transient I–Vs of the MIS-HEMTs are depicted at V_{OV} of 5V in Fig. 4. In low HBM pre-charge voltage ($V_{pre} <$ 160 V), the maximum transient HBM linear current ($I_{lin,max}$) is linearly increased with a fixed R_{ON} of ∼52 Ω [Fig. 4(a)], which is similar to the TLP R_{ON} in the linear region. However, as $V_{pre} >$ 160 V, the V_{DS} corresponding to HBM peak voltage (V_{peak}) is significantly increased, as shown in Fig. 4(b). This results in a high-impedance discharge region. Eventually, when the V_{DS} is back to the linear region condition, the discharge impedance can be aligned back to the linear R_{ON} in Fig. 4(a). However, the corresponding $I_{lin,max}$ is obviously reduced by increasing the HBM V_{pre}. The higher HBM V_{pre} induces higher V_{peak} and accompanies a more pronounced current drop from the I_{peak}. In addition, a large voltage drop from the higher HBM V_{peak} to the low V_{DS} in the linear region can cause further current drop during the saturation-to-linear transition. Fig. 5 shows the impact of different V_{OV} conditions on the peak current (I_{peak}) and DUT impedance (Z_{DUT}) extracted from the HBM transient waveforms. In Fig. 5(a), the I_{peak} is linearly increased in the linear condition ($V_{DS} < V_{OV}$). However, it saturates when $V_{DS} > V_{OV}$, where the Z_{DUT} becomes critical and comparable with the HBM source resistor of 1.5 kΩ, as shown in Fig. 5(b). The measured $V_{DS,sat}$ values as the boundaries of linear and saturation are close to the corresponding V_{OV} values. When the $V_{DS} > V_{DS,sat}$, the Z_{DUT} starts to be modulated from low constant impedance (∼50 Ω) to high increasing impedance (>900 Ω). These measured results imply that a different ESD HBM discharge mechanism exists in the GaN (MIS)HEMTs. The increase of the Z_{DUT} by increasing V_{peak} will be discussed in next section by TCAD and SPICE simulations.

IV. HBM Discharge Mechanism

RC parasitic components exist in the RF GaN (MIS)HEMTs, as illustrated in Fig. 6 [31]. From the experiments in [28], the HBM discharge impedances in the linear region are determined by the resistance composed by the $2R_C$, $R_{acc,D}$, R_{ch}, and $R_{acc,S}$ in the 2DEG. In order to investigate the reasons for increasing HBM discharge impedance in the saturation region, TCAD and SPICE simulations are used in the following paragraphs to understand the impact of the other *RC* components in Fig. 6.

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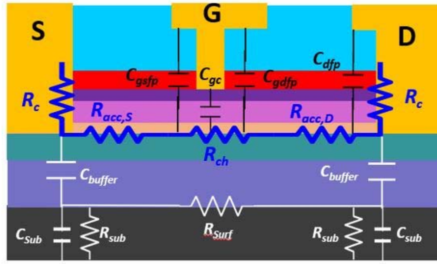


Fig. 6. Parasitic *RC* model in GaN (MIS)HEMTs. The R_C, $R_{\text{acc},D}$, $R_{\text{acc},S}$ and R_{ch}, respectively, represent contact, drain-side access region, source-side access region, and channel resistance. The R_{surf} and R_{sub} are the interface resistance between the buffer and substrate and the resistance in the Si substrate. C_{buffer} and C_{sub} are the capacitance for buffer layer and substrate. C_{dfp}, C_{gc}, C_{gdfp}, C_{gsfp}, represent drain-to-channel, gate-to-channel, gate field plate-to-channel (drain-side), and gate field plate-to-channel (source-side) capacitance, respectively, [28], [31].

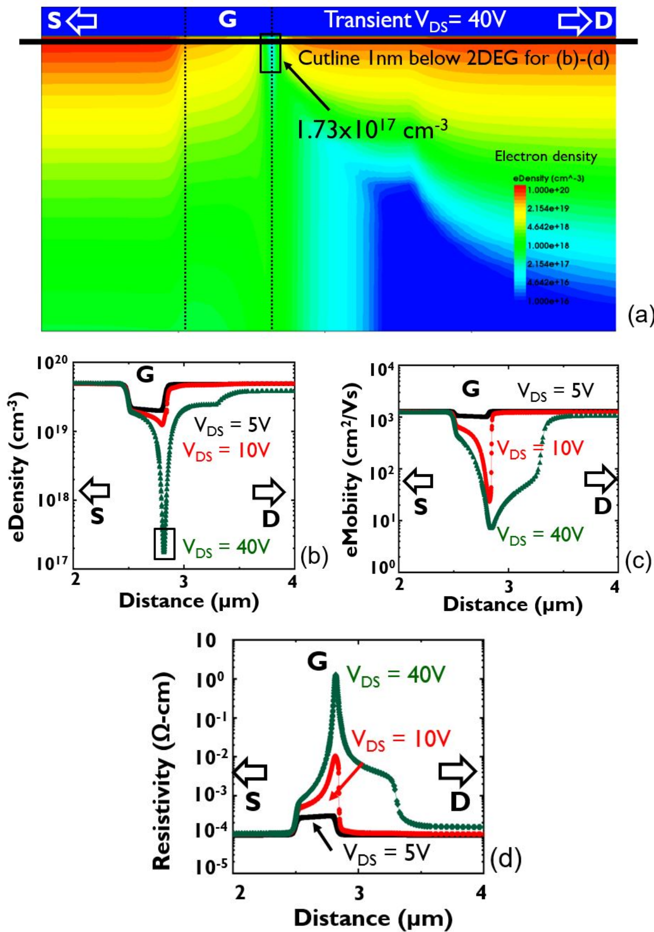
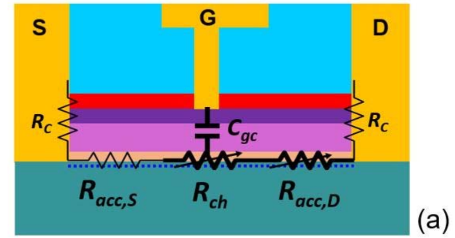


Fig. 7. (a) TCAD simulation results of the electron density (N_e) in cross-sectional view at transient V_{DS} of 40 V. The horizontal line in the cross-sectional view is cut at 1 nm below the 2DEG surface to observe the distribution from source to drain. The distribution of (b) N_e, (c) electron mobility (μ_n), and (d) resistivity in the horizontal cutline view with the transient V_{DS} of 5, 10, and 40 V. Both the N_e and μ_n significantly dropped at the gate corner to the drain side when the V_{DS} is increased from 5 to 40 V, resulting in the resistivity significantly increased [28].

TCAD simulations by Synopsys Sentaurus Device are deployed with transient source at the drain side and with the gate and the source of the GaN (MIS)HEMT grounded. The resistivity of the 2DEG channel can be calculated by the equation of $(q \times \mu_n \times N_e)^{-1}$, where q is the electron charge, μ_n is the electron mobility, and N_e is the electron density. Fig. 7(b) shows that electron density (N_e) significantly reduced from 10^{20} cm^{-3} to 10^{17} cm^{-3} by increasing V_{DS} from 5 V (linear region) to 40 V (saturation region) due to the channel pinch-off. The depletion area is located at the gate corner of the drain side and the gate-to-drain access region in the vicinity of the gate. The cutline depth in Fig. 7(b)–(d) is the 1 nm below the interface of the 2DEG channel to observe the parameters in the equation varied by the V_{DS} increase [28]. Not only N_e is significantly reduced [Fig. 7(b)], but also the μ_n drops $\sim$100$\times$ from the V_{DS} of 5 to 40 V [Fig. 7(c)]. With the increasing transient V_{DS}, the overall resistance mainly corresponding to the R_{ch} at the gate corner of the drain side can be modulated more than $\sim$10 kΩ·cm [Fig. 7(d)]. Besides, the piece of $R_{\text{acc},D}$ near the gate corner is also modulated by the high transient V_{DS}. From the simulation results, the impedance increase in the saturation region comes from the R_{ch} and $R_{\text{acc},D}$.



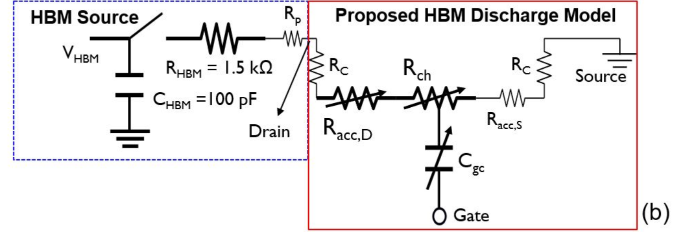


Fig. 8. (a) Calibrated HBM transient *RC* discharge model in GaN (MIS)HEMTs. (b) Schematic of HBM source and proposed HBM discharge model. The HBM source which has been simplified by removing some parasitic components in [28] includes the parasitic resistance (R_p) of the probe needles.

The impact of the parasitic capacitance on HBM V_{peak} for the buffer thickness variation and the chuck bias conditions have been presented [28]. It is proved that the C_{buffer} and C_{sub} have no influence on V_{peak}. From the calculated individual parasitic capacitors indicates that the C_{gc} is dominant among the other capacitors [28]. Thus, compared to the other capacitors, C_{gc} can be seen as a dominant capacitor in the HBM transient discharge model [Fig. 8(a)]. The schematic of the proposed HBM transient discharge model in the GaN (MIS)HEMTs with the simplified equivalent circuit of HBM ESD source is depicted in Fig. 8(b). The SPICE simulations by Keysight ADS are constructed to verify the impacts of R_{ch}, $R_{\text{acc},D}$, and C_{gc} on HBM discharge mechanism. All the *RC* values are extracted from the measurement results. In a linear region with the V_{pre} of 100 V, the simulated voltage waveform is perfectly matched to the measurement [Fig. 9(a)]. From the *RC* time

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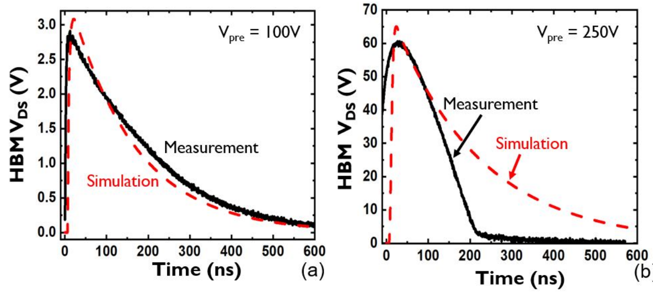

Fig. 9. HBM voltage waveforms of SPICE simulation and HBM measurement in (a) $V_{pre} = 100$ V, and (b) $V_{pre} = 250$ V. The fixed R_{DS} values in simulation can match to the measurement waveform in $V_{pre} = 100$ V (linear region), whereas it cannot match to the measurement in $V_{pre} = 250$ V (saturation region) due to the dynamic R_{ch} and $R_{acc,D}$ during the falling edge of discharge waveform [28].

constant (τ_{rc}), the R is mainly related to the sum of R_{HBM} in the HBM source and the total resistance in the model, and the C is only dominated by the C_{HBM} of 100 pF. C_{gc} is too small to impact the HBM waveforms. In Fig. 9(b), the simulated V_{peak} in the V_{pre} of 250 V is consistent with the measured V_{peak}. However, the full simulated discharge waveform cannot match the measured result.

This mismatch is attributed to a fixed simulated R_{DS}. In fact, the TCAD results have indicated the R_{ch} and $R_{acc,D}$ can be significantly modulated by high V_{DS}. This modulated R_{ch} and $R_{acc,D}$ can directly bring the impact on R_{DS} ($2R_C + R_{acc,S} + R_{acc,D} + R_{ch}$). With the modulated R_{ch} and $R_{acc,D}$ from 527.8 to 15.8 Ω depicted in Fig. 10(a) (dash lines), the measured voltage waveform will follow these modulation dash lines. Eventually, the waveform follows the linear region with the constant impedance. Fig. 10(b) demonstrates the discharge mechanism during the full HBM transient I–V. At the beginning of the HBM rising edge, the high V_{pre} of 250 V suddenly increases V_{DS} and I_{DS}. As the V_{DS} increased (phase A), the I_{peak} can be obtained at the V_{DS} of ∼36 V. Afterward, the I_{DS} progressively decreases until the $V_{DS} = V_{peak}$. After the V_{peak} (phase B), the R_{ch} and $R_{acc,D}$ are modulated from the order of 527.8 to 15.8 Ω as the V_{DS} decreased in the saturation discharge region illustrated in Fig. 10(a). The R_{ch} and $R_{acc,D}$ modulation will be ended until the V_{DS} back to the linear discharge region (phase C).

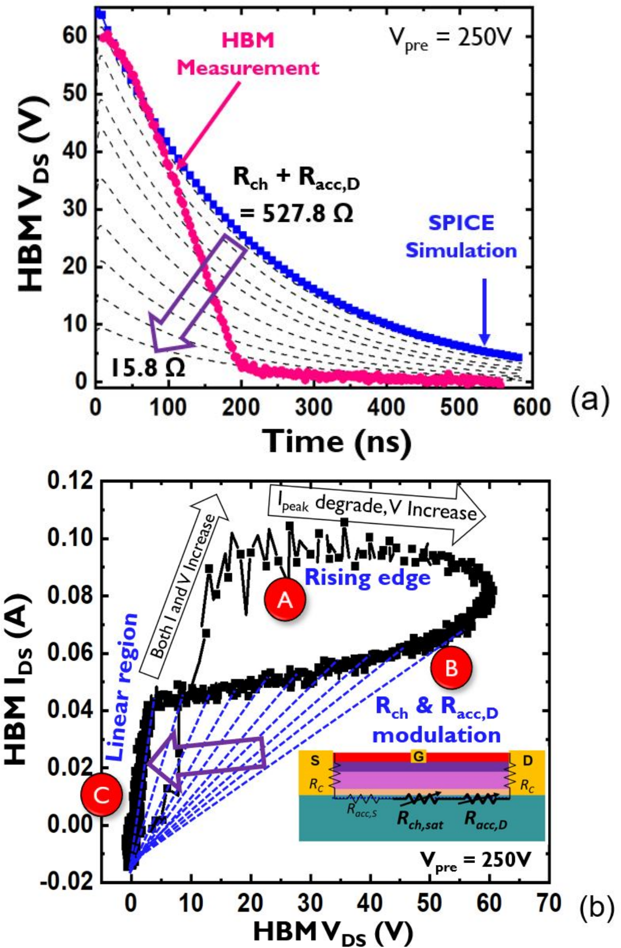

Fig. 10. (a) SPICE simulated voltage waveforms with the modulated ($R_{acc,D} + R_{ch}$) from 527.8 to 15.8 Ω under the pre-charge voltage (V_{pre}) of 250 V are shown as the dash lines. The measured HBM voltage waveform can follow the simulated waveforms with different ($R_{acc,D}+R_{ch}$) values. This demonstrates that the ($R_{acc,D} + R_{ch}$) are dynamically modulated during the discharge period. (b) Corresponding measured HBM transient I–V characteristics are defined with three different discharge phases. During the rising edge (phase A), the high V_{pre} of 250 V causes the abruptly raising V_{DS} and I_{DS}. After the I_{peak}, the V_{DS} is still raising to the V_{peak} while the I_{DS} slightly degrades. Phase A ends when the V_{DS} reaches to V_{peak}. After the V_{peak}, due to the ($R_{acc,D} + R_{ch}$) dynamic modulation, the V_{DS} and I_{DS} are gradually decreased following the high impedance change in phase B. When V_{DS} drops <5 V (phase C), the ($R_{acc,D} + R_{ch}$) modulation is ended and the resistance is back to the constant 52 Ω in the linear region (phase C) [28].

V. Discussion

A. Physical Mechanism Under HBM Transient Rising Edge

In the HBM model, the HBM V_{pre} discharges the DUT through the 1.5 kΩ resistor. In a low-impedance DUT ($R_{DUT} \ll 1.5$ kΩ), the I_{peak} will be mainly determined by the 1.5 kΩ resistor and the V_{peak} is from the IR drop of the I_{peak} and R_{DUT}. In the GaN (MIS)HEMTs, however, the high impedance in the saturation region limits the I_{peak}, which matches the maximum 2DEG driving capability (I_{max}). The limited I_{peak} discharging through the 1.5 kΩ generates a lower voltage drop, which consequently increases the voltage potential at the drain terminal of the GaN (MIS)HEMTs. This can cause the obvious rising time difference (∼40 ns) between HBM transient voltage and current waveforms, as shown in Fig. 11(a). The I_{DS} and V_{DS} will be adjusted by following Kirchhoff's voltage law (KVL) during the t_1 and the t_2 in Fig. 11. However, a significant current collapse which is induced by an extra mechanism is observed in the HBM transient waveforms. In the ideal case without any current collapse, the I_{peak} follows the constant saturated current $I_{DS,sat}$, which is equaled to the I_{max}. In reality, the current collapse of the saturated I_{DS} has been observed in the TLP I–Vs with <100 ns stress duration. Fig. 3 shows the 15% of current collapse at the V_{OV} of 5 V. Nonetheless, the current collapse in the measured HBM current waveform is much pronounced than the 15% current collapse. It implies the extra mechanism

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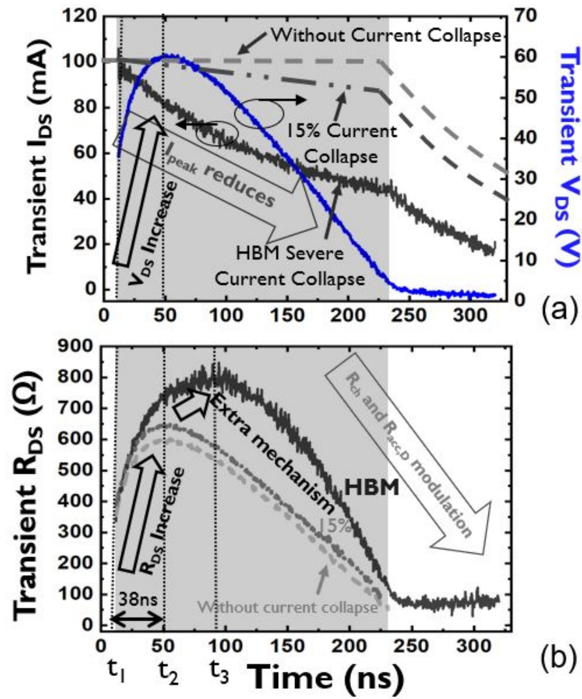

Fig. 11. (a) Measured HBM voltage and current waveforms at $V_{pre} = 250$ V with two illustrated current waveforms without current collapse and 15% current collapse. (b) Corresponding transient R_{DS}. At the rising edge, the I_{peak} (t_1) occurs earlier than V_{peak} (t_2). With the severe current collapse, the peak R_{DS} is after the V_{peak}, as compared to the peak R_{DS} which is aligned to the V_{peak} without the severe current collapse. After the V_{peak}, the device starts to discharge with the transient resistance modulation and extra mechanism until back to the constant R_{DS}.

of the current collapse under the HBM stresses. The corresponding transient R_{DS}, as shown in Fig. 11(b), also indicates that the time of peak R_{DS} aligns to the V_{peak} without the severe current collapse. However, with the severe current collapse in the measured HBM current waveform, the peak R_{DS} will be shifted from the V_{peak} at t_2 (50 ns) to t_3 (95 ns). The transient resistance modulation is not only determined by the I_{max} but also impacted by the severe current collapse induced by the extra mechanism. This extra mechanism might be attributed to additional nano-seconds transient trapping effects from [29].

B. GaN (MIS)HEMTs Versus CMOS LV Transistors

Different from the GaN (MIS)-HEMTs, an ESD clamp transistor in *LV* CMOS technology has a parasitic BJT which can provide a low-impedance discharge current path while it triggered. Its impedance is typically lower than 50 Ω of the TLP tester. Consequently, its I_{t2} can well correlate to the V_{HBM} with a factor of ∼1.5 kΩ. However, the GaN (MIS)-HEMT has an impedance much higher than 50 Ω (close to 100–1 kΩ) after the current saturation. This high impedance induces the mis-correlation between TLP I_{t2} and V_{HBM} (Fig. 12). In order to roughly estimate the HBM robustness from TLP I_{t2}, the impedance of GaN (MIS)HEMTs should be considered in a revised correlation of $V_{HBM} = I_{t2} \times (R_{HBM} + R_{DS})$. However, the severe current collapse observed in the HBM current waveform can induce an additional R_{DS} deviation from the revised correlation.

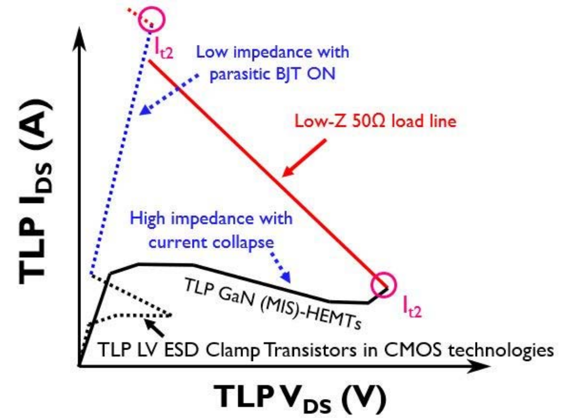

Fig. 12. Illustrated TLP *I–V* characteristics of the ESD clamp transistors in *LV* CMOS technologies and GaN (MIS)HEMTs. As compared to LV CMOS device, the GaN transistor does not have parasitic BJT providing low-impedance current path before it failed. Instead, the GaN TLP current is saturated with much higher impedance than the 50 Ω TLP tester. The high impedance can induce the mis-correlation between TLP I_{t2} and HBM ESD robustness (V_{HBM}) [28].

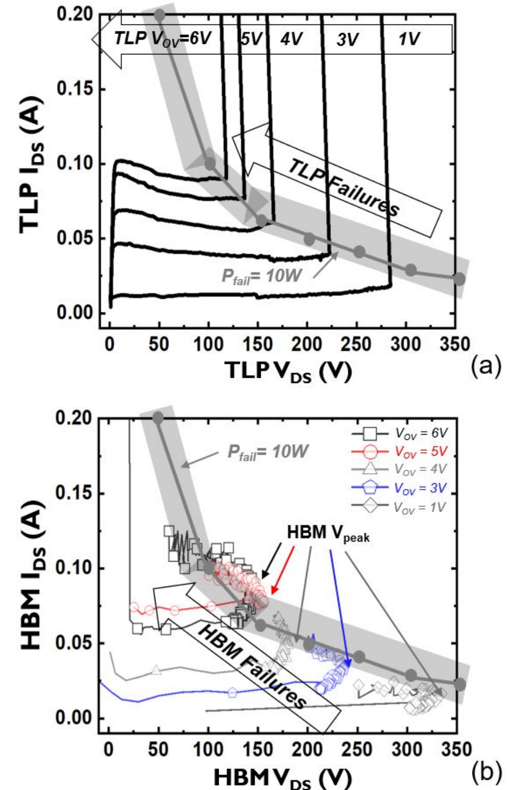

Fig. 13. Measured (a) TLP *I–V* curves and (b) HBM transient *I–V* curves with different V_{OV} after the device failures. The constant failure power of 10 W is illustrated. Both ON-state TLP and HBM follow the power failure mechanisms [22], [24].

C. Failure Mechanisms in TLP and HBM

The benefits of the HBM transient I–Vs which can provide more information than the TLP I–V have been revealed

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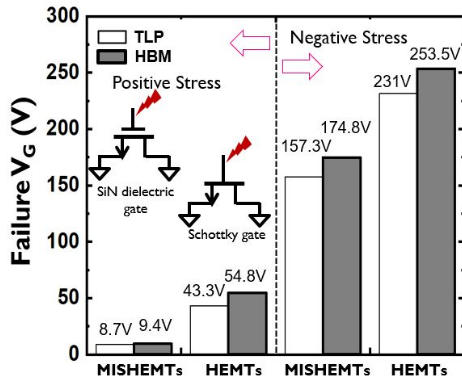

Fig. 14. GaN (MIS)HEMT gate failures in the TLP and HBM tests. Both TLP and HBM stress configuration in the gate immunity tests are zapping gate terminal with drain–source, and substrate grounded. The TLP and HBM failure voltages are consistent in both positive and negative stresses [24].

in [28]. However, a completed failure mechanism in HBM ESD stress has not yet been disclosed. Fig. 13(a) indicates the ON-state TLP failures of the GaN (MIS)HEMTs follow the constant power curve of 10 W. The deviation can be observed in the low V_{OV} bias conditions ($V_{\mathrm{OV}} = 1$–3 V). This ON-state failure mechanism has been proposed in [22]. Furthermore, Fig. 13(b) shows the ON-state HBM failure mechanisms, which approximately follows the same constant power curve in the TLP results [Fig. 13(a)]. Different from the TLP results, the deviation of the ON-state HBM failures at the V_{peak} from the constant power curve can be seen in each V_{OV}. The root cause may be related to the severe current collapse and different sampling windows of the captured I–V characteristics between TLP and HBM. On the other hand, in [22] and [24], OFF-state TLP failure mechanisms are determined by the constant voltage (electric-field), which is intrinsically attributed to the gate immunity of the devices. Fig. 14 presents the gate immunity in the MIS-HEMTs under the TLP and the HBM tests. The TLP gate immunity tests have been discussed in [24]. The HEMTs which have higher TLP failure levels in terms of positive and negative stresses are also evaluated. The corresponding HBM gate immunity tests are included in Fig. 14. Compared with the TLP failure levels [24], the slightly higher HBM failure voltages directly captured at the gate terminal could be attributed to the different sampling windows in the TLP and HBM. Overall, the OFF-state failure mechanisms of the GaN-on-Si MIS-HEMTs and HEMTs are consistent in the TLP and HBM.

VI. Conclusion

In this work, the mis-correlation between TLP I_{t2} and V_{HBM} has been investigated in detail. The new proposed HBM discharge model with the dynamic resistance modulation is revealed and successfully explains the HBM transient discharge mechanism. This modulation induces the total discharge impedance variation from ~560 to ~52 Ω under the V_{pre} of 250 V. By the TCAD and SPICE simulations, the root cause of the resistance modulation is attributed to the influence of the V_{DS} on μ_n and N_e in the 2DEG channel (R_{ch}) and the drain access region ($R_{\mathrm{acc},D}$). The severe current collapse induced the extra mechanism has been observed under the HBM transient current waveform. This caused more pronounced resistance modulation under the HBM ESD stresses. The revised correlation between the TLP I_{t2} and HBM robustness (V_{HBM}) has been proposed. However, the extra parasitic components in HBM source, the severe current collapse in the HBM current waveforms, and different sampling windows between TLP and HBM can bring the influence on the revised correlation. Finally, the TLP and HBM failure mechanisms have been completely compared in the ON-state and OFF-state GaN (MIS)HEMTs. In general, the ON-state and OFF-state failures in the TLP and HBM still follow the constant power and electric field mechanisms, respectively.

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