# E-test validation of space error budget and metrology

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***Abstract*— The electrical validation of a generalized space error model is reported. This was achieved by comparing inline e-beam "direct" space metrology measurements with an end-of-line, yield-based, space error metric. This electrical test (e-test) of the space error is derived from the conductance of metallized test structures with programmed interlayer offsets between line and block layers used for patterning. Local space variation was extracted from voltage contrast arrays, and from inline metrology statistics. A good match was observed between the predicted space error from the weighted sum of the local and non-local terms, and the measured e-test space error. A model is proposed for the experimental validation of the local term (stochastic) of the space error model.**

***Index Terms*—Space error, Edge placement error, Electrical test device, Voltage contrast**

## I. Introduction

Edge placement error (EPE) is defined for a single layer as "a term which refers to the placement of edges of lines and other features in comparison to the target placements as specified by the circuit designer" [1]. On the other hand, space error (SE) refers to the space variation in between two layers as explained by Gabor et al. [2]. SE is defined as a global parameter, a weighted sum of errors due to CD, overlay, optical proximity correction (OPC), etch biases, line edge roughness (LER) over the whole wafer. The challenge is to experimentally validate this metric which results from potentially more than $10^9$ failure opportunities. Thus, accurate measurement of edge placement error and space error are gaining importance in advanced semiconductor technologies [3-7], as the number of parameters contributing to these errors continues to increase, thereby limiting yield.

Understanding the relative importance of the sources of variation within the SE budget has led to different models [2;8-11], which need to be validated. However, a direct measurement of this SE through, e.g., e-beam metrology, provides its own challenges [9;12-14]. Depending on the use case, SE includes a "snapping" term which will be discussed in Section III.A and is difficult to estimate without wafer data. Hence, it is useful to know the relevance of the measured space error components to device yield.

**Eq.(1.1)** describes our base assumption that systematic, global and local errors combine additively, based on the nested, extreme-value model of Ref. [8], rather than through the alternative root-sum-squared averaging of these terms. **Eq.(1.2)** is our general equation where the coefficients *m*, *n* & *p* depend on the number of failure opportunities of a given device per chip and on the length scale of global variation (e.g. wafer, lot, fab, ...). These coefficients refer to the number of sigma value at which design-rules need to be tested to ensure high yield [2] for each of the corresponding terms. The length scale of global variation effects is assumed to be larger than ~100um, whereas local (stochastic) effects occur at a much higher spatial frequency, with a characteristic length of a few nanometers.

$$SE_{max} = '\,systematics' + 'local' + 'global' \tag{1.1}$$

$$SE_{max} = \frac{HR_{OPC}}{2} + \frac{m\sigma_{PBA}}{2} + n\,\sigma_{LER} + \sqrt{\left(p\sigma_{overlay}\right)^2 + \left(\frac{p\sigma_{CDU}}{2}\right)^2} \tag{1.2}$$

$$\text{With } \sigma_{LER} = \sqrt{\sigma_{LER,line}^2 + \sigma_{LER,block}^2} \tag{1.3}$$

$$\text{and } \sigma_{CDU} = \sqrt{\sigma_{CDU,line}^2 + \sigma_{CDU,block}^2} \tag{1.4}$$

The first part of the equation **Eq.(1.2)** is summed in a linear way and represents the systematic errors that repeat each die, and the local stochastics errors. The first term $HR_{OPC}$ is the half-

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range of the CD error due to optical proximity (OPC) residuals. The second term represents proximity bias average (PBA), which is the field average CD variation caused by scanner tool-to-tool variation. **Eqs.(1.3)-(1.4)** refer respectively to the last two terms of **Eq.(1.2)** for the specific case of patterning line-ends with a block mask. The local errors term ($\sigma_{LER}$) originates from resist and photon stochastics and is typically measured as line edge roughness (LER) [15]. The overlay and CDUs of lines and blocks are seen as independent variables that impact the global space error. Therefore, a root sum square of these components is used to estimate the space error. Overlay includes imaging pattern placement errors coming from reticles, imaging and patterning steps, but also incorporates scanner grid matching components and pattern shift uniformity caused by optical effects in the projection and illumination optics. The CDU includes reticle error, scanner error and CD errors coming from etch and deposition processes.

The goal of this study is to investigate the validation of the proposed model and determine experimentally the $n$-sigma local component resulting from stochastic events on a given family of devices. The first two terms of **Eq.(1.2)** ($HR$ & $\sigma PBA$) are not addressed, and the effect of Overlay/CDU is derived from a single SEM image per die or from a single voltage contrast array location. Thus, the focus is on validating experimentally the coefficient $n$ of the $\sigma_{LER}$ term, which is also the largest contributor to edge placement error in leading-edge nodes.

In this paper, two electrical measurement techniques were used. The first method allows to extract the worst-case SE between line and block layers by examining open or short margins in conductive structures patterned using both layers. It consists in measuring the resistance through a structure connected to large pads. Structures cover an area of ~100x30µm or more, containing $10^3$-$10^6$ active features, and will typically yield one datapoint (the electrical resistance). To extract the SE, several structures need to be tested, each corresponding to a different placement of the features in both layers relative to each other (*e.g.* relative placement of lines and blocks). The process yield is high enough to ascertain the electrical failures of the e-test structures are mostly caused by block-to-line placement, rather than by effects not related to the SE, such as metal stringers, particles, etc.

The second measurement technique is based on voltage contrast (VC) [16-17], and is used to assess the local contributor to the SE budget. The measurement is carried out by using an e-beam tool on a device under test (DUT). Floated features in the DUT are charging up positively once exposed to the electron beam. Hence, the majority of produced secondary electrons are prevented from reaching the detector. These structures appear dark in the e-beam image. On the other hand, grounded features do not charge and appear bright thanks to the high secondary electron yield. Within the e-beam image field of view, many independent features can be tested separately, giving statistical information of the local contributors to SE. This technique enables the validation of the local SE term with statistical data but can only sample a limited number of features and locations.

Wafer processing steps and metrology techniques are described in Section II. In Section III, the correlation between inline e-beam "direct" space metrology with an end-of-line e-test SE metric is investigated. The experimental validation of the stochastic term of the extreme value SE formula is investigated in Section IV.

## II. EXPERIMENTAL DESIGN AND METHODS

### *A. Description of the process flow*

In this work, a litho-etch-litho-etch (LELE) process was chosen and combined with a block approach to achieve a 48nm metal (M1) pitch using a 193nm immersion scanner. The pattern was decomposed into three layers Me1A, Me1B and Block layers. Me1A and Me1B layers were patterned into a single oxide "memory layer". The metallization strategy is a single damascene approach. A simplified process flow is shown in **Fig. 1(a)**. The relative placement of block and line edges during patterning therefore determines the continuity of the line, as described in **Fig. 1(b) & Fig. 1(c)**.

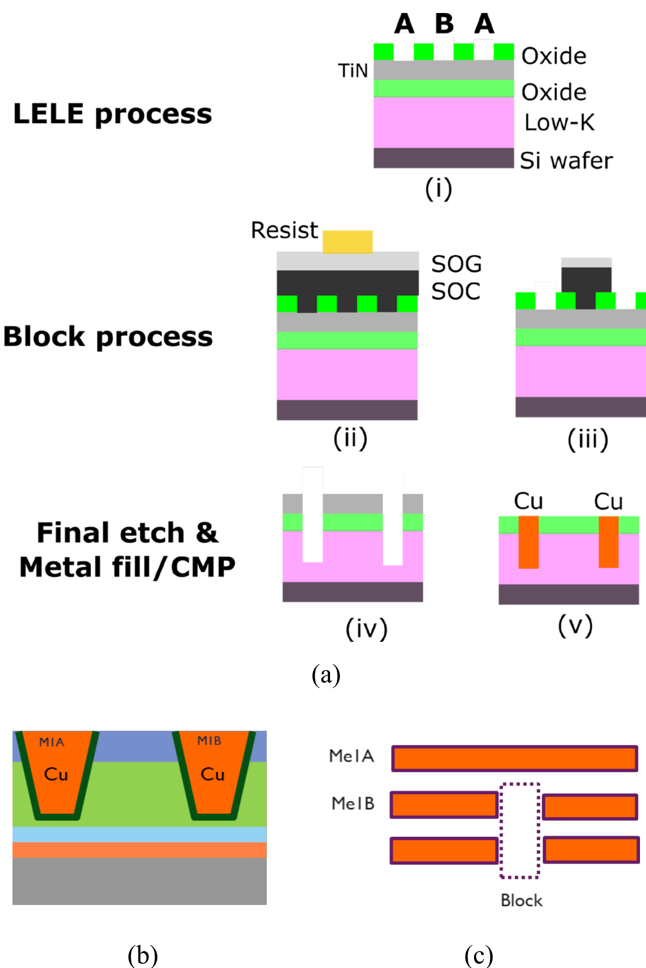


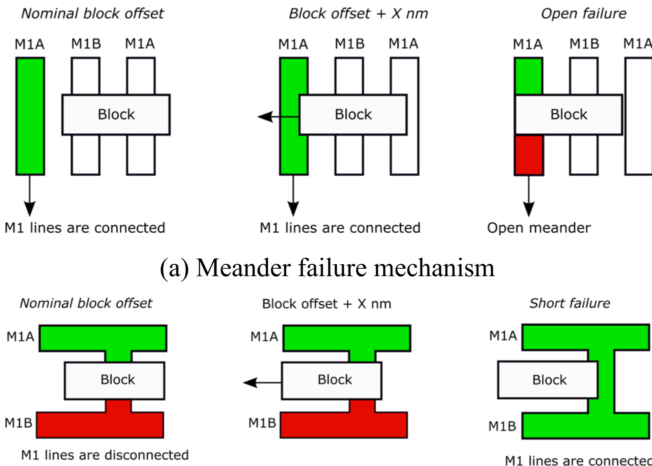

**Fig.1.** Process flow showing LELE and block approach to achieve 48nm pitch.

BEOL stack deposition was followed by the first layer Me1A lithography exposure under an ASML immersion scanner. The post-lithography target critical dimension (CD) for the trenches was 24nm. A negative tone lithography development (NTD) process was chosen to pattern the trenches. An 85 nm resist on top of 30nm Spin-on-glass (SOG) and 100nm Spin-on-carbon (SOC) was first patterned. The resist patterns were consequently etched down into the SOG/SOC using a plasma-

assisted etching technique in a Tokyo Electron Limited (TEL) equipment, and then transferred into an oxide layer. A second lithography exposure was performed to pattern the Me1B layer, followed by transferring the pattern onto the same oxide storage layer. The block layer was then processed using a positive tone lithography development (PTD) process. The stack consisted of a resist on top of SOG and SOC. A Focus Exposure Matrix (FEM) was exposed with dose variation on x-axis and focus variation on y-axis. The purpose is to obtain (1) a wide variation in the CD fingerprints to assess the impact of the mean CD component of the global variation term", (2) and modulate the local CD variation to assess its impact on the local error term. The resist patterns were subsequently etched down into the SOG/SOC layers using a plasma-assisted etching technique. At this intermediate process step (SOC open), inline e-beam block-to-line space data was collected as described in Section II.C. Finally, the patterns were etched down into the TiN hard mask layer and consequently into the low-*k* material. These trenches were then filled with copper, followed by a chemical-mechanical polishing step.

*B. Description of the electrical testing and structure*

In this study, two families of e-test devices (meander and fork-fork) were investigated, showing opposite failure modes. The reticle field is divided into 25 sub-dies. Within a reticle field, each sub-die contained a set of 24 electrical structures Each set contains electrical devices that are identical, except for a slightly different block offset ranging from 0 nm to 38 nm as schematically shown in **Fig. 2**. The block offset is a design offset which describes how much the block is shifted from the line pattern. Hence, an increasing block offset leads to a shorter block-to-line space. The meander fails when a particular block cuts the conductive metal line, leading to an open (**Fig. 2(a)**). In the fork-fork structure, the failure happens when the block no longer cuts the metal line, leading to a short (**Fig. 2(b)**).

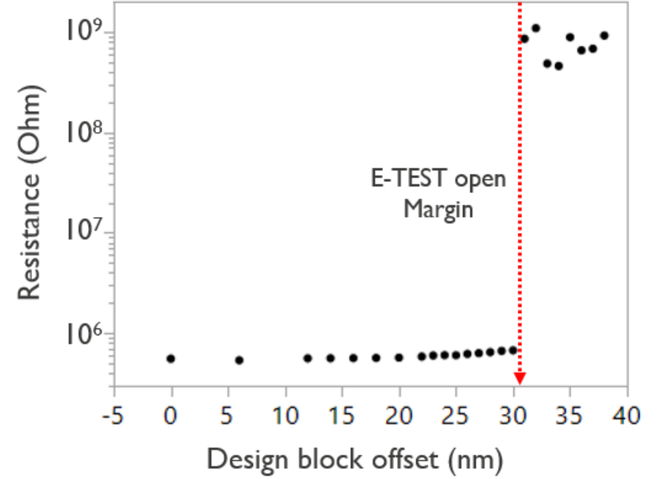



(a) Meander failure mechanism

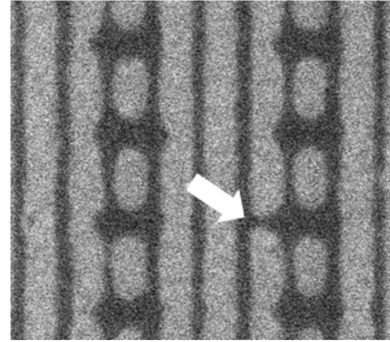
(b) Fork-Fork failure mechanism

**Fig 2.** Description of e-test devices

Each meander or fork-fork structure contains ~$10^5$ or ~$2x10^5$ block units, respectively. At the end of line, the resistance of all structures is measured within a set. Considering that the block-to-line space is gradually offset in the X direction by 1nm block offset steps, line resistance increases as blocks start to cut the active line, as shown in **Fig. 3(a)**. When the block offset passes a certain threshold, the line is fully cut in at least one location (**Fig. 3(b)**) which leads to a resistance increase of several order of magnitude.




(a) Meander resistance as function of block offset



(b) SEM image of an open failure on a meander

**Fig. 3.** Electrical failure in e-test device

The block offset threshold at which the e-test failure occurs is defined as the *Etest open margin (*or *Etest short margin)* and can be broken down using **Eq.(2.1)** and **Eq.(2.2)**, for meanders and fork-forks, respectively. These e-test margins can be written as the difference between (1) the maximal achievable margin (*Design margin*), i.e., the margin obtained at zero space error, and (2) the $SE_{max}$ budget from **Eq.(1)**, offset by a "snapping" term (*S.O.*), which is fixed by the process, to first order.

$$Etest\ open\ margin_{meander} = Design\ margin\ - SE_{max}\ - S.O.\ (2.1)$$

$$Etest\ short\ margin_{ForkFork} = Design\ margin\ - SE_{max}\ + S.O.\ (2.2)$$

The *Design margin* term is calculated as the distance between the block and trench edges for the nominal block offset on design, as shown in **Fig. 4**. The *S.O.* term refers to a certain space CD which leads to a trench failure before the block tip reaches the line edge due to etch loading effects.

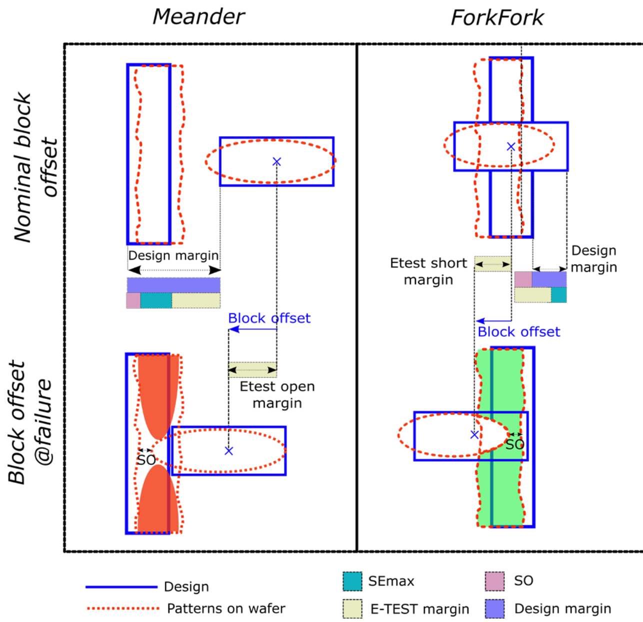



**Fig. 4.** E-test open/short margin.

The *Etest open margin* is therefore offset in magnitude from the $SE_{max}$, but in a 1:1 relationship with $SE_{max}$; Thus, a 1nm larger $SE_{max}$ will result in a 1nm smaller *Etest open margin*.

The electrical failure mode of fork-fork structures is opposite to that of the meander structures. Considering the block-to-line space is gradually offset in the X direction by 1nm block offset steps, beyond a certain block offset, the blocks no longer cut the middle M1 line correctly, and both sides of the line are now shorted as shown in **Fig. 4**. Each series of 24 structures with different block offsets yields one electrical margin datapoint, defined as the block offset at which the open/short transition takes place. For this use case, this transition is generally sharp (its width is smaller than the block offset step).

### C. *Inline direct SEM Metrology*

Direct SEM line to block space measurements were carried out after the opening of the SOC material of the block process. At this process step, the block patterns are still visible on top of the bottom grating which allows to directly measure the SEM block-to-line space (edge to edge distance) in between the two layers, as indicated by the red arrow in **Fig. 5**. The measurements were performed using a Hitachi CDSEM. the block-to-line space was reported for every individual block within the image field of view in the first array of the e-test series, where the block offset, is set to 0nm by design.

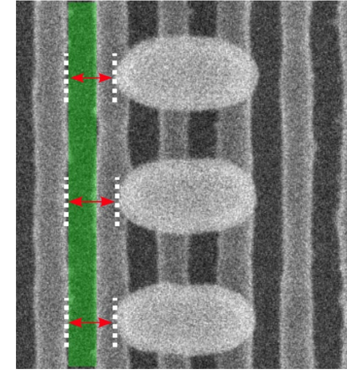


**Fig. 5.** SEM image post SOC etch at a 0 nm block offset.

The trench colored in green corresponds to the conductive metal line post metal fill. A sparse sampling was used to assess cross wafer variation; to derive the mean block-to-line space from SEM images, the spaces from 32 blocks visible on each micrograph were averaged.

### D. *Voltage-contrast e-beam metrology*

Local SE variation was extracted from voltage contrast structures using an inline metrology HMI eP5 e-beam tool. The principle of VC measurement can be found in [16]. The VC arrays are composed of a set of 39 8x8µm modules (clips), containing each 1200 active block units with identical block placements (**Fig. 6(a) & 6(b)**). The drawn block-to-line separation changes in 1nm steps from array to array and varies across a 39nm-wide range. An 8µm field-of-view (FOV) image is acquired on every clip from a set using a special VC-optimized beam. As shown in **Fig. 6(c)**, the lower part of the active line appears dark on the e-beam image when the block fully cuts the line. On the other hand, the whole line segment appears bright when the block only partially cuts the line (**Fig. 6(d)**). When the blocks are centered (block offset 0nm) by design, all the line segments are completely cut, and therefore dark (**Fig. 6(e)**) Considering that the block-to-line separation is gradually offset in the X direction, beyond a certain block offset, some blocks will start to cut the active line, as shown in **Fig. 6(f)**.

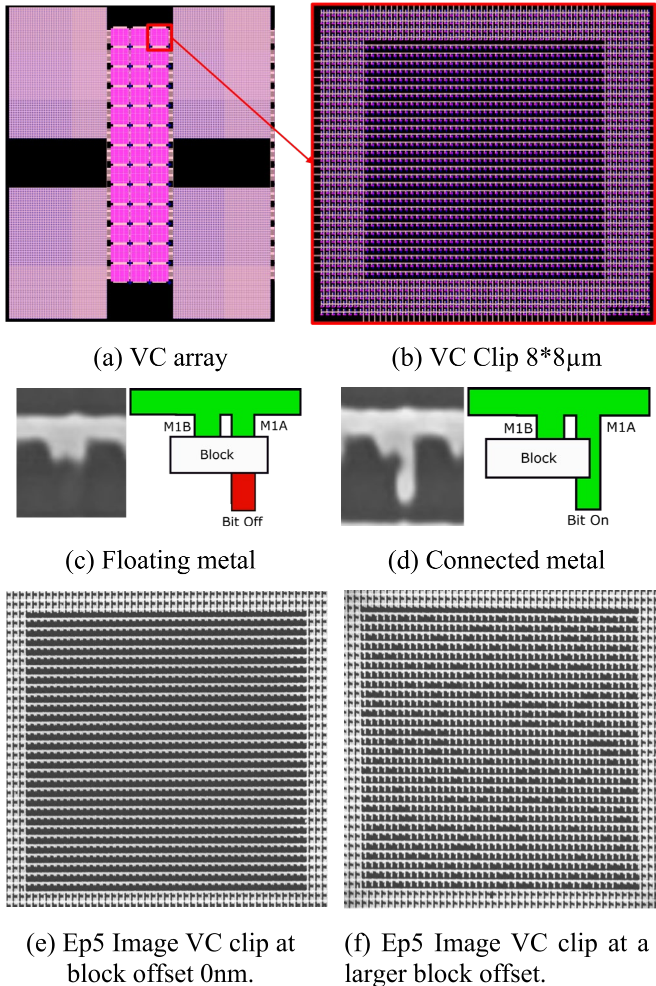



**Fig. 6.** Principle and design of voltage contrast arrays.

The VC proxy yield, which is defined as the ratio of the number of "failing" blocks (bright line segments) over the total number of active block units, is directly linked to the local SE distribution, and can be plotted per field as shown in **Fig. 7.** An automatic image post-processing algorithm was developed to assess the VC yield.

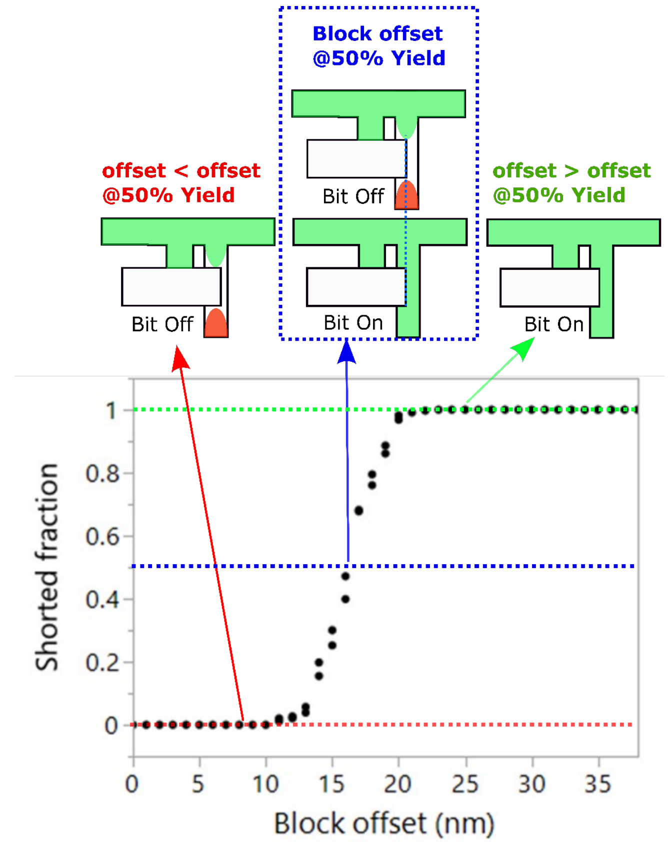



**Fig. 7.** VC proxy yield as a function of block offset.

From this curve, the local component of the SE, $\sigma_{LER(VC)}$, is extracted from the variance of the cumulative error distribution function that best fits the VC yield curve. The global component of the SE (CD/overlay) can also be extracted from the data and correspond to the block offset value at a 50% VC yield threshold.

## III. Results and Discussion

### *A. SEM block to line space metrology*

**Fig. 8** shows the fingerprint of the SEM block-to-line space data of the FEM wafer. This space corresponds to the geometrical distance from the left tip of the block to the left edge of the neighboring trench as indicated by the red arrow in. **Fig.5**. The block dimensions and local CD variation both vary with imaging conditions. A higher exposure dose shortens the block length, leading to a higher block-to-line space. A Bossung behavior can be noticed in the Y direction as the defocus increases from best focus condition set at 0.07 um. Note that the SEM block-to-line space data plotted here are averaged over a SEM image from a sample of 32 blocks. The local space components therefore act as a zero-mean "noise term" added to the average space, with a variance suppressed by a factor $1/\sqrt{32}$.

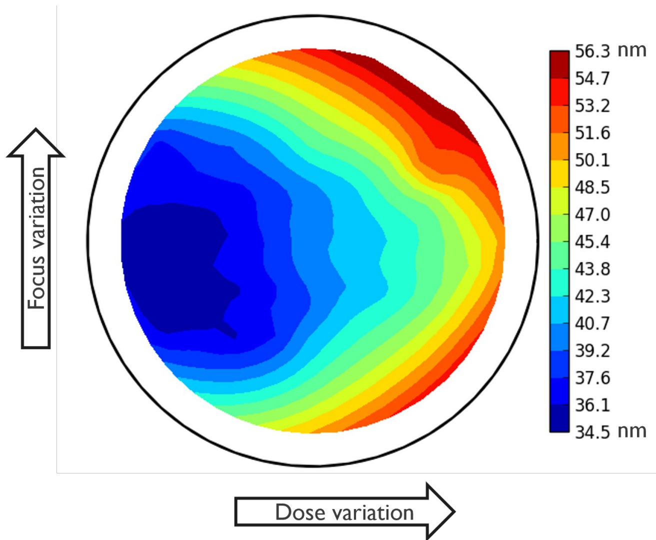



**Fig. 8.** SEM block-to-line space at a 0 nm block offset

*B. SEM space metrology to e-test margin correlation*

To investigate the correlation between the SEM block to line space and the electrical open margin for the e-test structures, local contributors must be added to the SEM data discussed in the previous section. The local contributors to the SE could not be extracted directly from the SEM data (because too few blocks are imaged). Thus, these local effects were extracted using the end of line VC metrology. Using **Eq.(3)**, the *Reconstructed open margin* is built from the SEM and VC metrology data on the meander devices.

$$Reconstructed\ open\ margin_{meand} = SEMspace_{blocktoline} - 4.5 \times \sigma_{LER(VC)} - S.O. \quad (3)$$

The $SEMspace_{blocktoline}$ space term extracted from CDSEM measurements at SOC open step (Section III.A) contains the global contributors to the $SE_{max}$ budget, and hence accounts for overlay, CD uniformity and mean CD offset from design CD. The second term is the local contribution to the extreme-value SE and depends on $\sigma_{LER}$, defined as the RMS average of the block LCDU, block local placement error and of the trench LER. This term was not directly extracted from the SEM data on the same device as for the SEM space data. The $\sigma_{LER(VC)}$ term was extracted from the VC yield statistics, as described in Section II.D. A correction factor was applied to account for the difference in pattern density, optical proximity and etch loading effects in between the meanders and the VC features.

The coefficient $n$ in **Eq.(1.2)** of the local SE term can be estimated from the extreme value distribution. The mean of the maximum for a meander array size of $1.82 \times 10^5$ active block units is estimated to be 4.5 according to the Fisher-Tippett-Gnedenko formula [18]. This coefficient is representative of the failure opportunities of the meander device. The process "snapping effects" are assumed to contribute a constant offset ("*S.O.*") to the SE budget. As shown on **Fig. 9**, the trench failure is expected to happen before the block tip reaches the line edge which account for the snapping term.

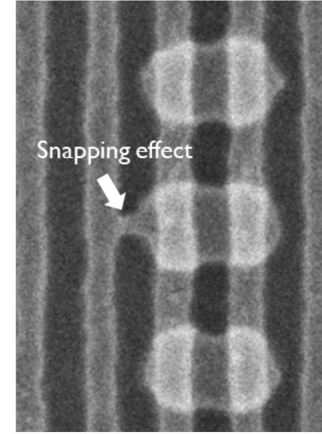



**Fig. 9.** Post TiN etch SEM image of a meander device.

In **Fig. 10**, the measured e-test open margin measured on the meander devices is plotted as a function of the *Reconstructed open margin* (**Eq.(3)**).

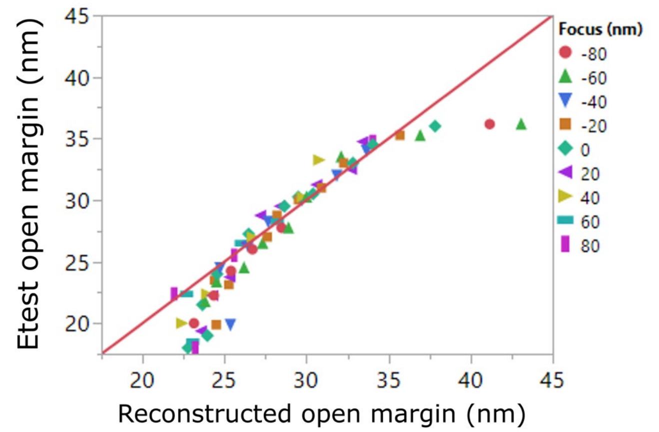



**Fig. 10.** *Etest open margin* as a function of the *Reconstructed open margin*

The S.O. constant offset is considered as a fitting parameter having a constant value of 2.8nm. The local SE sigma term contributes to the total *Reconstructed open margin* within a range from ~2nm to ~2.5nm depending on imaging conditions. A large part of the modulation results from the *SEMspace* term, which varies with the block CD through the FEM and contributes 34-56nm to the total reconstructed budget, as discussed in Section III.A.

The data close to the center of the SE distribution shows a good match between the *Reconstructed open margin* and the measured *Etest open margin*. In this range, we also observe that the focus and dose variations are captured by the proposed model. The e-test datapoints that deviate from the *Reconstructed open margin* predictions correspond to the wafer edge and can be explained by a CD fingerprint effect. Indeed, the direct SEM space data were taken at an intermediate process step (SOC open), which has its own process fingerprint with a center-to-edge variation, whereas the electrical open margin data were measured after metal CMP. An inversion of the center-to-edge variation of the trench CD was observed as the pattern is transferred into the low-k dielectric. This was also confirmed by resistance measurements after polish.

### C. Space error Formula validation

The previous section validates the correlation between SEM and *Etest open margin*, but the modulation observed in **Fig. 10** results in large part from a change in block CD, determined by the exposure dose and focus in the FEM. The local SE term in **Eq.(3)**, is small relative to the total range of the edge-to-edge margin from line to block, which makes the method relatively insensitive to the coefficient of $\sigma_{LER(VC)}$. To verify this coefficient more accurately, a method relying solely on data obtained after metallization was used. To this end, the end of *line Etest short margin* data from fork-fork structures were compared to the local and global SE components extracted from the VC features, as described in **Eq.(4.1)**. The e-test fork-forks and the VC arrays have a similar failure mode, as described in **Fig. 2(b)** and **Figs. 6(c) & 6(d)**.

$$Etest\ short\ margin_{ForkFork} = Block\ offset_{@50\%\ VC\ Yield} - n \times \sigma_{LER(VC)} \tag{4.1}$$

therefore,

$$SEresiduals = Block\ offset_{@50\%\ VC\ Yield} - Etest\ short\ margin_{ForkFork} = n \times \sigma_{LER(VC)} \tag{4.2}$$

where $n$ is a fitting coefficient. The global SE component (CD/OVL) is extracted from the VC yield curve as described in Section II.D and is defined as the block offset at 50% VC Yield. Considering the extreme-value SE formula from the generalized model, the local SE term can be looked as a residual and its coefficient can be extracted from the data as described in **Eq.(4.2)**. **Fig. 11** shows the *SEresiduals* as a function of $\sigma_{LER(VC)}$.

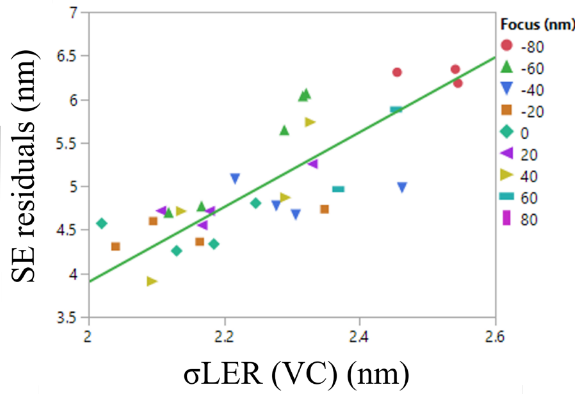



**Fig. 11.** *SEresiduals* as function of $\sigma_{LER(VC)}$.

In this experiment, the local SE sigma varies from ~2nm to ~2.5nm since block local CD variability changes with imaging conditions (*e.g* Focus & Dose variation). Through this range, the *SEresiduals* data is consistent with a 4.3:1 slope. Here, the extreme-value local coefficient depends on the failure opportunities per device and expected to be 4.3 as fork-fork arrays contain $9.1.10^4$ active block features according to the Fisher-Tippet-Gnedenko formula. This coefficient is slightly smaller than the one expected for the meander structures since the fork-fork structures have fewer failure opportunities.

## IV. CONCLUSION

A process for the characterization of SE sensitive electrical devices was demonstrated. This process, based on a LELE and block patterning approach, allowed the validation of inline SEM margin measurements by comparing the latter with an end-of-line, yield-based, SE metric. Near the wafer center, we observe a good match between the SE predicted from the weighted sum of the local and non-local terms, and the measured *Etest open margin*. A model was also proposed to explain the deviations from the SE prediction observed at the wafer edge. Local SE variation was successfully extracted using voltage contrast structures, and from inline metrology statistics. An experimental validation of the local (stochastic) term of the extreme-value SE formula was performed by showing that the coefficient of this local term, as fitted from the data, was consistent with the extreme-value statistics calculated for the e-test structures.

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