Electrostatic discharge robustness of amorphous indium-gallium-zinc-oxide thin-film transistors

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Abstract – The thin-film-transistor (TFT) technology has attracted significant attention in account of the possibility to manufacture transistors on large and flexible substrates, at low processing temperatures and at a low cost. Next to the well-established amorphous silicon TFT technology used mostly for displays, the amorphous Indium-Gallium-Zinc-Oxide (IGZO) and Indium-Tin-Zinc-Oxide (ITZO) materials offer a higher current conductivity and thus a better performance. This makes them interesting candidates for TFT integrated circuits also beyond displays. However, integrated circuits can be easily damaged by electrostatic discharges (ESD) and require integrated protection solutions. To find possible vulnerabilities and solutions, this paper analyzes ESD robustness of two IGZO and one ITZO TFT device architecture.

Keywords – Electrostatic Discharge, ESD, Thin-Film Transistor, TFT, Indium-Gallium-Zinc-Oxide, Indium-Tin-Zinc-Oxide, IGZO, ITZO

1 Introduction

The main application of Thin-Film-Transistor (TFT) technology today is in flat-panel display production. Since TFTs can be produced on transparent and flexible materials using a very low thermal budget, this technology started appearing in applications beyond displays. Two examples are the Internet of Things (IoTs) and wearable electronics [1, 2, 3] in form of flexible application-specific integrated circuit (ASIC) designs.

Electrostatic discharge (ESD) events are a common reliability concern. Most ESD events observed during production and assembly, both for ASICs and displays, can be prevented using well established ESD control practices [4, 5]. However, the only solution to the ESD threat after production is ESD protection circuits integrated into the ASIC itself. Such integrated protection solutions are even more important for those ASICs with input/output pins exposed to the user. For displays, in-pixel ESD protection circuits may not be necessary, still, protection circuits are introduced at the peripheral driving circuits. However, with integration of driver and control circuits into the display panel itself, integrated ESD protection will be necessary [6].

The Thin-Film-Transistor (TFT) technology that uses the amorphous Indium-Gallium-Zinc-Oxide (IGZO) material as semiconductor is a promising candidate for the flexible ASIC application. Compared to the more commonly used amorphous silicon, IGZO produces a higher field-effect current density [1, 7]. Still, being a relatively young technology, publications on IGZO TFT reliability and ESD performance are scarce. Some published works on the topic include [8, 9, 10]. Knowledge on reliability for amorphous Si is more abundant [11, 12, 13, 14, 15, 16].

In this work we first asses the sensitivity of a pixel circuit and a display to ESD stress. We use the Transmission Line Pulser (TLP) HED-T5000 by Hanwa Electronic to test for robustness to ESD events. Afterwards we study the ESD protection capabilities of diode connected transistors, using three different TFT architectures based on the IGZO material.

Compared to our previous publication [17], this paper includes TLP measurement results on devices with an added ITZO cap layer and circuit measurements that asses sensitivity to ESD stress that have not been published before.

2 Measurement methods

Electrostatic discharge (ESD) events appear regularly in the environment. Part of these events can be replicated in laboratory using the Human Body Model (HBM). However, the HBM ESD tester produces a relatively complex waveform and is mostly used to perform pass/fail tests. The Transmission Line Pulser (TLP) is the *academic* equivalent of the HBM tester and is mostly used for in-depth analysis of ESD protection devices and circuits. In this work we mostly use the TLP setup (Figure 1) and the HBM tester just to correlate TLP measurements to a real-world scenario.

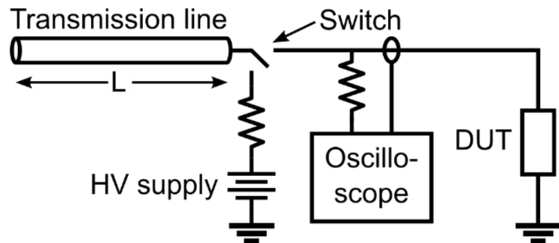

Figure 1 – Simplistic schematic of the Transmission Line Pulser (TLP) measurement setup.

The TLP instrument uses transmission lines charged to a high voltage to produce rectangular pulses. In this work we have used 100 ns long pulses with 2 ns rise and fall times in all cases. These pulses are released to the Device Under Test (DUT) and their voltage and current are measured with an oscilloscope. Depending on the DUT load, according to the transmission line theory, the pulse voltage or current can be reflected or absorbed. We always report the measured voltage V_{TLP} and current I_{TLP} values.

The HBM tester uses a charged 100 pF capacitor which is then discharged through a 1.5 kΩ resistor to the DUT.

A DC characteristic of the DUT is measured before the first and in between each consecutive pulse, both for TLP and HBM. We report only a single value from the measured characteristic as function of V_{TLP}, often named I_{leak}, even though a DC sweep from -5 V to +2 V in forward polarization is performed. I_{leak} is the value measured for the -5 V bias.

The single TFTs used in this work to assess the ESD protection capabilities have been measured in the diode-connection, as depicted in Figure 2. In both cases, for single and dual-gate devices, all gate terminals have been connected together with the drain terminal. TLP and DC characteristics have been measured from the drain towards the source terminal, thus in forward polarization. Diode-connected TFTs under ESD stress in reverse polarization have been shown ineffective [9] and are not studied in this work.

The pixel select circuit (Figure 3) has been chosen to measure the TFT technology sensitivity to ESD events. The circuit we used has six ports: one select port labeled *SEL*, one calibration port *CAL*, two data ports *DATA1* and *DATA2* and two testing ports *INT1* and *INT2*. Since the testing ports would not be present in a display, the select *SEL* port has been chosen as the weakest link in the event of an ESD. Therefore, the TLP stress has been applied to the *SEL* port while the *DATA1* and *INT1* ports have been grounded. For the DC measurement, the gate voltage (port *SEL*) has been swept from -2 V to +2 V, the drain bias (*DATA1*) has been set to +2 V and the drain current (*DATA1*) has been measured.

Similarly, for the display, TLP stress has been applied to the select (*SEL*) lines. In this case, the bias contact has not been used, so the *DATA* lines have been floating. The ground pin has been connected to the ground port of the display.

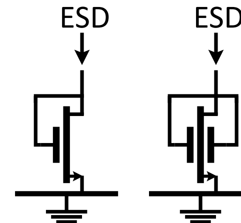

Figure 2 – Diode connected TFT.

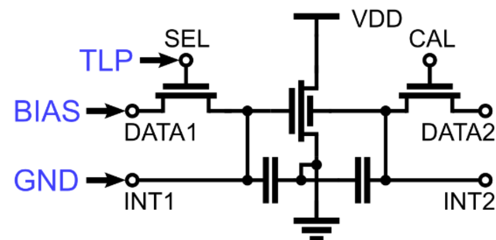

Figure 3 – Schematic of the 3T2C pixel circuit used in TFT displays. The pixel photodiode is not shown.

3 Assessment of TFT circuits sensitivity to ESD

The following measurement results have been acquired by applying a linearly increasing TLP stress to a 3T2C pixel circuit and a prototype

display previously described in [18, 19]. The measurement setup has been explained in Section 2.

The TLP stress can significantly reduce the driving capabilities of the select TFT in the pixel circuit, as depicted by a degrading DC characteristic in Figure 4. The rightmost point from Figure 4 is extracted and plotted against the measured TLP voltage (V_{TLP}) in Figure 5. The breakdown point is found to be at about 120 V and is observed as a sudden drop in current I_{DATA}.

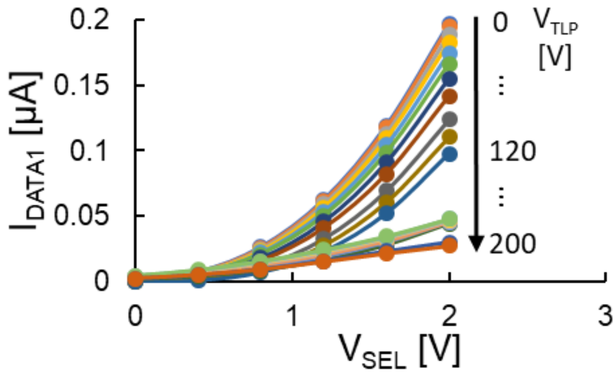

Figure 4 – I_d-V_g curves measured on the *select* transistor in the 3T2C pixel circuit. Clear degradation can be observed with increasing TLP stress until breakdown at about 120 V.

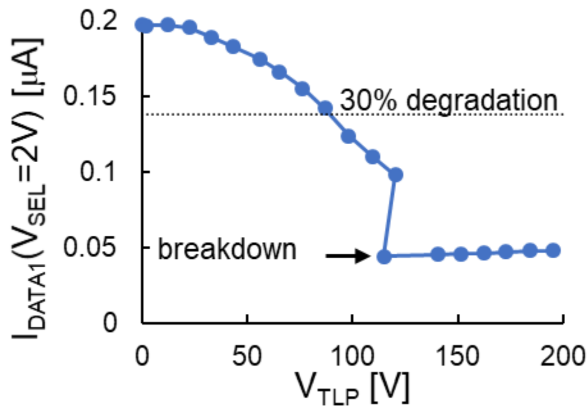

Figure 5 – Drain current of the *select* transistor in the pixel circuit as function of V_{TLP} stress.

However, before breakdown, the select transistor driving performance is degraded significantly. This can most easily be seen in Figure 5 where the drain current is 30% lower after TLP stress of roughly 80 V. Just before breakdown, the drain current is 50% lower than in an unstressed TFT.

We have taken photographs of the pixel circuit after breakdown to learn more about the breakdown mechanism. Unfortunately, the damage to the TFT itself is not visible under the optical microscope that we used. Continuing with TLP stress beyond the breakdown point and up to a V_{TLP} of about 200 V has produced visible damage to the dielectric separating two metal layers, as depicted in Figure 6. Even at this point no visible damage to the TFT under stress has been observed.

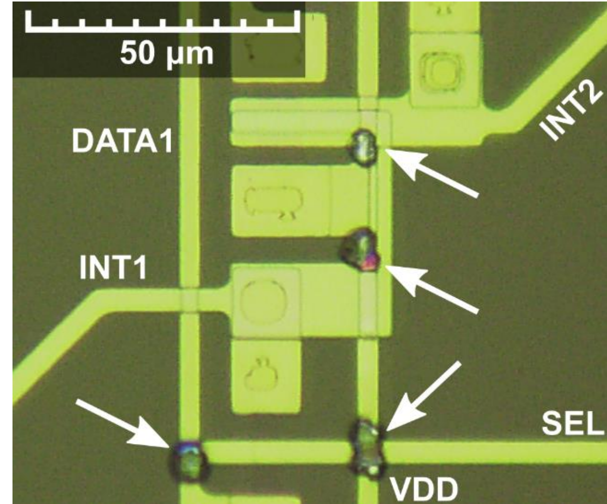

Figure 6 – Photograph showing a part of the 3T2C pixel circuit after TLP stress beyond breakdown (V_{TLP} ≈ 200 V). Damaged points indicated with arrows are intersections of metal lines. No damage is visible on the transistors themselves.

To verify if the observed degradation can disrupt the functionality of the circuit, we have applied TLP stress to a full prototype display which contains thousands of equivalent pixel circuits.

For this experiment, some dead pixels were already present prior to ESD testing. As noted in Figure 7, three lines have been selected and stressed with increasing TLP pulses amplitudes. Lines *n* and *n+2* have been stressed with TLP with maximum amplitude of 26 V and 24 V accordingly. After the stress, line *n* still performs well while line *n+2* is dark, meaning that it has been broken.

Since dielectric breakdowns have in general a distributed nature and are strongly affected by process-variability and defects, it is expected that one line in the display can survive a higher stress then the other. Interestingly, even with TLP stress of about 215 V, which is well beyond the expected breakdown point, applied to line *n+4*, the neighboring lines have not been affected. This indicates that applying TLP to a

display remains localized to the line under stress.

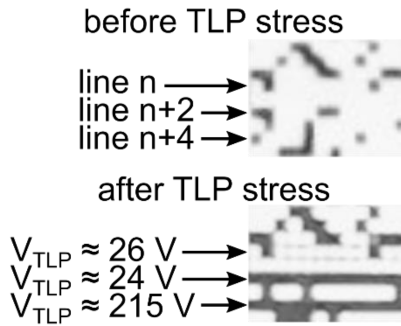

Figure 7 – Photographs of a small portion of a prototype TFT display before and after TLP stress.

To conclude, pixel circuits and displays produced in the IGZO TFT technology can be very sensitive to ESD. Even though hard breakdowns are expected at stresses above 100 V for standalone circuits, system level breakdowns are observed already at V_{TLP} of 24 V. We presume these early breakdowns of display lines are explained by the degradation of TFTs already at lower stress levels.

4 Thin-film transistor technologies

Several TFT technologies based on the Indium-Gallium-Zinc-Oxide (IGZO) material exist today. To investigate the impact of different TFT architectures on ESD performance, three different TFT technology flavors have been analyzed in this paper.

The first one is the top gate self-aligned (SAL) technology depicted in Figure 8.a. Compared to the bottom gate technology fabricated using the etch stopper layer methodology, SAL has a lower parasitic capacitance and a higher scalability potential [1].

The second flavor is an extension of the SAL technology including an additional back gate resulting in a dual-gate self-aligned (DUGA) technology. The extra bottom gate can be used to control the threshold voltage of the TFT and is a very interesting feature for circuit design in this unipolar technology family. Other advantages of DUGA over SAL, such as a higher drive current and a steeper subthreshold slope, are better described in [20]. Figure 8.b depicts a cross-section of the DUGA technology.

The third technology flavor is the same as DUGA, except for the dual-layer semiconductor Indium-Tin-Zinc-Oxide (ITZO) and IGZO (Figure 8.c). TFTs with this IGZO-ITZO combination have proven to have a higher current conductivity compared to the ones with only IGZO [21].

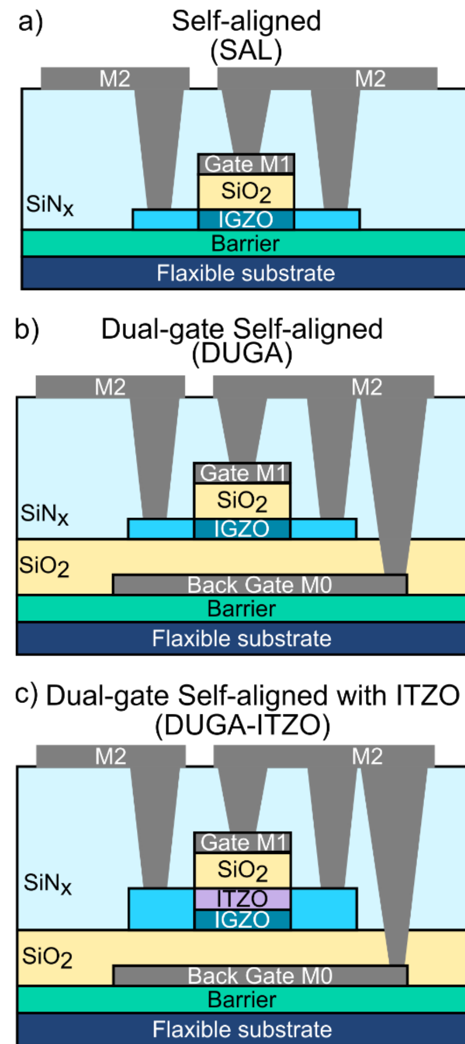

Figure 8 - Cross-sections of the three IGZO TFT technology flavors used in this paper: a) the self-aligned top gate only process (SAL), b) the dual-gate process (DUGA) and c) the DUGA with the added ITZO semiconductor (DUGA-ITZO).

5 ESD measurements of diode connected TFTs

Previous works from our group that have reported similar measurements include [8] and [9]. The main concern was a negative threshold voltage and significant leakage currents. The technology has improved significantly since then. Positive threshold voltages and a reduced leakage at zero bias can be achieved [21]. In this paper, the ESD performance of dual-gate

devices with the dual-layer IGZO-ITZO has been measured according to Section 2 and presented for the first time. All data in this section has been measured on single diode-connected TFT devices, as depicted in Figure 2.

The breakdown criterium has been defined as an increase in the leakage current I_{leak} of at least a factor of two in all following measurements, or, alternatively, a significant increase in I_{TLP}. The voltage V_{TLP} and current I_{TLP} values measured in the last point before breakdown are labeled as V_{t2} and I_{t2} respectively. Another value reported in this paper is the dynamic resistance R_{on} of the DUT during TLP. R_{on} is calculated from the V_{TLP} and I_{TLP} characteristic.

5.1 Self-aligned (SAL) top gate TFT

The TLP measurement results of the SAL devices with two different gate lengths (2 and 5 µm) are depicted in Figure 9. The I_{t2} value in both cases is about 30 mA. The R_{on} roughly doubles for the longer device from 1 to 2 kΩ. These values are comparable to previous measurements [8, 9], except here I_{leak} is significantly lower.

The measured I_{leak} degradation (see Figure 9) for the device with L of 2 µm is not taken as a failure. Such degraded devices continue to offer efficient ESD protection. Only a significant increase in I_{leak} is considered a failure.

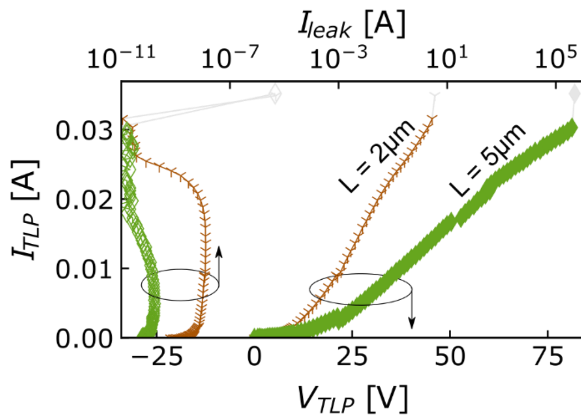

Figure 9 – TLP measurement results for two SAL TFTs with different gate lengths and width equal to 100 µm.

5.2 Dual gate (DUGA) TFT

DUGA devices can be manufactured both as dual-gate and single-gate devices with only the top gate. In this experiment, we have used both dual-gate (DUGA-DG) and single-(top-)gate (DUGA-SG) TFTs, which resemble the SAL devices.

The TLP results from the DUGA-SG devices with four different gate lengths are depicted in Figure 10. The ESD performance of the DUGA-SG devices is worse than SAL TFTs. The I_{t2} values are ~30% lower. The V_{t2} is comparable. This suggests a lowered thermal dissipation caused by introducing the SiO_2 back-gate dielectric on top of the Al_2O_3 barrier. Indeed, the thermal conductivity of SiO_2 is significantly lower compared to Al_2O_3, implying a weaker self-heating effect of the SAL device compared to the DUGA-SG device. Please note that the higher leakage current for the device with gate length L = 5 µm in Figure 10 is an exception. We have observed other equivalent devices with lower leakage values. As the DUGA-SG devices are shown here mostly for facultative reasons and are not the first choice for ESD protection circuits in the DUGA technology, we did not further investigate this exception.

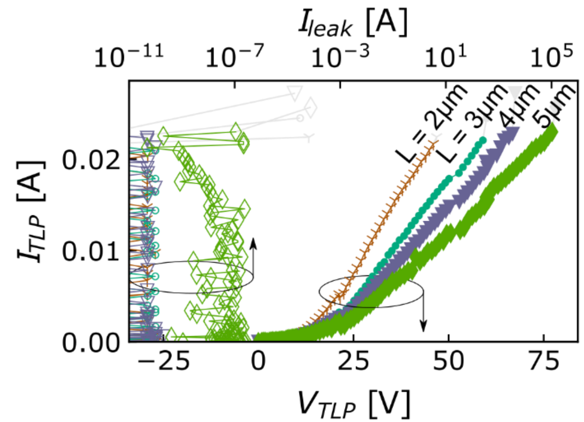

Figure 10 – TLP measurement results for four DUGA single-gate (DUGA-SG) TFTs with four different gate lengths and width equal to 100 µm.

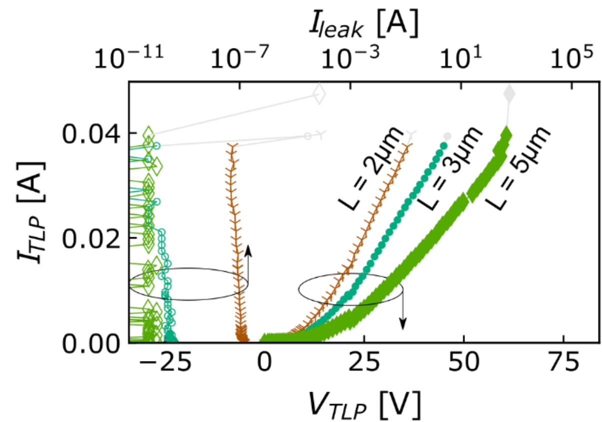

Figure 11 - TLP measurement results for three dual-gate DUGA-DG TFTs with three different gate lengths and width equal to 100 µm.

The dual-gate DUGA-DG device, when connected in diode mode, shows a significantly improved performance compared both to SAL and DUGA-SG devices, as depicted in Figure 11. As expected, DUGA-DG TFTs have a higher drive current that translates into a lower R_{on}. Compared to SAL, the I_{t2} is 25% higher and the V_{t2} is 25% lower. Even though the DUGA active region is thermally better insulated than the SAL, a higher drive current compensates for this. Finally, DUGA-DG devices with an I_{t2} of about 40 mA are about 30% better than SAL.

5.3 Dual-gate DUGA-ITZO TFT

The dual-layer ITZO-IGZO semiconductor yields transistors with increased current driving capabilities, implying an improved ESD performance of diode-connected TFTs. Even though they have comparable V_{t2} values as DUGA-DG, their I_{t2} is increased by 25% to 50 mA on average, as can be seen in Figure 12.

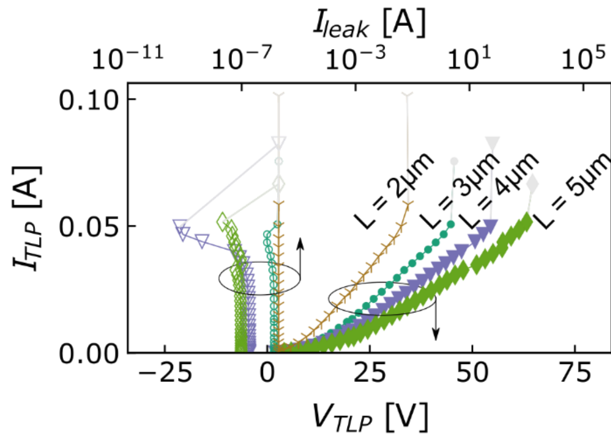

Figure 12 - TLP measurement results of DUGA-ITZO TFTs with four different gate lengths and width equal to 100 µm.

5.4 Summary of technology options in TFT

To summarize the TLP measurement results, we compare the $I_{t2}V_{t2}$ product plotted against the TFT gate area, as shown in Figure 13. In this way we can disregard the differences in the field-effect mobility process variations between the DUGA and SAL technologies. The value of $I_{t2}V_{t2}$ is equivalent to the power dissipated in the transistor active area.

Figure 13 confirms that the single-gate DUGA (DUGA-SG) transistors are the worst performing, while the DUGA-ITZO transistors are the best option for ESD protection circuits.

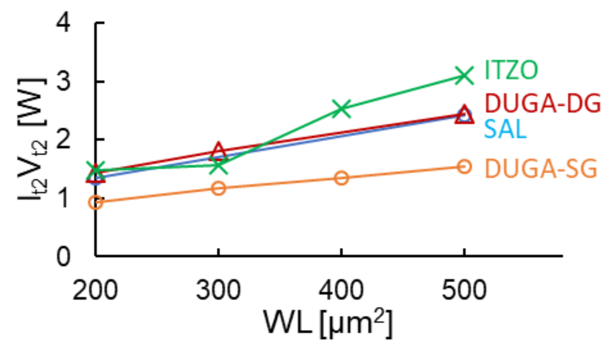

Figure 13 - Equivalent electric power delivered to the TFT before failure.

An abrupt increase of the leakage current has been taken as failure criterium. The I_{t2} and V_{t2} values, which represent the TLP current and voltage, are equal to the last measured point before failure.

5.5 HBM measurements

To offer a more comprehensible view on the ESD performance of diode-connected TFTs, we have performed HBM measurements on the DUGA-ITZO devices. Results are presented in Figure 14. HBM measurement results, V_{HBM}, are compared to TLP results by multiplying I_{t2} with the system resistance R. R is equal to the sum of the device resistance R_{on} and the HBM to TLP tester correlation resistance, usually 1.5 to 2 kΩ. R_{on} is calculated from the measurement data as V_{TLP}/I_{TLP} and is included here because for these devices it is significant, in the range from 400 to 800 Ω. Normally, for highly efficient ESD devices, this resistance would be significantly lower and thus neglected.

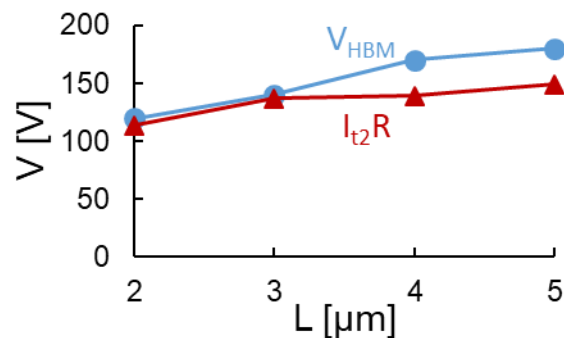

Figure 14 – HBM measurement results, V_{HBM}, of DUGA-ITZO TFTs with four different gate lengths and width equal to 100 µm. HBM results are compared to TLP by using the I_{t2} values multiplied with R, the summed device R_{on} and the HBM-to-TLP correlation resistance of 2 kΩ.

Three reasons exist why in this work we use 2 kΩ to compare I_{t2} to HBM and also why there is a slight difference between the TLP and HBM data in Figure 14. Firstly, the HBM measurement step is 10 V while the TLP step is 1 V in the data presented here. Furthermore, the small voltage steps in the TLP measurement result in an increase of the cumulative stress on the device compared to the HBM tests. Even though cumulative damage is not considered in this paper, it might play a role in this comparison. Secondly, device to device mismatch is not negligible in the samples we measured. This is best observed in the leakage currents which can differ from device to device and do not always scale as expected (see Figure 10 as example). Thirdly, our calculation of R_{on} from V_{TLP} and I_{TLP} data is sensitive to noise and the chosen observation window. This could have also introduced some mismatch.

Nevertheless, the data presented in Figure 14 matches well with difference within 15 % and allows us to conclude that TLP measurements of TFT devices can be correlated to HBM measurements.

6 Discussion on thermal failure under ESD stress

As already hinted in the previous section, self-heating effects are considered to be the main cause of breakdown in ESD protection devices. Indeed, when semiconductor devices conduct current, they also generate heat. To provide adequate protection, ESD devices need to divert a very large amount of charge in a very short time, thus generating a lot of heat. To study both the thermal and electrical properties of the selected IGZO-based TFT devices, we employ DECIMM, an industry-standard mixed-mode finite elements TCAD simulator [22].

6.1 TCAD analysis

To reproduce the TLP measurements as closely as possible, we used 100 ns wide pulses generating approximately 20 mA of current in our TCAD simulations. The simulated transistor dimensions match the measured ones with a width of 100 µm and length of 5 µm. Even though the thermal properties of a low thermal budget SiO_2 and Si_3N_4 layers are not completely certain [23], our simulations are sufficiently close to the measurements. We assume the main heating source of the TFT is the active IGZO region found underneath the top gate.

Figure 15 depicts a 2D TCAD simulation of a dual-gate DUGA transistor (Figure 15.a) at the end of a 100 ns pulse. The simulated thermal profile (Figure 15.b) shows that the heat generated in the active region mostly spreads vertically toward the gates and much less laterally towards the source and drain. TCAD predicts temperatures of 550 K located in the active region.

The same simulations have been repeated for the single-gate DUGA (DUGA-SG) and SAL transistors (Figure 16). We find that the DUGA-SG structure heats up more at the end of a TLP pulse. In comparison, the DUGA-DG dissipates more thermal energy to the additional bottom metal gate. However, the SAL structure dissipates more heat to the underlaying Al_2O_3 barrier layer, since it has no SiO_2 layer immediately under the IGZO channel. Note that SiO_2 has a lower thermal conductivity than Al_2O_3. At least qualitatively, these simulation results agree with measurement results in Figure 13.

The SAL transistor is significantly slower to heat up at the beginning of the TLP pulse, due to the proximity of the Al_2O_3 barrier which has a higher thermal conductivity than SiO_2. From [24, 25] we know that SiO_2 has a thermal conductivity between 1.3 and 1.5 W/(m·K), lower than Al_2O_3 with typical values between 12 and 38.5 W/(m·K), although values down to 4 W/(m·K) have been reported for thin layers [28]. The close proximity of the IGZO active area and the Al_2O_3 barrier helps to reduce self-heating in SAL TFTs.

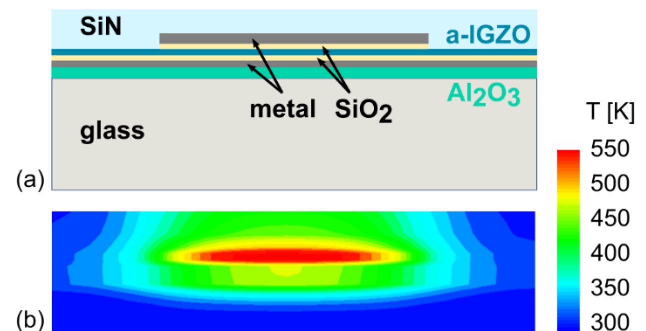

Figure 15 – The TCAD simulation a) structure (example for the dual gate DUGA TFT) and b) result of self-heating at the end of a 20 mA 100 ns TLP pulse.

DUGA-ITZO devices are not included in this discussion because they are structurally

identical to IGZO (DUGA) devices. It is not the scope of this section to study thermal properties of IGZO and ITZO, but to compare the three different structures. Also, the ITZO layer is very thin and we do not expect any significant difference in thermal conductivity compared to IGZO devices.

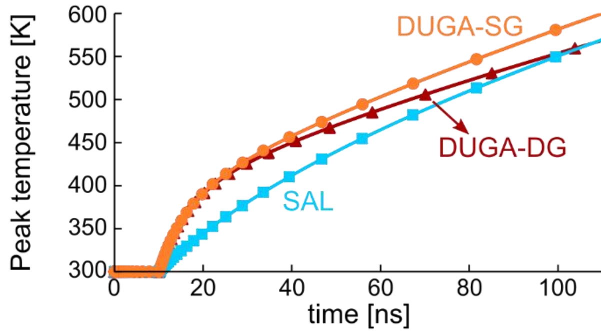

Figure 16 – The temperature peak in the active IGZO region during the 100 ns TLP pulse for SAL, DUGA-SG and DUGA-DG transistors.

6.2 Thermal hot spot

In the attempt to learn more on the location of the thermal breakdown in the IGZO-based TFTs, we have performed more TLP measurements on devices with a varied spacing between the gate and source/drain contacts. Figure 17 depicts a cross-section of a DUGA transistor indicating to this spacing as *SP*.

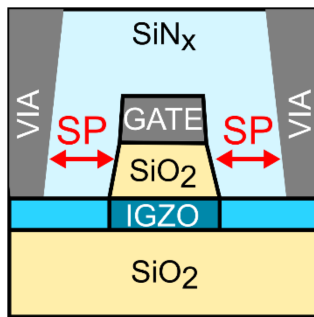

Figure 17 – The cross-section of a dual-gate DUGA transistor indicating the spacing between the gate and the source/drain terminals by *SP*.

Three transistors in diode connection with SP equal to 3, 5 and 15 µm have been measured with the TLP setup. Smaller transistors have been used in this case with gates equal to $WL = 15 \times 5\ \mu m^2$. All three have the same I_{t2} and R_{on} values, as depicted in Figure 18. This confirms that no significant correlation exists between SP and the transistor performance. Indeed, the part of the IGZO layer which is not part of the active region under the gate, is doped and highly conductive. From I_{t2}/W scaling in [9], we know that the gate resistance R_g does not affect I_{t2}. The device turns on uniformly along the 100 µm wide channel and the R_g from edge to edge is negligible in terms of ESD performance.

As such, we conclude that gate region is the determining factor for I_{t2}. Finally, while I_{t2} remains constant for increasing L from 2 to 5 µm, V_{t2} increases significantly. As such, the SiO_2 layer under the gate is not the prime cause of failure, since it will be subjected to significantly higher voltage before failure in the $L = 5$ µm device. Consequently, we must assume that the channel-IGZO itself is responsible for the failure.

During visual inspections of the broken transistors from Section 5, we have discovered clear breakdown marks. A photograph taken with an optical microscope indicates these marks in Figure 19. The marks are located at the edge of the gated region. Such failure location can be expected in case of thermal runaway in the TFT channel, leading eventually to the formation of a destructive current filament.

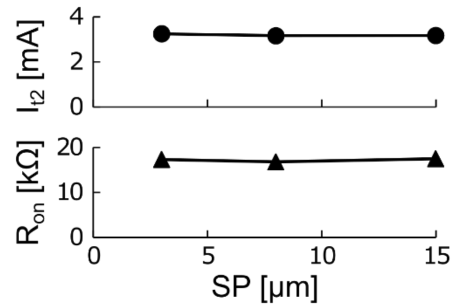

Figure 18 - The source/drain to gate spacing (SP) does not affect the device I_{t2} and R_{on} values.

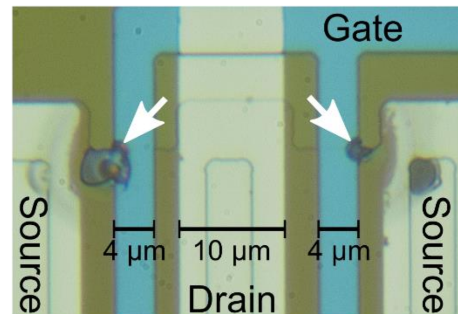

Figure 19 – IGZO TFT with two breakdown points observed after breakdown induced by TLP stress. The gate and drain terminals have been shorted during TLP measurements (see Section 2).

7 Degradation of diode connected TFTs

As mentioned in Section 3, degradation of IGZO-based transistors could be an issue for integrated circuits when ESD stress is applied to the gate terminal. The same is true for integrated ESD protection circuits. In this section we take a deeper look into the degradation effects of the diode connected transistors as function of TLP stress applied to the drain terminal. In Section 5 we have only reported the leakage current I_{leak} measured with a bias of -5 V. Here we also discuss the drive current I_{on} measured with a bias of +2 V. Both are depicted in Figure 20.

For SAL devices, I_{leak} first increases with TLP stress and then decreases beyond the initial value. The increase is negligible for I_{on}, but the degradation before failure is even more significant. Basically, the SAL device completely fails the current driving capability with high TLP stress. Dual-gate devices, both DUGA and ITZO, do not show such behavior. In these cases, the degradation of both I_{leak} and I_{on} is minimal before breakdown.

The major technology difference between dual-gate and SAL transistors is the dielectric on which the IGZO/ITZO layer is deposited. For SAL this is Al_2O_3 and for dual-gate it is SiO_2. A suggestion to explain this phenomenon may lie in the interface between IGZO/ITZO and Al_2O_3, which can be electrically less stable and degrade more severely with stress. It has been observed in advanced CMOS technologies that Al_2O_3 has a stronger charge trapping capability [26]. It has also been reported that Al_2O_3 can have a detrimental effect on the TFT reliability [27].

Degradation of the DC characteristics has been observed under TLP stress prior to failure. Since a substantial increase in leakage current has not been observed in these tests, this degradation is not considered important for ESD applications.

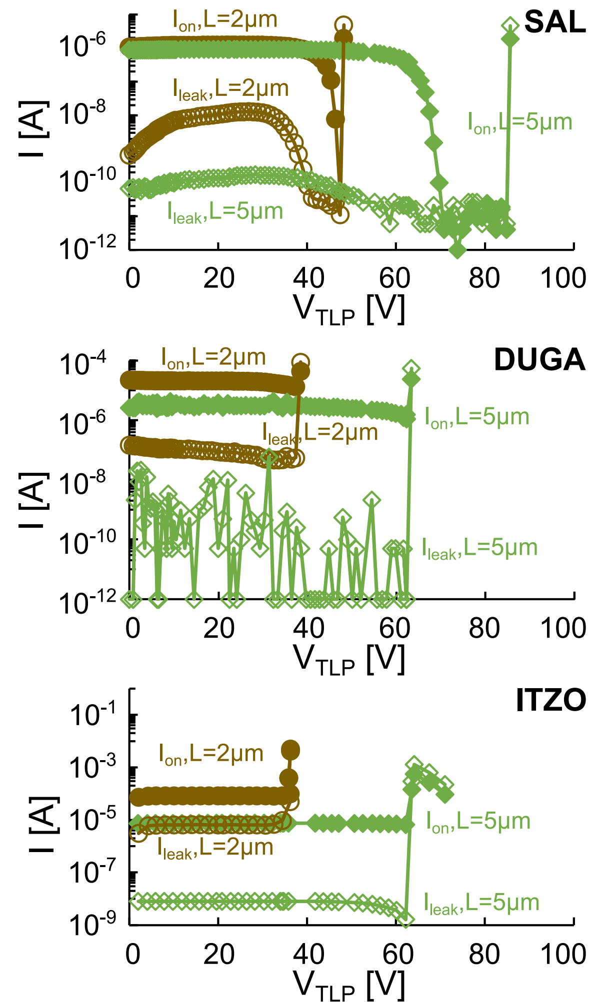

Figure 20 – The *on* current I_{on} measured for V_g = 2 V and the *leakage* current I_{leak} measured for V_g = -5 V. In case of the dual-gate structures, DUGA and ITZO, both gates have been shorted together.

8 Conclusion

IGZO-based thin-film transistor circuits are very sensitive to ESD stress. Pulses with amplitudes of 24 V can break circuits such as displays. Lower stress levels can cause significant degradation. Diode connected transistors are one of the few ESD protection solutions available in the IGZO TFT technology, as there are no junctions present. Among the three technology flavors that we tested, the dual-semiconductor IGZO-ITZO outperforms the SAL IGZO and DUGA IGZO and is the most promising technology in terms of ESD protection performance, thanks to the highest driving current capability.

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