ESD study on a-IGZO TFT device architectures

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Abstract – The indium-gallium-zinc-oxide (IGZO) thin-film-transistor (TFT) technology offers to manufacture transistors on large and flexible substrates at low processing temperatures and at a low cost. However, optimization of ESD protection devices in this technology has not been thoroughly investigated. This paper analyzes the ESD performance of three different TFT device architectures.

I. Introduction

The Thin-Film-Transistor (TFT) technology is mainly used for flat-panel displays today, but a strong tendency exists to also use it for application-specific IC (ASIC) designs in the field of the Internet of Things and wearable electronics [1]. Similarly to mature CMOS IC technologies, electrostatic discharge (ESD) events are a reliability threat and proper protection needs to be developed in TFT technologies too. The ESD threats in TFT display applications can be even worse due to the large panel size and glass substrate. The accumulated electrostatic charge that can cause an ESD event is closely monitored and minimized during the display panel manufacturing and assembly, to avoid any ESD event in the first place [2]. After production, ESD protection can be implemented using a system level ESD protection approach with off-chip components.

Flexible TFT-based Radio-Frequency identification (RFID) products, need to have fully integrated ESD protection as there are no external electrical connections for off-chip components. A similar approach might be needed to support the trend towards bezel-less displays, in which additional complex driving circuits are being integrated into the display [1].

The amorphous Indium-Gallium-Zinc Oxide (a-IGZO) material is one of the best candidates for low power flexible ASIC applications (Figure 1) due to its high field-effect mobility [1,3]. Several publications have reported on ESD robustness, reliability and breakdown mechanisms of poly-Si TFTs, which are the preferred choice for displays, [4, 5, 6, 8, 9]. However, for the more recent a-IGZO TFTs, less publications are available. [7,10,11] focus on the implementation of a-

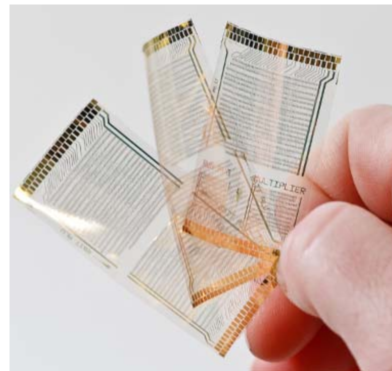

Figure 1 - Photograph of a flexible TFT microprocessor [12].

IGZO TFTs in circuits, comparison with amorphous Si, analysis of different substrates, contact resistance and device characteristics in general. No ESD analysis on different TFT device architectures has been performed so far.

In this work, we analyze three different a-IGZO TFT structures for their ESD robustness by means of Transmission-Line-Pulse (TLP) measurements. Firstly, the state of the art of the technology is presented, and secondly, the measurement results are shown and discussed. As a conclusion, the best TFT structure in terms of ESD protection is chosen.

II. The State of the Art

The majority of a-IGZO TFT technologies today are fabricated using the etch stopper layer (ESL) methodology, which is a bottom-gate architecture. Due to its high parasitic overlap capacitance and low scalability, it is not the preferred technology for high end applications today [1]. Instead, a top gate self-

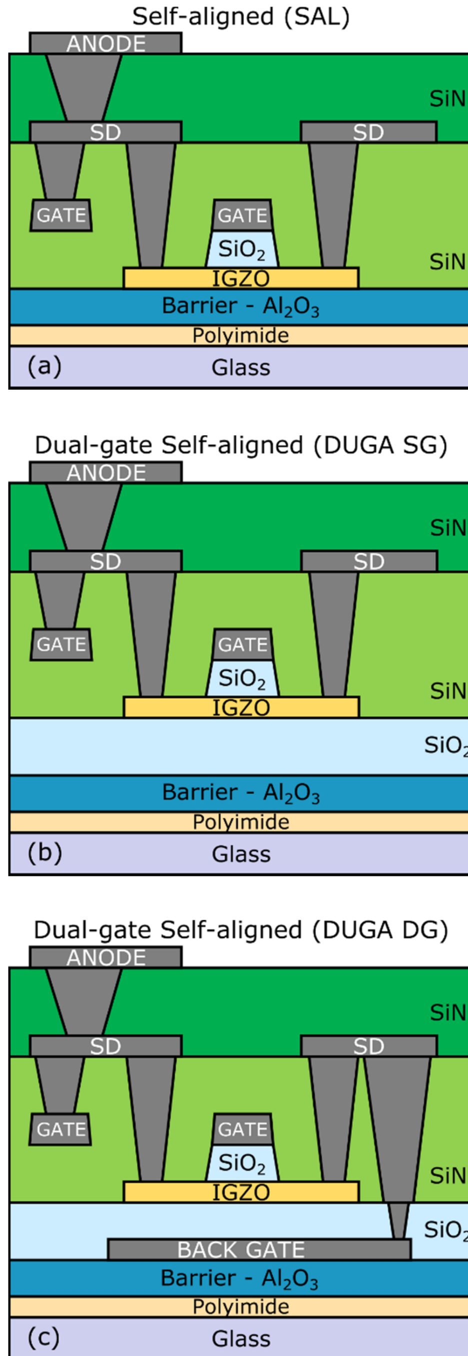

Figure 2 - Cross-sections of the a-IGZO TFT for (a) a self-aligned top gate only process (SAL), (b) a dual-gate process (DUGA) w/o the bottom gate and (c) and with the bottom gate.

aligned (SAL) technology with no overlap (Figure 2a) is a more favorable choice.

A. Dual-Gate Structures

An additional back-gate can be included to the SAL technology, featuring the ability to control the threshold voltage of each individual TFT and thus the functional transistor performance. Figures 2b and 2c depict the cross-section of such dual-gate self-aligned (DUGA) technologies with and without the bottom gate option respectively.

B. Tunable Threshold Voltage

The bottom gate or backgate in the DUGA TFTs can be used in a similar way as the body terminal in planar Si-based CMOS technologies. Therefore, it allows tuning of the threshold voltage of individual devices, which has been proven beneficial in unipolar circuit design [1]. A comprehensive study of amorphous Si and organic dual-gate TFTs has been presented in [13], listing the threshold voltage modulation, a steeper subthreshold slope, a higher drive current and a lower off current as main advantages with respect to a single gate device.

The ESD measurements of a-IGZO TFTs presented in [7] and [10] revealed leakage currents of the ESD device in the order of µA. Meanwhile, the technology improved significantly toward a positive threshold voltage. In this paper, the ESD performance of dual-gate devices is measured for the first time.

III. ESD Measurement Results

The three TFT devices of Figure 2 are measured by 100 ns transmission line pulse (TLP) system with 2 ns rise time. The TLP stress pulses have been applied to the shorted gate and drain terminals of the TFT, while the source terminal has been grounded. Therefore, the transistor has been measured in a forward diode-connection mode. Between every pulse, a DC IV sweep has been performed from -5 V reverse till 2 V forward polarization, to monitor the *leakage* and *on* currents. An abrupt increase of the leakage current has been taken as failure criterium. The I_{t2} and V_{t2} values, which represent the TLP current and voltage, are equal to the last measured point before failure.

A. SAL TFTs

The measured TLP results on the SAL devices with two different gate lengths (Figure 2a) are shown in Figure 3. As expected, the channel resistance (R_{on}) increases by increasing the gate length. The extracted I_{t2} and V_{t2} parameters are given in table 1. These results are comparable to references [7] and [10], except here the observed leakage current is significantly lower. Even though a leakage current degradation of about three orders of magnitude is observed for the device with L of 2 µm (Figure 3), this is not taken as a failure. The reason for this is that the device can still protect against ESD without affecting the power consumption. Only an increase of leakage current is thus taken as a failure.

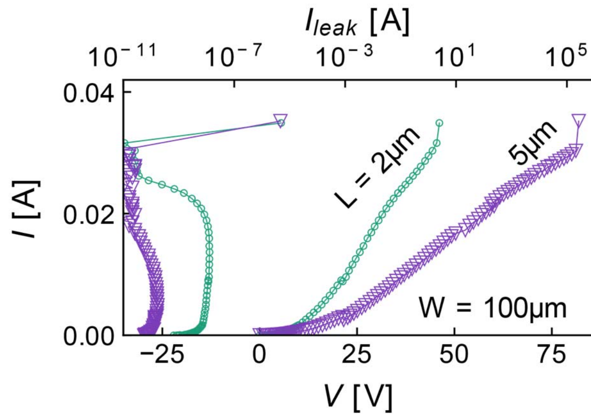

Figure 3 - TLP measurement results for two SAL TFTs with different gate lengths.

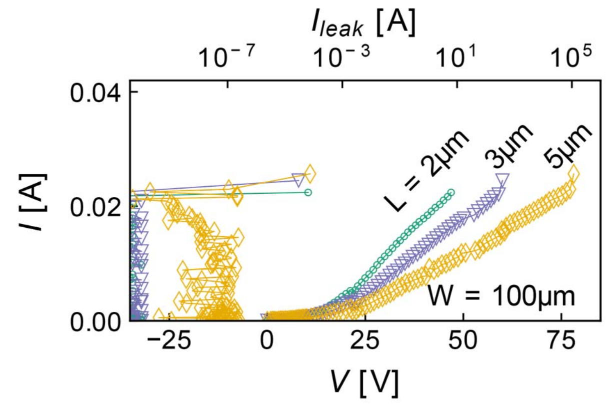

Figure 4 – TLP measurement results for three DUGA top-gate-only TFTs with three different gate lengths.

B. DUGA TFTs

The measurements performed on single-gate (SG) DUGA TFTs (Figure 2b) with three different gate lengths of 2, 3 and 5 µm, are shown in Figure 4. Compared to SAL, the I_{t2} values are approximately 30% lower, but the V_{t2} remains the same. This suggests a lowered thermal dissipation, as will be further explained with TCAD simulations in subsection C.

Still, using a double gate (DG) (Figure 2c), which is the main scope of DUGA, restores and even boosts the I_{t2} values, as shown in Figure 5. In this case, compared to SAL, the I_{t2} has been increased by 25% and the V_{t2} lowered by 25%. This suggests more carriers are available in the channel due to the increased electrical field. The extracted TLP and DC parameters can be found in table 1.

Since not all measured TFTs have the same field-effect mobility and the possibility of process variations between the DUGA and SAL technologies exist, we compare the three architectures by taking the product of I_{t2} and V_{t2}. For all experiments the same TLP pulse width of 100 ns has been used, so this product is equivalent to the net of generated and dissipated power in the a-IGZO semiconductor.

The $I_{t2}V_{t2}$ product for all measured devices is plotted against the gate area and shown in Figure 6. This plot suggests that DG DUGA devices are equivalent with the SAL devices, even with the additional thermally-insulating SiO_2 layer. An explanation for this may be attributed to the bottom gate, which is a metallic layer and therefore an excellent thermal conductor. TCAD simulations in the following sub-section will provide a better insight into the thermal behavior of all three TFT architectures.

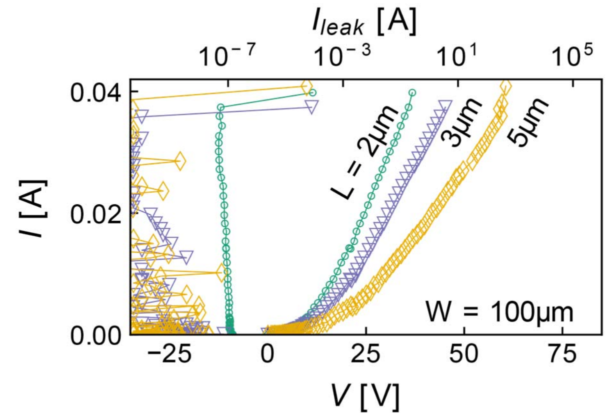

Figure 5 - TLP measurement results for three DUGA TFTs with three different gate lengths, whereby the top gate is connected to the back gate.

Table 1: Parameters extracted from the TLP measurements on three different TFT structures from Figure 2.

Device	L [µm]	I_{t2} [A]	V_{t2} [V]	R_{on} [Ω]	I_{leak} [A]
SAL	2	0.03	45	1044	6.50E-10
SAL	5	0.03	81	2029	6.60E-11
DUGA-SG	2	0.02	46	1405	1.00E-12
DUGA-SG	3	0.02	59	1898	1.00E-12
DUGA-SG	5	0.02	77	2558	4.60E-08
DUGA-DG	2	0.04	36	677	1.50E-07
DUGA-DG	3	0.04	45	853	2.30E-09
DUGA-DG	5	0.04	61	1179	1.00E-12

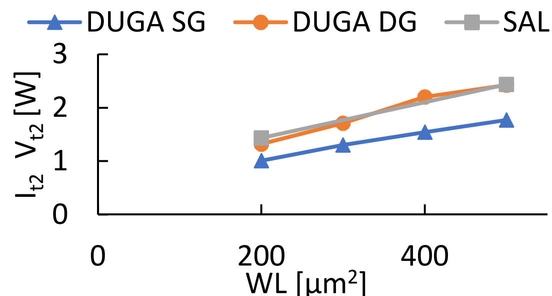

Figure 6 - Equivalent electric power delivered to the TFT before failure.

C. TCAD Thermal Analysis

An industry-standard mixed-mode finite elements simulator [15] has been used to compare the self-heating effect of the three a-IGZO TFT architectures. A 100 ns wide TLP pulse resulting in about 20 mA of current has been used as the stress condition, to emulate the measurement results. The simulated device dimensions have been chosen equal to the actual ones, 100 µm in width and 5 µm in length. Despite uncertainties on the exact thermal properties of the oxide layer grown with a low thermal budget [16], a meaningful model was obtained that allows for a relative comparison. As an example, the used dual gate DUGA TFT structure is shown in Figure 7a. At the end of the TLP pulse the peak temperatures reached 550 K in the a-IGZO channel. Due to its elongated geometry, the heat flow from the channel is mainly vertical, as depicted by the thermal profile of the TFT cross-section in Figure 7b.

Such simulation of the peak temperature has been performed for all three TFT architectures and is depicted in Figure 8. It has been observed that the SAL structure heats up significantly less during the first ~50 ns of the TLP pulse, compared to the two DUGA structures. This can be explained by the AL_2O_3 barrier layer, which is a relatively good heat conductor located directly underneath the a-IGZO channel, in the SAL TFT. The heat capacitance of SiO_2, which is in the range from 1.3 to 1.5 W/(m·K), and of Al_2O_3 barrier, which is in the range from 12 and 38.5 W/(m·K) [14], indicates that TFTs produced with the DUGA technology may be more susceptive of self-heating compared to SAL.

Part of the thermal energy from the SAL device channel is immediately evacuated to this barrier layer. In both DUGA structure, the a-IGZO-channel is surrounded by a thin SiO_2 layer, which is a good thermal insulator and causes the channel to heat up more quickly. Nevertheless, DUGA TFTs are able to remove some of the heat to the gate metals (top and bottom) after a small delay. This process is obviously more efficient where both bottom and top gate metal are present (DUGA). As such, at the end of the TLP pulse (100 ns), the dual-gate DUGA and SAL structures have both reached a similar peak temperature, while the single-gate DUGA TFT is significantly hotter because it only has the top metal gate acting as a heat sink. This result explains at least qualitatively the difference in the absorbed electric energy observed in the measurements.

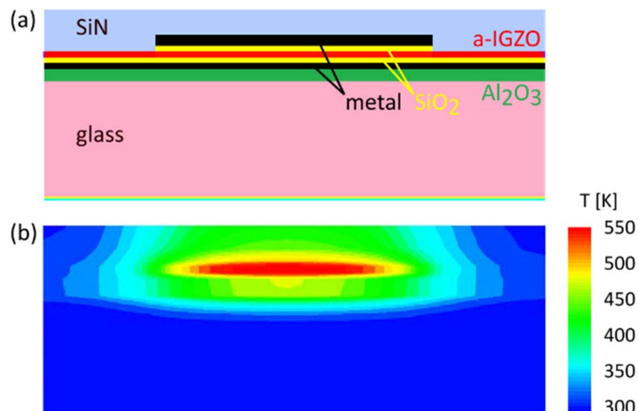

Figure 7 – The TCAD simulation a) structure (example for the dual gate DUGA TFT) and b) result of self-heating at the end of a 20 mA 100 ns TLP pulse.

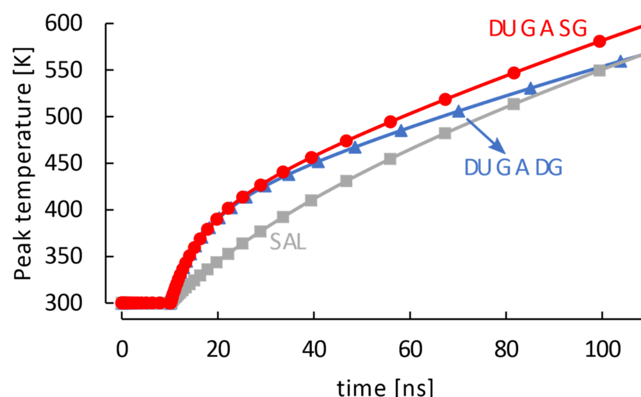

Figure 8 – The temperature evolution in the a-IGZO channel during the 100 ns TLP pulse for the three TFT structures, the SAL, the single- and dual-gate DUGA. Even though the dual-gate DUGA heats up faster it has an equivalent peak temperature as the SAL at the end of the TLP pulse.

D. Thermal Hot Spot

We have observed breakdown spots after TLP stress, located between the gate and the source terminal, as shown in Figure 9. It is believed the breakdown originates in the dielectric between the gate metal and the a-IGZO channel. Note that the gate and drain terminals have been shorted and at the same potential.

In order to confirm that the breakdown location is between the gate and the channel and not between the gate and source terminals directly, we have conducted more measurements. Several devices with varying distances between the gate to the source/drain contact holes (SP), as depicted in Figure 10, have been measured. The argument for this experiment is that the a-IGZO layer might represent a high resistance and thus the TFTs weak point is not necessarily under the gate. In principle, the SiN_x intermetal-dielectric dopes the a-IGZO resulting into a more conductive a-IGZO, while the SiO_2 gate dielectric maintains the semiconducting properties of a-IGZO.

For this scope three devices of the single-gate DUGA structure have been measured with TLP. The extracted results are shown in Figure 11. Both the I_{t2} and the channel resistance R_{on} are not correlated with SP, proving that the a-IGZO extensions (the SP region) are not the weak point. This suggests that the failure point is between the channel and the gate, as explained by literature for the amorphous Si case in [4].

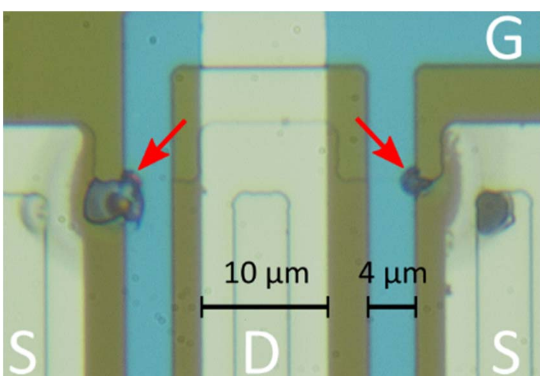

Figure 9 – Two breakdown points observed after TLP stress on a TFT device with WL = 100 × 4 µm^2. G marks the gate terminal, S the source terminals and D the drain terminal. The breakdown starts betwen the gate and the a-IGZO channel (right arrow) and propagates towards the source (left arrow).

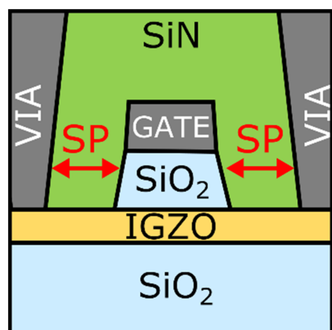

Figure 10 - The spacing (SP) between the gate and source/drain contacts can vary and it has been used to check if the breakdown due to TLP stress happens in the SiN or in the SiO_2 dielectric.

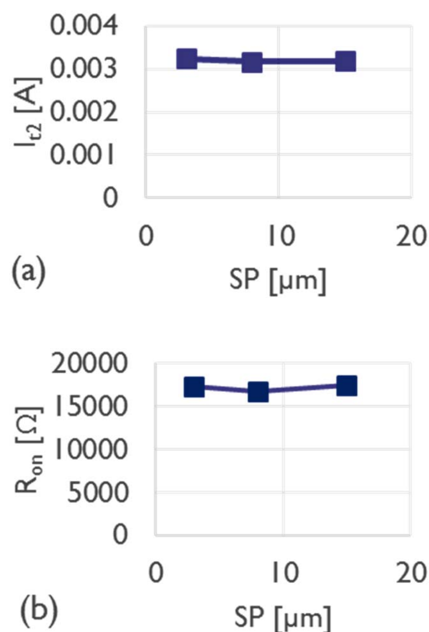

Figure 11 - The source/drain to gate spacing (SP) does not affect the device (a) I_{t2} values and (b) the on resistance (R_{on}). The common area of the devices used in this experiment is WL = 15 × 5 µm^2.

E. Leakage and Drive Current Degradation

Degradation of the TFT DC performance has been observed during TLP measurements. For SAL devices, the leakage current I_{leak}, measured at -5 V gate bias, for all measurements first increases with TLP stress and then decreases again. The same increasing trend has also been observed for the drive current I_{on}, measured at +2 V gate bias, but there the effect is so small that it can safely be neglected. On the other hand, I_{on} completely degrades before the hard failure. Both I_{leak} and I_{on} currents for the SAL device as function of TLP stress are depicted in Figure 12a.

The I_{on} degradation is less pronounced for the DUGA architecture with a single gate, at least for the device with the longer channel (L = 5 µm), as depicted in Figure 12b. The most reliable structure so far is the dual-gate DUGA, for which the I_{on} degradation is the smallest of the three (Figure 12c).

Since the strongest degradation is observed in the SAL device architecture, a possible explanation could be that the exposure of the a-IGZO layer to the Al_2O_3 barrier has a more detrimental effect on the threshold voltage than the exposure to SiO_2. Al_2O_3 has been reported to have a stronger charge trapping when used in advanced CMOS technologies [17]. For top-gate TFT technologies it is known that this barrier layer can have a detrimental effect on the device reliability [18].

Another explanation, suggested by [19], could be that using double gates with equal potentials cancels the electric field in the a-IGZO layer, thus reducing the stress and degradation.

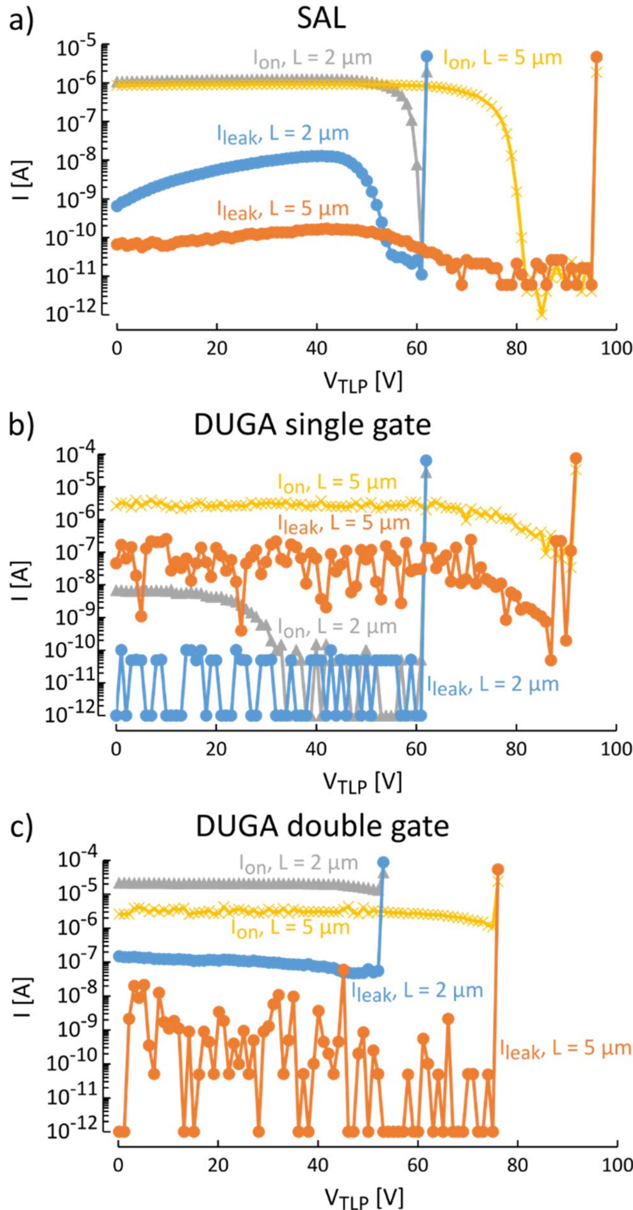

Figure 12 – The *on* current I_{on} measured for V_g = 2 V and the *leakage* current I_{leak} measured for V_g = -5 V. In case of the dual-gate structures, both gates have been shorted together.

IV. Conclusion

We have analyzed three a-IGZO TFT architectures in two different technologies for ESD robustness using the TLP measurement method. Our insights suggest that the double gate DUGA TFT devices, given it has better threshold voltage control and an comparable thermal conductivity as the SAL devices, is the best of the three to be used as an ESD protection device.

Acknowledgements

This work received funding from the European Research Council under the European Union's Horizon 2020 research and innovation program under grant agreement no. 716426 (FLICs project).

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