

# Active capacitive ECG system with all-digital “driven right leg” common mode suppression

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**Abstract**—A digital system for capacitive ECG measurement is proposed, including a digital driven right leg loop, which compared to current analog systems, can provide significantly greater robustness for the placement of electrodes in real-world scenarios such as inside a vehicle, as well as greater flexibility in algorithmically defining the optimal ECG electrode positions in an array post-acquisition. The system is stable with high DRL gains and successfully rejects common mode interference, such as motion artefacts from nearby movements, by up to 60dB.

**Keywords**—*electrocardiography, capacitive ECG, unobtrusive sensing, active electrode, driven-right-leg circuit*

## I. INTRODUCTION

Capacitive, through-clothing measurement of the electrocardiogram (ECG) enables applications in unobtrusive monitoring, where traditional ECG measurements are not suitable or desirable. The sharp features in the ECG signal make it uniquely suited for precise and direct measurement of heartbeat intervals and derived features such as heart rate variability (HRV). Other unobtrusive measurement methods such as ballistocardiography (BCG), (remote) photoplethysmography (PPG), or doppler radar measure pulse rate and pulse rate variability (PRV) instead, which has been found to significantly differ from HRV under certain circumstances, including stress, respiration, exercise and ambient temperature [1]. Accurate unobtrusive HRV measurements can enable applications such as the monitoring of stress [2], emotional state [3] as well as

various aspects of cardiovascular health [4]. The unobtrusive nature of the measurement allows to integrate it naturally into objects surrounding us in daily life, such as car seats [5][6], home and hospital beds [7][8], office seats [9], toilet seats etc.

Since capacitive ECG exhibits a very high source impedance, up to 59 G $\Omega$  at 0.67Hz [9], in practice the use of active electrodes is required, where the input amplifier or buffer is placed very close to the sensing electrode surface, which itself is a conductive plate (e.g. conductive textile), frequently shielded / guarded from the back side to avoid pick-up of environmental noise. Currently, capacitive ECG active electrodes are implemented with analog outputs [8][9][10]. In the back-end, these analog signals are pair-wise differentially amplified (Fig. 1 (a)). This provides rejection of common mode signals, so that a relatively high gain and limited ADC resolution can be used. This approach has two main drawbacks. First, the analog interconnections are susceptible to picking up noise. This is a concern in real-world applications with various sources of environmental interference present (e.g. inside a vehicle), and particularly when the active electrode front-ends are positioned in significantly different locations (e.g. one electrode at the steering wheel and another one in the car seat), where interference will be picked up differentially and hence not suppressed by the differential amplifier’s common mode rejection ratio (CMRR). Second, to obtain sufficient CMRR, electrodes need to be pair-wise combined in ‘positive’ and ‘negative’ electrodes to perform differential amplification of

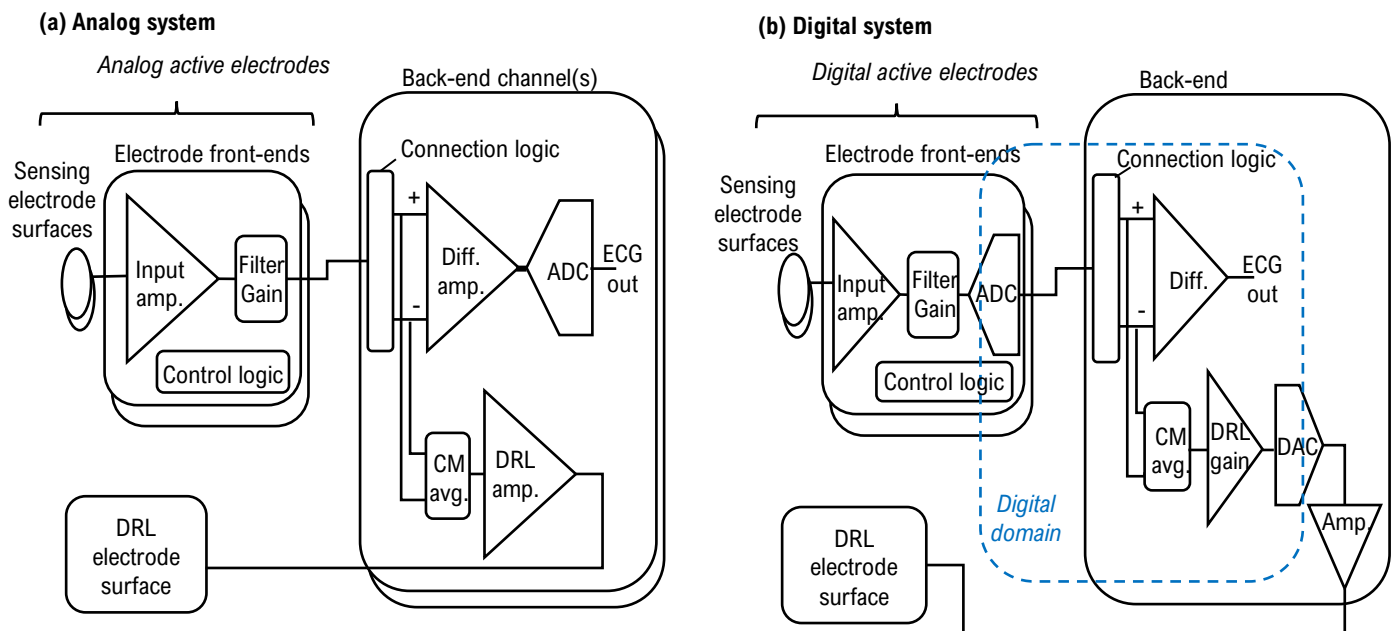


Fig. 1. Simplified block diagrams of (a) analog and (b) digital capacitive ECG system. DRL=Driven Right Leg. CM=Common Mode.

the signal. These combinations need to be made upfront or in real time. If the combination turns out to have been suboptimal (e.g. because one of the two electrodes in the pair was not well coupled to the body), the signal is unrecoverably lost. If a common negative ‘reference’ electrode is used for all ECG channels, a poor coupling on this electrode would jeopardize the entire signal set. This is especially a concern in larger arrays of electrodes allowing to support various body postures as required for true unobtrusiveness.

The digital system proposed in this work addresses both these limitations as well as some new inherent challenges.

## II. DRIVEN RIGHT LEG (DRL) CIRCUIT

The effective CMRR is limited by the ratio of source impedance mismatch to input impedance as well as by mismatch in the input impedance and/or front-end gain. For example, with a coupling of 10pF with a mismatch of 30% and an input impedance of  $(50\Omega // 3\text{pF}) \pm 20\%$  [9] the effective open-loop CMRR could be as low as 30dB at 10Hz. This is insufficient for robust real-world measurements. While mains interference may be acceptably handled by frequency-based filtering, in-band sources of common mode interference cannot be removed in that way. An important source of such in-band common mode interference in real-world capacitive ECG measurements are nearby motions, e.g. of other people in the immediate vicinity or even of the subject’s own limbs. A frequently applied technique to improve the effective CMRR is DRL, where the averaged common mode voltage of the measured ECG signal is inverted & amplified and fed back into the body through a separate DRL electrode (see Fig. 1), improving the effective CMRR by a factor equal to  $[1 + \text{the closed loop DRL gain}]$ . This well-known technique is particularly useful in capacitive ECG to improve robustness against nearby motions. To be effective, the (inverting) gain in the DRL loop needs to be high enough, while avoiding loop instability. Due to the higher attenuation in the capacitive feedback to the body, typical effective DRL gains are higher than for contact ECG, in the order of -10 to -100.

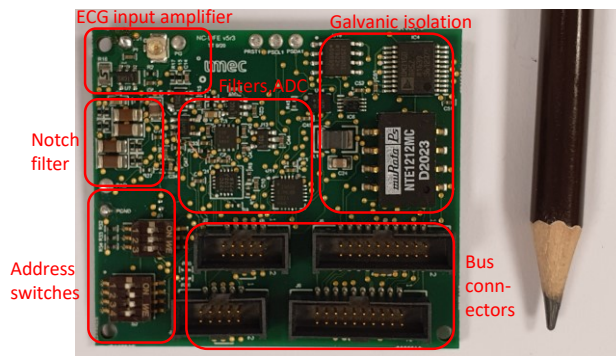


Fig. 2. Digital front-end board (51x44mm), pencil for size reference

## III. DIGITAL SYSTEM ARCHITECTURE

The digital system architecture is depicted in Fig. 1 (b). The key concept is straightforward: moving the ADC from the back-end into the front-end. This results in a digital interconnection which can robustly be integrated in various locations. The digital signals can be communicated over different types of industry standard buses (e.g. a CAN or similar bus inside a vehicle). In the implemented system (shown in Fig. 2), I<sup>2</sup>C and SPI buses are used. A common signal ground connection is also required.

This approach comes with two new challenges: First, the single-ended signal is digitized, hence all common mode components are still present. Therefore, analog gain is very limited, resulting in a high dynamic range requirement for the ADC. This aspect also leads to an important improvement in flexibility over the analog system: each single-ended signal is recorded independently. There is no need to designate pair-wise electrode combinations or a shared common electrode upfront – this can be calculated in the digital domain, in real time or off-line. This allows the optimal electrode combinations to measure the ECG signals of interest to be determined algorithmically after the acquisition. Note that a real time determination of which electrodes’ common mode signals will be used as input to the DRL feedback is still needed. This can be done using signal quality indicators [11] or potentially using capacitive lead on/off measurements, e.g. based on electrode-body

TABLE I. STABILITY (PHASE MARGIN) ANALYSIS OF DIGITAL DRL LOOP

Digital DRL gain	Overall DRL gain	Digital delay						Phase margin (°)
		5 $\mu$ s	10 $\mu$ s	20 $\mu$ s	50 $\mu$ s	100 $\mu$ s	200 $\mu$ s	
1	-1.65	STABLE	STABLE	STABLE	STABLE	STABLE	STABLE	
2	-3.3	132.6	132.3	131.8	130.1	127.2	121.5	
5	-8.25	102.4	101.5	99.6	94.0	84.6	65.9	
10	-16.5	90.5	88.6	84.8	73.2	54.0	15.5	
20	-33	79.3	75.4	67.8	44.8	6.5	UNSTABLE	
50	-82.5	57.9	48.8	30.8	UNSTABLE	UNSTABLE	UNSTABLE	
100	-165	34.7	18.8	UNSTABLE	UNSTABLE	UNSTABLE	UNSTABLE	

Phase margin legend:	>60°	30°-60°	0°-30°	<0°
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“STABLE” indicates unconditionally stable (loop gain never reaches 0dB). “UNSTABLE” indicates a negative phase margin. A phase margin of 60° or more is ideal, 30° is considered the minimum for stability. Simulation parameters: DRL electrode to body capacitance: 250pF, body to ground capacitance: 250pF, ECG electrode to body capacitance: 35pF, DRL loop bandwidth 146Hz. Overall DRL gain includes an inverting gain of -1.65 in the analog domain.

capacitance [9].

The second challenge for a fully digital interconnection is that the DRL loop needs to operate through the digital domain as well. This introduces additional delay in the loop which, if uncontrolled, may lead to instability. Table 1 shows the results of a stability analysis of the digital DRL loop. To maximize DRL gain for effectiveness while maintaining stability, the digital delay from the ADC input through the digital processing unit to the DAC output should be kept preferably below  $20\mu\text{s}$ .

The combination of these two challenges result in a stringent specification for the ADC: it needs to have a high dynamic range due to the single-ended measurement, and at the same time it needs to be fast to minimize the digital delay for DRL loop stability. To investigate the required resolution for the ADC, the proposed proof of concept system (Fig. 2) implements two ADC's: a high resolution, relatively slow signal path ( $0.67\text{-}67\text{Hz}$  bandwidth) using a 24-bit ADC (TI ADS122C04, with 17.2 ENOB at 600Hz sample rate), and a fast, slightly lower resolution signal path ( $0.67\text{-}10\text{kHz}$  bandwidth) using a 16-bit ADC (TI ADS8326, with 14.7 ENOB at 250kHz sample rate). As shown in Fig. 7 and discussed below, the 16-bit ADC resolution and ENOB is sufficient, so future implementations of the proposed system will not require the separate higher resolution ADC.

To avoid the possibility of interference coupling into the signals from e.g. the acquiring PC through the ground, a galvanic isolation is placed between the front-end's signal ground and the back-end. This signal ground is also connected to the galvanically isolated DRL feedback circuit. This galvanic isolation also provides additional safety for the subject.

The digital part of the DRL signal path is implemented using an FPGA to minimize the delays. The measured digital

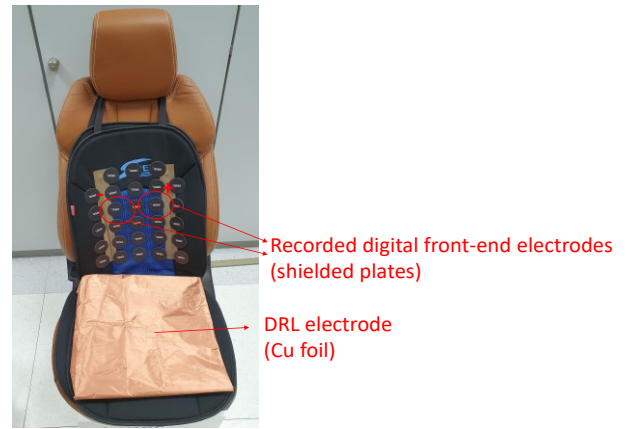


Fig. 3. Test setup used for digital capacitive ECG measurements. Digital front-ends are placed in the back of the seat cover and connected to the back-end in the back of the seat.

delay from ADC input to DAC output is  $13.6\mu\text{s}$ . The use of an FPGA also allows to use a single clock line with two MISO SPI lines for simultaneous acquisition of the signals used for DRL.

#### IV. MEASUREMENT RESULTS

Through-clothing capacitive ECG measurements were done from a seat (Fig. 3) using the proposed digital system. Fig. 4 shows example resulting ECG signals and Fig. 5 shows the quantified ECG signal quality in function of DRL gain. These results illustrate clearly how the digital DRL effectively suppresses common mode interference, and particularly from a nearby moving subject, increasing the signal quality.

Note that the proposed system features an optional analog  $50\text{Hz}/60\text{Hz}$  mains notch filter which can fully suppress

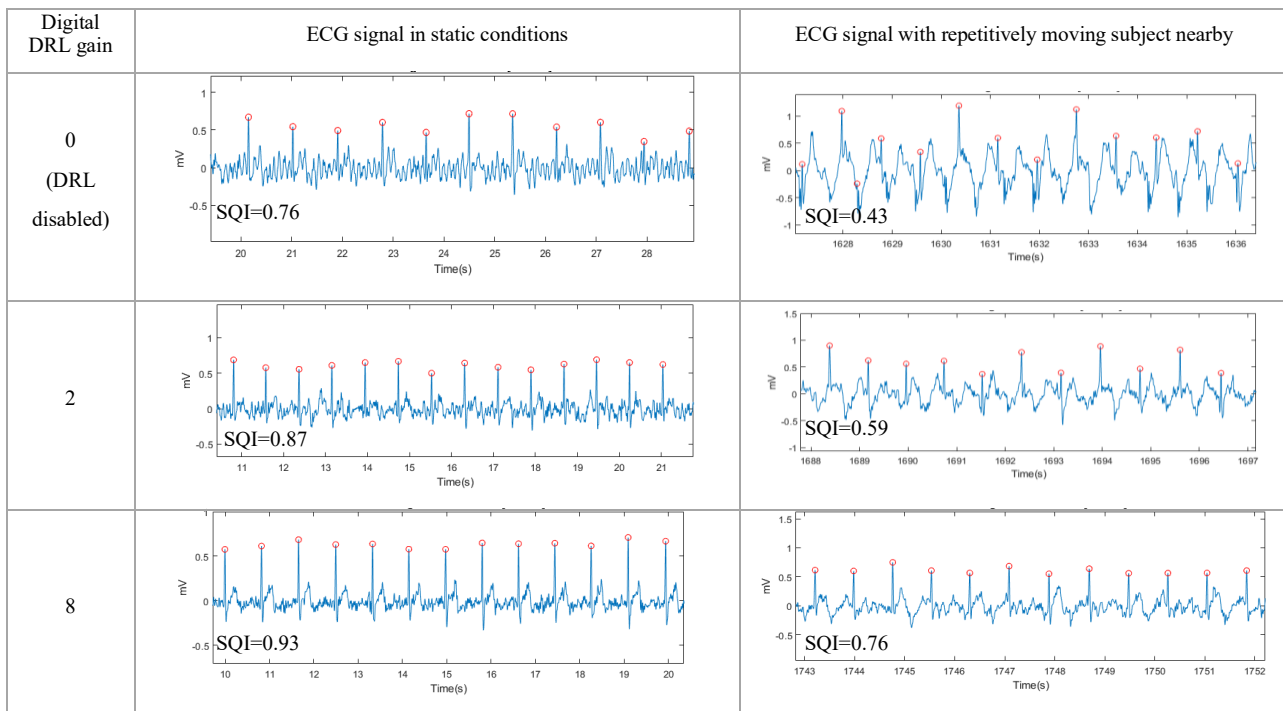


Fig. 4. Example differential capacitive ECG signals in static conditions and with repetitive motions of  $1.5\text{-}2\text{Hz}$  by a second person situated approximately  $80\text{cm}$  behind the subject, for 3 different settings of digital DRL gain. These signals were measured from the back with the setup in Fig. 3 through one layer of clothing. Signal quality is quantified using a template correlation-based signal quality indicator (SQI) [11].

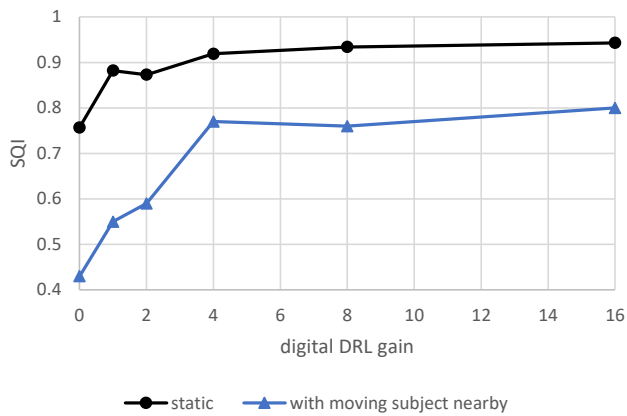


Fig. 5. Quantified signal quality using template correlation based SQI [11] in function of digital DRL gain with and without a moving subject nearby.

mains noise, but such a filter has no effect on the common mode noise induced by a nearby moving subject and was not used in the presented measurements. In order to characterize the effective CMRR in the real system (including the human body), the effective impact on ambient 50Hz mains noise was measured (Fig. 6). The digital difference process provides a CMRR of 25-28dB compared to the single-ended signals (including all mismatches as described above). This baseline CMRR is further significantly improved by the DRL gain, up to a total of 60dB, roughly in agreement with the theoretical expectations. This CMRR increase is evidenced in the signals from Fig. 4 in static conditions, where for example the T wave is less affected by CM noise.

Finally, the required effective resolution of the ADC is quantified in Fig. 7 by truncating and rounding the 24-bit ADC codes to the mentioned number of bits. It shows an effective number of bits (ENOB) of 14 is sufficient to avoid significantly degrading the ECG signal quality by quantization errors.

## V. CONCLUSIONS

The proposed work has successfully demonstrated the feasibility of a digital active electrode capacitive ECG system with an all-digital DRL loop to reject common mode interference including artefacts from nearby motions. When compared to analog systems, this enables an important increase in flexibility, both in placement e.g. inside a vehicle by an increased robustness against interference, as well as by permitting to optimally derive the desired ECG signals

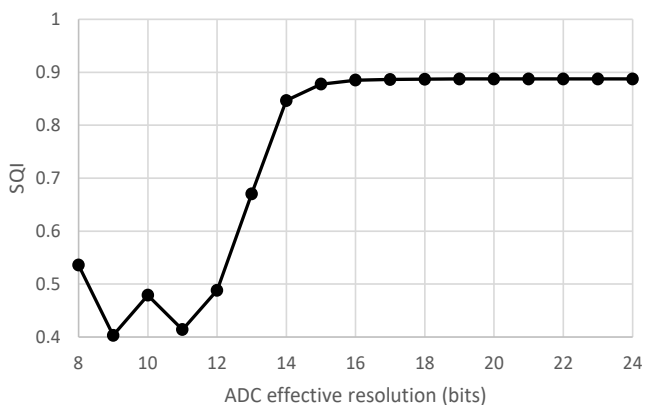


Fig. 7. ECG signal quality estimated using template correlation SQI [11] vs. ADC effective resolution.

from an array algorithmically post-acquisition, to accommodate for varying body postures and obtain a truly unobtrusive measurement. In future work, this concept can be further validated in real world scenarios such as inside a driving vehicle.

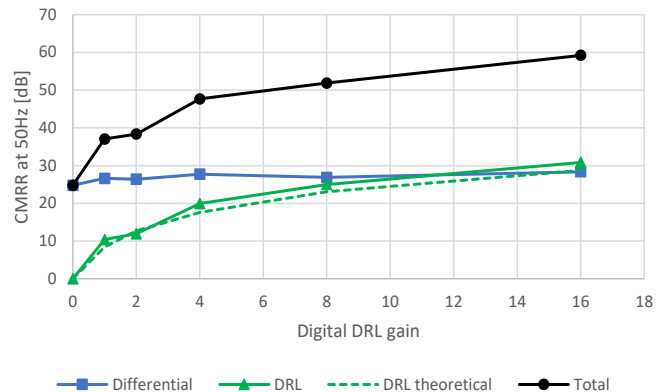


Fig. 6. Measured CMRR at 50Hz in the setup of Fig. 3 vs. digital DRL gain

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