

Analysis of Thermal Cross-Talk in Photonic Integrated Circuit using Dynamic Compact Models

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Abstract—Thermal modelling of photonic integrated circuits (PICs) is required for circuit design and for the development of thermal control algorithms. In this work, we present a methodology for obtaining a compact dynamic thermal RC-model of a PIC. PICs are sensitive to thermal coupling, and in this paper it is shown that traditional resistive coupling does not suffice and a new coupling method is derived. The case study to which the new methodology is applied, is a dense wavelength division multiplexing ring filter with 8 channels. With the obtained RC-model, computational time is reduced from 5.5 hours for finite element simulation to <1 second for a single step response. Using the compact model, circuit-level analysis of frequency response is carried out. Because of its high computational efficiency, the compact model opens possibilities of simulating thermal tuning algorithms.

Index Terms—Silicon Photonics, compact thermal modelling, RC-network, thermal crosstalk

I. INTRODUCTION

SILICON photonics (SiPho) transceivers are used for communication links which require high bandwidth and long distance. Data centers are a prototypical example of this. The optical transceivers use wavelength-division multiplexing to increase the data throughput in optic fibers by combining multiple data streams in parallel [1], [2]. Electro-optic modulators and wavelength filters used in transceivers are typically resonance based devices, which are very sensitive to fluctuations in temperature. To combat this, they are implemented with metallic or doped Si heaters for thermal tuning [3]–[5]. In this paper a methodology is proposed for compact dynamic circuit-level thermal modelling of a photonic integrated circuit (PIC). An 8 channel dense wavelength division multiplexing (DWDM) double ring filter array is used as a case study. This PIC is used at the receiver side in order to demultiplex an incoming signal and pass the correct wavelength to the corresponding photodetector. A schematic representation of this wavelength filter is shown in Fig.1. The red lines represent the waveguides and the black lines are the heater connections. Double ring filters typically use collective thermal tuning, meaning that there is a single heater current input line, splitting its current over all channels equally. This is in contrast with individually tuned channels, where the resonance in each channel is monitored and the heater current is adapted appropriately in order to lock the ring to the desired wavelength. The die cross section is shown in Fig.2. Substrate undercut (UCUT) is introduced in order to increase the thermal performance. By locally

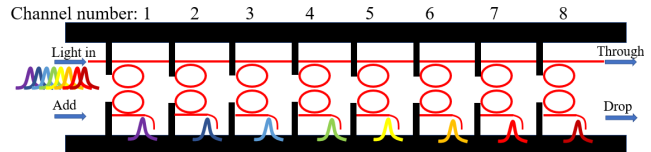


Fig. 1. Schematic representation of 8 channel DWDM double ring filter array, red = waveguide, black = heater connects

etching the Si substrate below the device, heat flow directly into the substrate is avoided and the heater efficiency is increased [6]–[8]. The effect of UCUT on the device and circuit dynamics will be further investigated in this paper.

The traditional method used for thermal modelling PICs is with finite element (FE) simulation [9]. However, because of the multi-scale nature of the problem, the computational time becomes very large. Resolving geometric details at device-level (nm scale) together with the full circuit geometry (100 μm –1 mm scale) results in a large number of required elements for simulation. As shown in this paper, a single step response FE simulation takes up to 5.5 hours (~ 30 time steps). Thermal tuning and control simulation requires hundreds or thousands of step responses, showing that this is infeasible with the traditional modelling methods. Compact thermal RC-models have been applied in many areas, e.g. non-photonic integrated circuit (IC) design [13], [14] and electronic packaging [10]. However, in Section II.D it is shown that thermal coupling in PICs requires special treatment compared to regular ICs. Compact RC-models for PICs shown in [15], [16] rely on abstract 3D representation of the structure using resistive elements, which is more complex compared to the method used in this paper. In Section II the methodology is further elaborated and in Section III the results are analyzed. In Section III.A the device and circuit frequency response are calculated. In Section III.B a circuit start-up simulation is performed, in Section III.C circuit thermal coupling is investigated and in Section III.D thermal tuning and control are simulated.

II. METHODOLOGY

The proposed methodology is shown schematically in Fig.3. We start from a PIC circuit layout and experimental data on the performance of the photonic devices. This information is used to construct a high-fidelity finite element thermal model.

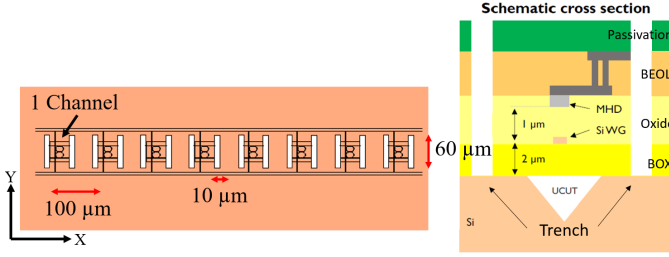


Fig. 2. Cross section of SOI SiPho die. BEOL = back end of line, MHD = metal heater, Si WG = Si waveguide, BOX = buried oxide, UCUt = substrate undercut. Thermal insulation trenches are optional for cross-talk mitigation.

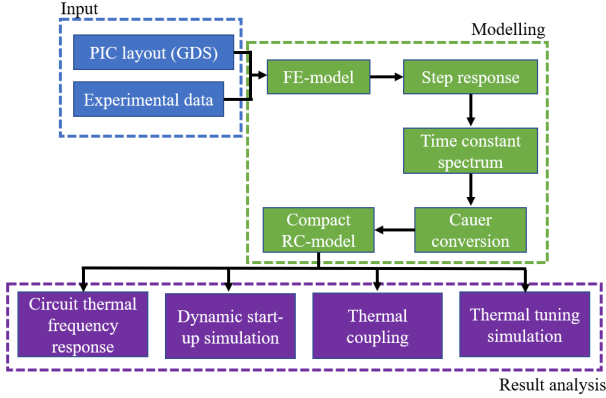


Fig. 3. Schematic of compact modelling methodology used in this paper

With this model a dynamic simulation of a step response is done, which allows to extract a time constant spectrum that describes the system dynamics. Using the information in this spectrum, the system can be modelled with resistive and capacitive elements. This allows to simulate the PIC in a circuit simulator (e.g. LT Spice). The resulting RC-network is called a Foster network, which is converted to a Cauer network in order to better match the physical layout of the PIC. Once the compact circuit RC-model is obtained, this opens up possibilities to analyze the circuit which is not practical with standard FE simulations because this is too time consuming.

A. Finite element model

The FE-model contains 1.5 million elements and the detailed geometry of a collectively tuned 8 channel DWDM filter (Fig.4). Each ring filter has a diameter of 14 μm and the pitch between the rings is 100 μm . A real optical transceiver die is more complex and contains a large amount of photonic devices. To simplify the analysis, we only consider the 8 channel filter array. The computational domain is a SOI die (Fig.2) with size 1x1.5 mm^2 , with a 200 μm thick Si substrate. The boundary conditions mimic probestation testing: an isothermal bottom face of the die, natural air convection on the top surface and adiabatic sidewalls. The model can be calibrated with measurement data. The average waveguide temperature in each channel is of interest and this can be validated experimentally by measuring the resonance wavelength shift of a ring filter. The wavelength shift and temperature are related through the thermo-optic coefficient of the waveguide. The average

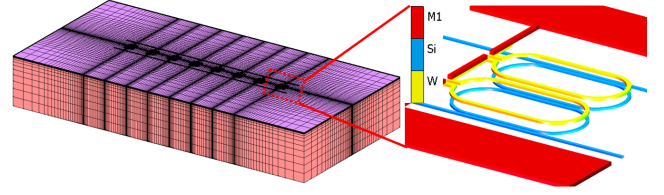


Fig. 4. Full finite element PIC model and detail of a double ring filter

waveguide temperature from the simulation is 4.8 $^{\circ}\text{C}/\text{mW}$ (with UCUt), converted to wavelength shift this corresponds to 319 pm/mW . With a free spectral range (FSR) of 13.12 nm, this results in a power consumption of 41.1 mW/FSR which can be compared with values from literature. In [11] a very similar filter is tested experimentally with a heater power consumption of 36 mW/FSR . Without UCUt, the heater efficiency is only 1.52 $^{\circ}\text{C}/\text{mW}$, which is more than three times lower compared to the case with UCUt. For this reason, the main focus will be on the case with UCUt as this is more relevant. More details on simulation parameters and material properties can be found in [17].

B. Step response and time constant spectrum

The objective of the spectral analysis is to extract R and C components which model the dynamic behavior of the ring filter. Using the FE-model, a Heaviside step function is applied to the heater power and the thermal response of the waveguide is recorded. The average waveguide temperature of a single channel is shown in Fig.5 for the case with and without UCUt. Typically the thermal response is characterized with a single exponential function, with a single time constant. However, by doing this first-order approximation a significant error can be introduced by not capturing important device dynamics. For this reason both profiles are used as an input in a least-squares fit with exponential functions which seeks to find the best fit over a whole range of time constants. The result is called the time constant spectrum (Fig.6). We see that the first time constant peak is almost insensitive to the addition of UCUt. This first peak corresponds to the vertical heat diffusion from the heater to the waveguide below. The larger time constants shift to the right after introducing UCUt, indicating that the increased horizontal heat spreading in SiO_2 causes a larger thermal mass and inertia. With this spectrum, the temperature profile can be modelled by the integration over the whole range of time constants (Eq.1). The amplitude of the time constant peak corresponds to the resistance R_{τ} . The capacitance of a time constant τ can be found as $C_{\tau} = \tau/R_{\tau}$. After inspecting the time constant spectrum, it becomes clear that the case without UCUt can be modelled by only 2 time constants and the case with UCUt with 4 time constants. The integral in Eq.1 results in a normalized temperature rise ($^{\circ}\text{C}/\text{mW}$), which is multiplied with the heater power ΔP_h (mW), and added to the ambient temperature ($^{\circ}\text{C}$).

$$T(t) = \Delta P_h \cdot \int_{\tau_{min}}^{\tau_{max}} R_{\tau} \left(1 - \left[e^{-\frac{t}{\tau}} \right] \right) d\tau + T_{\infty} \quad (1)$$

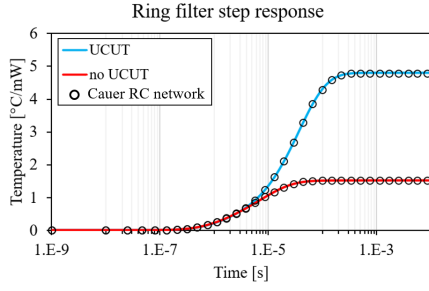


Fig. 5. Ring filter step response calculated with FE-model for UCUT case and without for a total power of 1 mW. Cauer RC-network fit shows good match with FE result.

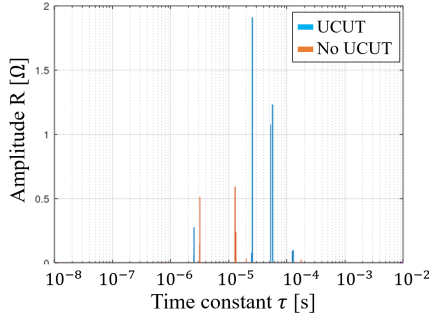


Fig. 6. Time constant spectrum for ring filter with and without UCUT

C. Cauer network conversion

The least-squares exponential fit of the step response results in a total equivalent series connection of RC-components, called the Foster RC-network. This is the mathematically best fit of the step response, but the RC-network implementation does not correspond to the correct physical behavior underlying in the structure. Because it is a series connection of RC-components, each part of the structure will heat up sequentially, i.e. each capacitor will be fully charged before the next one starts charging. In reality, the heating of the structure will be simultaneous at all scales (and capacitors). This is the motivation for the conversion of the Foster network to a layout called Cauer (Fig.7). Both circuits are equivalent because they reproduce the same total response, but the contribution of the various components is different. In the Cauer network, the different resistors and capacitors correspond to physical parts of the structure, which is not the case for Foster as this is a purely mathematical fit. The conversion is based on the methodology described in [18] and starts with calculating the equivalent complex impedance of the Foster network. The

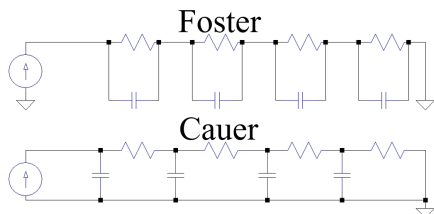


Fig. 7. Comparison between Foster and Cauer RC-network

TABLE I
R,C COMPONENTS FROM SPECTRAL ANALYSIS

	Foster		Cauer	
	No UCUT	UCUT	No UCUT	UCUT
R_1 [Ω]	0.651	0.276	1.061	1.135
R_2 [Ω]	0.872	2.01	0.459	3.093
R_3 [Ω]	n.a.	2.314	n.a.	0.5344
R_4 [Ω]	n.a.	0.198	n.a.	0.036
C_1 [μF]	4.880	9.094	3.686	4.297
C_2 [μF]	14.92	12.74	23.01	5.370
C_3 [μF]	n.a.	23.55	n.a.	84.96
C_4 [μF]	n.a.	626.3	n.a.	3274

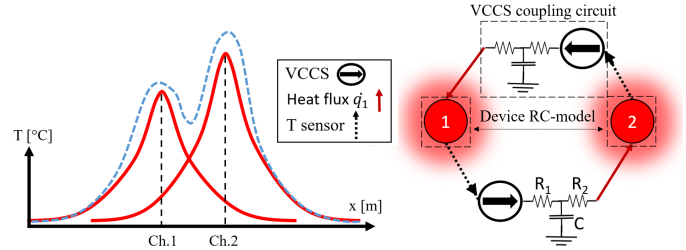


Fig. 8. Thermal superposition principle (left), and VCCS implementation between two heat sources (right).

impedance of a resistor and capacitor in parallel:

$$Z(s) = \frac{R \cdot (sC)^{-1}}{R + (sC)^{-1}} = \frac{R}{1 + sRC}, \quad s = j\omega \quad (2)$$

The total impedance is the sum of the series-connected RC-blocks:

$$Z(s) = \sum_{i=1}^n \frac{R_i}{1 + s\tau_i} = \frac{n_0 + n_1s + n_2s^2 + \dots + n_{N-1}s^{N-1}}{d_0 + d_1s + d_2s^2 + \dots + d_Ns^N} \quad (3)$$

which can be written as a rational function in polynomial form in numerator (n) and denominator (d). From this expression, the Cauer RC components can be retrieved according to the method described in [18]. The resulting Cauer network with 4 degrees of freedom matches the original FE simulation result very well: the mean squared error (MSE) between both is $10^{-6}[\text{°C}]^2$ (Fig.5). The calculated Foster and Cauer R,C components are shown in Table I. Note that the units given in Table I are the electrical equivalent units. The thermal unit for resistance in the simulation is °C/mW and the unit for capacitance is J/°C . This capacitance is obtained as the product of heat capacity and mass $C = c_p \cdot m$. Note that in Fig.6 some peaks are extremely close to each other, if this is the case they are grouped into a single time constant with the sum of amplitudes.

D. Fully-coupled RC-model

1) *Thermal (bi-directional) coupling methodology*: In this section we explain how to go from a single device RC-model to a fully-coupled circuit level RC-model. The principle of superposition is used for constructing the fully-coupled thermal model. A simplified drawing in Fig.8 shows a one-dimensional temperature profile of 2 heat sources in each other's vicinity. If each channel or source is activated

separately, the resulting red temperature profiles are obtained. However, when both channels are active simultaneously, the blue profile is obtained. This superposition is allowed under the assumption that the system is linear and time invariant (LTI). Typical non-linearities can include temperature dependent material properties which are neglected in this analysis. Time invariant can be justified as we investigate an idealized case which does not change when tested at a different time. This thermal crosstalk or coupling is difficult to model with traditional equivalent RC-networks. For example in [13] the coupling between neighboring devices is modelled with a basic resistive element. This does not work for a PIC because of two reasons: firstly, the model needs to mimic heat transfer from cold to hot (from Ch.1 to Ch.2 in Fig.8) which is impossible in an electrical simulation where the current always flows from high to low potential. Secondly, the coupling is always bidirectional which is not possible in electrical simulation because a conductor or resistor can never carry a current in two directions simultaneously. This suggests that thermal cross-talk can not be modelled accurately with a single resistive element. Alternatively, if multiple resistors are used for approximating the physical layout of the circuit, then thermal cross-talk can be captured [19] but this method requires a large number of resistors per device and is not the focus of this work.

To solve this problem, voltage controlled current sources (VCCS) are used to model the coupling (Fig.8, right). The VCCS senses the voltage (temperature) in the channel that is being heated, and sends the appropriate current (heat flux) to the neighbor channels. This coupling is implemented bi-directionally, and between all channels because each channel is coupled to all other channels. This implies that the coupling network resembles a *complete graph* where each node is connected to all other nodes, and the total number of edges scales with $E = n(n-1)/2$. Because each connection is bi-directional, the number of VCCS coupling circuits scales with $VCCS = n(n-1)$. Furthermore this coupling heat flux is not instantaneous, but depending on the relative distance between the channels there will be a delay on the coupling. This delay is modelled as a first-order exponential function by adding appropriate capacitive and resistive elements to the VCCS circuit. The comparison between simple resistive coupling and full VCCS coupling is shown in Fig.9, where it becomes obvious that if all channels are activated simultaneously, there simply flows no current in the coupling resistors, and the results are inaccurate as expected.

2) *Application to 8 channel DWDM*: In Fig.10 the proposed coupling method is shown for the 8 channel filter. A total of 56 VCCS coupling circuits are used, which can be determined from the scaling law mentioned in the previous section. The traditional resistive coupling is also shown for reference, where each device model is connected through a single RC component. The resulting compact RC-model is now compared with the reference FE-model. In Fig.11 the steady state calibration of the RC-model is shown, and in Fig.12 the dynamic calibration is shown. For the steady state

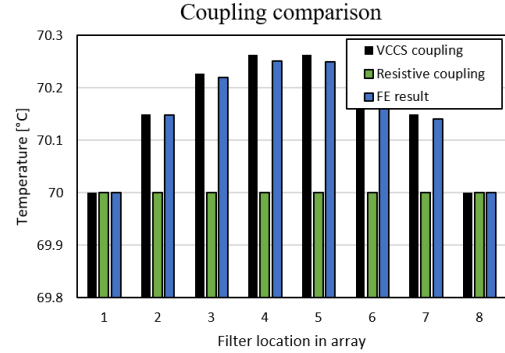


Fig. 9. Comparison between resistive coupling and VCCS coupling when all channels are activated simultaneously.

calibration the first channel of the filter is activated and the temperature of all the neighbors is calculated through the thermal coupling. A perfect match between FE and RC-VCCS model is obtained. In Fig.11 and Fig.12 also the RC-resistive result are shown: the simple resistive coupling works for the main channel and first neighbor, but underestimates the coupling to further neighbors significantly. For the dynamic calibration, a heater step function is applied to the first channel and the time evolution of all channels is calculated. The step response of the neighbors is not subjected to the spectral analysis in Section II.B because it can be approximated as a first-order exponential very accurately. This is because the response time is governed by the amount of SiO₂ between the channels and the heat flow is quasi one-dimensional. The time constants of the neighboring channels are shown in Table II. Up to two decimal places, there is no difference between the time constants for cross-talk with and without trenches and the introduction of UCUT only increases the time constants with ~1%. Important to note here is that the time constant of cross-talk is in the millisecond range, which is two to three orders of magnitude larger compared to the direct heating of the device. With these values, the parameters of the VCCS coupling circuits can be determined. To start off, the VCCS gain can be found from the steady-state FE simulation (Fig.11): the coupling of the neighbor is normalized and expressed as a fraction (between 0 and 1). The gain G will determine the amount of heat flux the VCCS puts out $\dot{q} = G \cdot T_{sense}$, where T_{sense} is the sensed temperature. The unit of the gain is mW/°C, so an extra step is required to go from the non-dimensional coupling to the gain $G = C/\eta$, where η is the heater efficiency expressed in °C/mW. As the next step, $R_{1,2}$ and C need to be determined (Fig.8). These circuit elements are added to model the time delay of the thermal coupling between neighbors. The resistances $R_{1,2}$ are chosen arbitrarily, are equal and at least 6 orders of magnitude larger than the other resistances in the network. The reason for this is that each VCCS circuit models uni-directional coupling, so backflow of heat flux needs to be prevented, otherwise the capacitor in the VCCS circuit will charge up when it should not. By using a sufficiently high resistance in the coupling network, these issues are prevented. The high resistance is not an issue for the VCCS itself, as it is

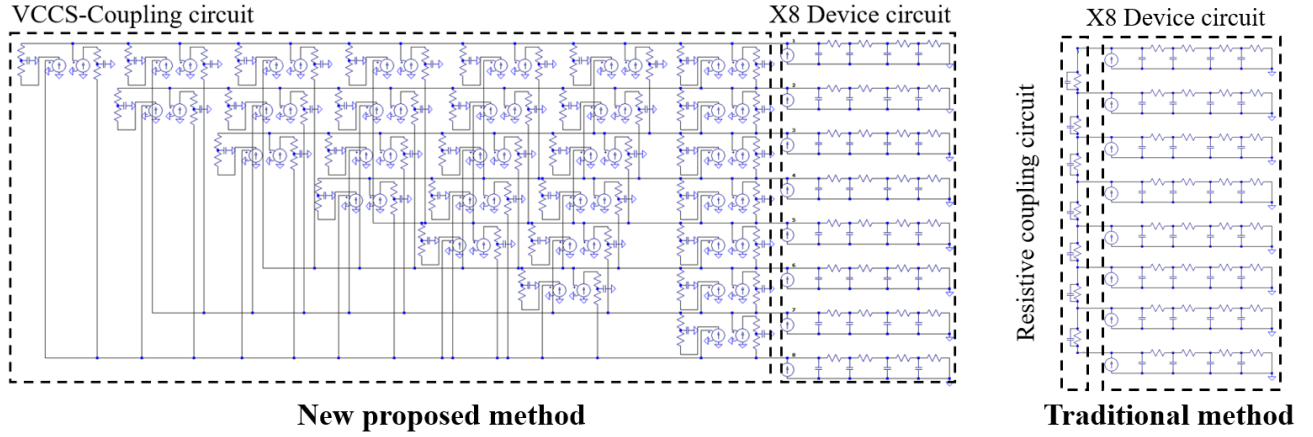


Fig. 10. Fully coupled RC-network of 8 channel DWDM ring filter array. New proposed method with VCCS coupling circuit (left) and traditional resistive coupling (right).

TABLE II
TIME CONSTANTS OF NEIGHBORING CHANNELS

	Time constants [ms]						
	τ_1	τ_2	τ_3	τ_4	τ_5	τ_6	τ_7
Time UCUT	4.14	5.67	6.57	7.21	7.82	8.48	8.99
Time UCUT+trench	4.16	5.67	6.57	7.21	7.82	8.48	8.99
Time no UCUT	4.09	5.55	6.47	7.12	7.64	8.35	8.87

current-controlled and will generate the required voltage to overcome the high resistance. Finally, the capacitance C of the VCCS network can be determined by the time delay of the neighbor (Table II), as $C = \tau/R_{1,2}$.

The full circuit dynamic FE simulation takes 5.5 hours to resolve a single heater step using 30 time steps. The compact RC-model accomplishes the same results in less than one second. This highlights the strength of this approach: having an extremely fast circuit model opens up new possibilities for analysis which are not feasible with standard FE-models. In order to construct the compact RC-model, one full domain FE simulation has to be done for extracting the RC-components, which takes a considerable amount of time but has to be done only once. Circuit-level analysis is discussed in Section III.

III. ANALYSIS OF RESULTS

A. Device and circuit frequency response

In this part the analysis of the compact model is presented. First, the frequency response of the filter is calculated. This is particularly fast in circuit simulators as the problem is transformed from time domain to frequency domain, which is not possible in most FE solvers. The result is shown in Fig.13. The behavior resembles a low-pass filter. Due to the thermal inertia of the structure, the response to high frequency will be small. The thermal frequency response is important to determine in case the heater is driven by an AC signal or PWM signal. In those cases, even though the input power is not constant, the waveguide temperature should be isothermal and not fluctuate. In order to guarantee this, the

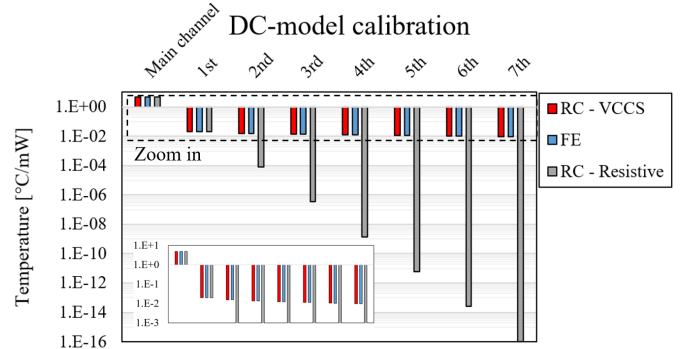


Fig. 11. Steady-state circuit calibration and comparison between FE-model and RC - VCCS model (a single heater is active). The RC - resistive coupling works for the main channel and first neighbor, but underestimates coupling to further neighbors.

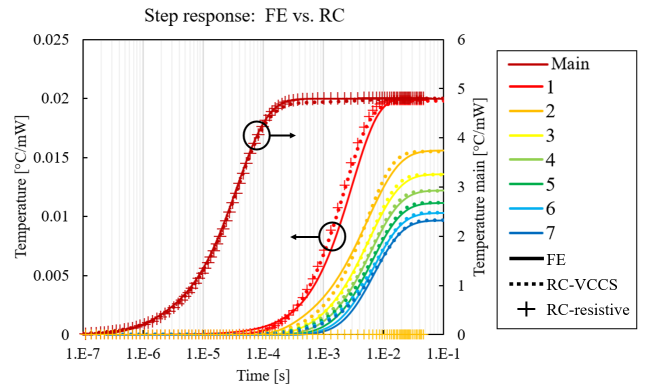


Fig. 12. Transient full circuit calibration and comparison between FE-model (solid) and RC-model (dots and crosses, a single heater is active).

drive frequency should be sufficiently high. For the filter under investigation, a drive frequency of 200 kHz corresponds with a response of -30 dB meaning that the amplitude of the fluctuations is 3 orders of magnitude lower compared to the low frequency behavior.

As a next step, the frequency response of the neighboring

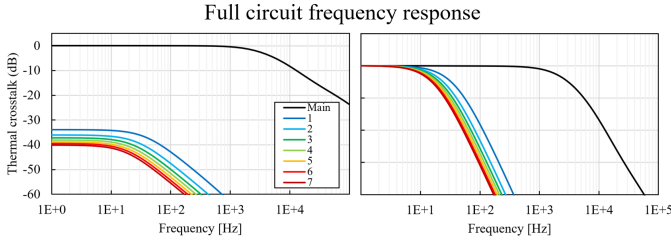


Fig. 13. Frequency response of full circuit, normalized (right)

channels is investigated. The first channel is driven with an AC-source with variable frequency and the response of the main channel itself is recorded, along with all 7 other neighbors. In Fig.13 (right) the responses are normalized. In an idealized case of one-dimensional heat spreading, there is a relationship between the thermal diffusivity α of the material, the time constant and the distance L at which the time constant is calculated [20]:

$$\tau = \frac{4}{\pi^2} \frac{L^2}{\alpha} \quad (4)$$

There also is a relationship between the time constant τ and the 3dB frequency (frequency at which 50% of the steady state response is obtained):

$$f_{3dB} = \frac{1}{2\pi\tau} \quad (5)$$

If Eq.4 and Eq.5 are combined, the expected $f_{3dB,i}$ of neighbor i is related to $f_{3dB,m}$ of the main heated channel:

$$\frac{f_{3dB,m}}{f_{3dB,i}} = \left(\frac{L_i}{L_m} \right)^2 \quad (6)$$

This relationship can be used to check if the simulated frequency response in Fig.13 corresponds to the theoretical value. The main channel is located at approximately $2 \mu\text{m}$ from the heat source and the first neighbor at $60 \mu\text{m}$. The 3dB frequency for the main channel is 30 kHz and the first neighbor 30 Hz, which matches well the theoretical value of 900 times lower f_{3dB} .

B. Dynamic start-up simulation

Circuit start-up is simulated by applying power to the heaters in all channels simultaneously. The resulting temperatures are shown in Fig.14 and two different dynamics can be distinguished. Device-level dynamics have a time constant of $40 \mu\text{s}$, while the circuit-level dynamics are much slower with a time constant of 4 ms. After zooming in on the results (Fig.14, right), it becomes apparent that the thermal coupling between the channels causes a DC offset of the steady state temperatures. The channels in the center of the filter array will reach a higher temperature due to thermal coupling. This can potentially be an issue if this temperature deviation becomes too large, which is further discussed in Section III.C. From this PIC thermal modelling result it is clear that there is a circuit-level thermal response on each device, due to the cumulative coupling from all neighboring devices. The extent of this cumulative coupling can be significant and

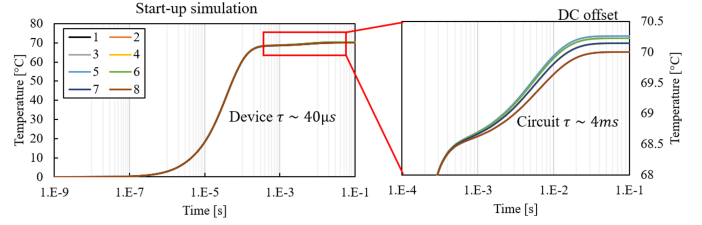


Fig. 14. Transient start-up simulation with compact RC-model

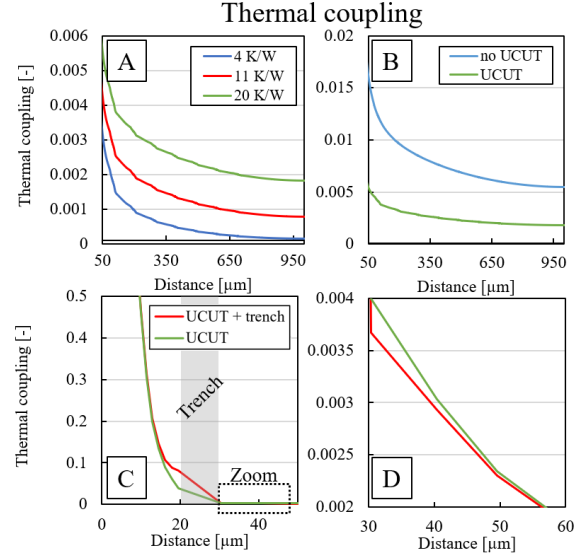


Fig. 15. FE simulation of thermal coupling. Thermal coupling for: (A) Different package thermal resistances, (B) UCUT and no UCUT, (C) trench and no trench, (D) Zoom-in at edge of trench

depends on boundary conditions, channel spacing, and location within the filter array. In this case, the cumulative coupling amounts to 2.8% and can not be ignored. Furthermore, due to the difference in coupling between the channels, they reach a different steady state temperature, which is an issue for temperature-locking the channels.

C. Thermal coupling

The thermal coupling or crosstalk is an important issue for resonance-based photonic devices. Single ring filters are extremely temperature sensitive, where a 0.1°C temperature shift from the operating point can already significantly degrade the optical performance [21]. Double ring filters are typically more robust as they have a flat-top transmission spectrum [12]. Thermal coupling between the channels causes temperature shifts (Fig.9) which can detune the filter. Other factors which can detune the filter include laser wavelength shift, dimensional tolerances of the ring waveguides and heat sources outside of the transceiver die. In the ideal case, there would be no thermal coupling and each channel would work independently. As thermal coupling can never be completely avoided, there should be methods implemented to handle the operation in a thermally-coupled environment. In order to calculate the thermal coupling between the channels, FE simulations are performed with varying boundary conditions.

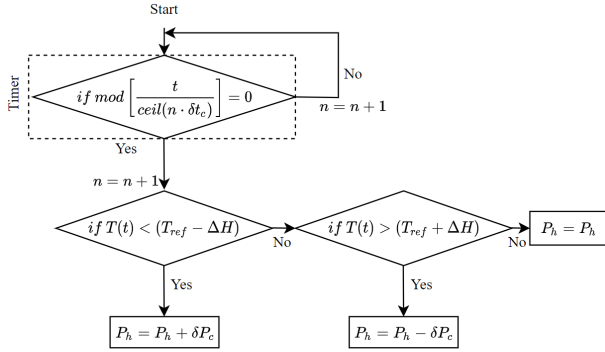


Fig. 16. Implemented tuning algorithm in compact circuit simulation

Thermal coupling is very sensitive to the type of package in which the die is assembled. In Fig.15 (A) the thermal coupling is shown for package thermal resistance values 4 K/W, 11 K/W and 20 K/W. The coupling is calculated as $C(x) = T(x)/T_{max}$ in function of the lateral distance x from the heater. In Fig.15 (B) a comparison of thermal coupling for the case with and without UCUT is shown (20 K/W package). With UCUT, the coupling is much lower, mainly due to the higher maximum temperature T_{max} at the active device. The effect of insulation trenches on coupling is shown in Fig.15 (C) (for 4 K/W package case): to the left of the trench the temperature increases due to the added insulation. A zoom in at the outside edge of the trench (Fig.15 (D)) reveals that the trench lowers the coupling with $\sim 10\%$ close to the trench, and this effect fades for distances larger than 50 μm . From this it is concluded that trenches are only useful for short range thermal coupling mitigation. For long range (50+ μm) the heat spreading in the Si substrate plays an important role, which is unimpacted by the trenches.

D. Thermal tuning

In this last section of this paper the implementation of a thermal tuning framework within the compact model is discussed. Based on typical wavelength locking schemes [21]–[23] a tuning algorithm is proposed (Fig.16). It works as follows: at a predefined timestep δt the optical power coupled in the ring filter is evaluated: if there is a deviation from the nominal working condition, the tuning control circuit will send an increased or decreased current to the heater. The control time interval δt is a first important tuning parameter. In general, it should be smaller than the time constant of the aggressor profile. At these instances, the controller checks if the temperature T of the ring is below the reference temperature minus hysteresis $T_{ref} - \Delta H$. The magnitude of the hysteresis depends on the allowed temperature drift of the filter, which is linked to the 3 dB bandwidth. As an example, a hysteresis of 0.1°C is used. If the temperature drops below this threshold, the heater power is increased with a small step δP , the second important tuning parameter. If this is not the case, it is checked whether the temperature is higher than the reference temperature plus hysteresis. If this is true, the heater power is decreased. Lastly, if this is not true, the heater power stays constant. The proposed tuning algorithm

is rudimentary, but can be expanded in order to incorporate more advanced PID control.

In order to test this tuning algorithm and ensure wavelength locking, the compact model is expanded with additional heat sources which mimic the fluctuating environmental temperature. This is typically called the aggressor profile or power. For the current test case, a total of 30 seconds is simulated while an aggressor profile with a 1 second time constant causes temperature fluctuations up to 5°C. The aggressor profile is chosen arbitrarily, and it can be described by first-order exponential response functions:

$$T(t) = \begin{cases} T_{ss}(t) \cdot \left(1 - e^{-\frac{(t-nt_p)}{\tau}}\right), & \text{if } \frac{dT}{dt} > 0 \\ T_{ss}(t) \cdot \left(e^{-\frac{(t-nt_p)}{\tau}}\right), & \text{if } \frac{dT}{dt} < 0 \end{cases} \quad (7)$$

Where T_{ss} represents the steady state temperature, n is the period number and t_p is the period duration. The aggressor power and temperature are shown in Fig.17. The channels are first simulated under the aggressor profile without tuning (Fig.17, upper-right). If no thermal tuning is implemented, the temperature of the channel will simply follow the environmental fluctuations. When the thermal tuning is implemented with a hysteresis of 0.1°C, the (blue) temperature is obtained. When two subsequent zoom-ins are done, more details on the control power become visible (Fig.17). In this simulation, a control timestep of 10 ms is chosen, which is the fastest time the circuit can react to temperature changes, along with a 0.01 mW heater power increase or decrease.

IV. CONCLUSION

Simulating traditional finite element circuit-level thermal models of PICs is very time-consuming and hence impractical. This is the motivation for introducing a compact thermal model, based on a thermal RC-network. In this work, the methodology for obtaining such a compact RC-model for an 8-channel DWDM filter is shown. We start from a high-fidelity finite element simulation of the PIC and use the simulation result for the calibration of the R and C components. The computational time required to solve the response to a heater power step function is reduced from 5.5 hours to less than 1 second. This opens up possibilities for thermal circuit-level analysis which would be infeasible with just the finite element model. For example, device and circuit thermal frequency response can be calculated. Thermal coupling and tuning of the different photonic devices can be analyzed and optimized. New thermal tuning control algorithms can be tested through simulation of the circuit, which allows to assess the tuning parameters within a theoretical framework.

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REFERENCES

- [1] Philippe P. Absil, P. Verheyen, P. De Heyn, M. Pantouvaki, G. Lepage, J. De Coster and J. Van Campenhout, “Silicon photonics integrated circuits: a manufacturing platform for high density, low power optical I/O’s”, *Optics Express*, vol.23, No.7, Apr. 2015, doi:10.1364/OE.23.009369.

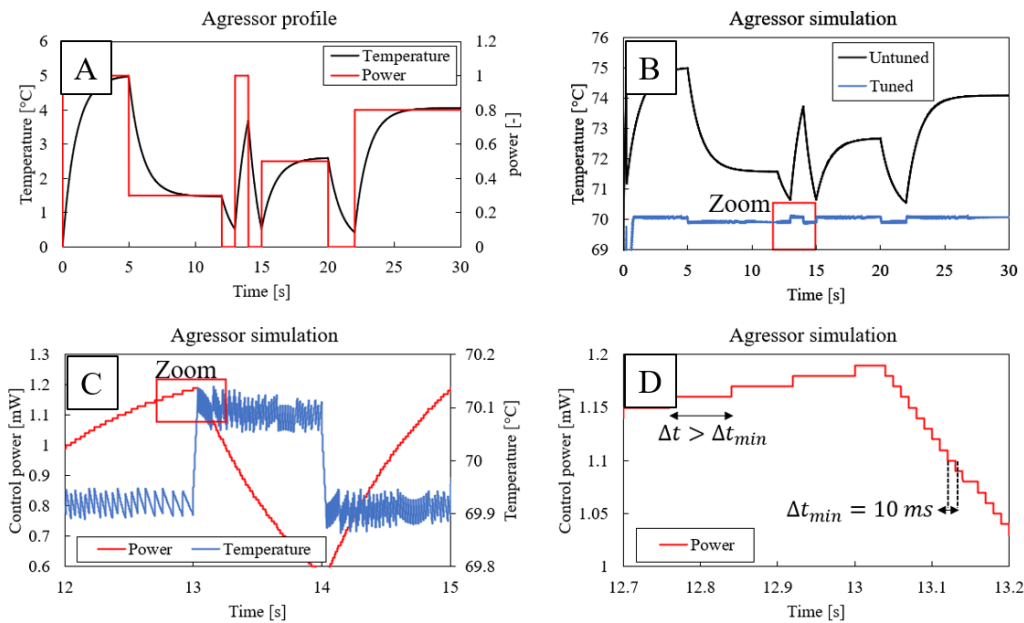


Fig. 17. Simulation of tuned circuit under influence of aggressor power and temperature fluctuations. (A) Shows the power of the aggressor and the corresponding ambient temperature fluctuations. (B) Shows the effect on the PIC: the temperature of the tuned and untuned channel. (C) Is a zoom-in detail of (B) and (D) is a second zoom-in, showing the control power.

- [2] M. Rakowski et al., "Hybrid 14nm FinFET - Silicon Photonics Technology for Low-Power Tb/s/mm² Optical I/O," *Symposium on VLSI Technology Digest of Technical Papers*, 2018.
- [3] A. Masood et al., "CMOS-compatible Tungsten Heaters for Silicon Photonic Waveguides," *9th International Conference on Group IV Photonics*, 2012.
- [4] A. Masood et al., "Comparison of heater architectures for thermal control of silicon photonic circuits," *10th International Conference on Group IV Photonics*, 2013.
- [5] Y. Xie et al., "Thermally-Reconfigurable Silicon Photonic Devices and Circuits," *IEEE Journal Of Selected Topics In Quantum Electronics*, Vol. 26, No.5, Sep. 2020.
- [6] I. Shubin et al., "Integration, processing and performance of low power thermally tunable CMOS-SOI WDM resonators," *Optical and Quantum Electronics*, Vol.38, Apr. 2012, doi: DOI 10.1007/s11082-012-9577-9.
- [7] Q. Fang. et al., "Ultralow Power Silicon Photonics Thermo-Optic Switch With Suspended Phase Arms," *IEEE Photonics Technology Letters*, Vol. 23, No. 8, pp. 525-527, Apr. 2011.
- [8] A.H. Atabaki, E. Shah Hosseini, A.A. Eftekhar, S. Yegnanarayanan and A. Adibi, "Optimization of metallic microheaters for high-speed reconfigurable silicon photonics," *Optics Express (OSA)*, Vol.18, No.17, Aug. 2010.
- [9] C. T. DeRose et al., "Thermal Crosstalk Limits for Silicon Photonic DWDM Interconnects," *IEEE Optical Interconnects Conference*, 2014.
- [10] F. Christiaens, B. Vandeveld, E. Beyne, R. Mertens, J. Berghmans, "A generic methodology for deriving compact dynamic thermal models, applied to the PSGA package," *IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part A*, Vol.21, No.4, pp.565-576, Dec. 1998.
- [11] Michal Rakowski et al., "A 4x20Gb/s WDM Ring-Based Hybrid CMOS Silicon Photonics Transceiver," *IEEE International Solid-State Circuits Conference*, Feb. 2015.
- [12] Peter De Heyn et al., "Fabrication-Tolerant Four-Channel Wavelength-Division-Multiplexing Filter based on Collectively Tuned Si Microrings," *Journal of Lightwave Technology*, Vol.31, No.16, 2013.
- [13] Massoud Pedram, Shahin Nazarian, "Thermal Modeling, Analysis, and Management in VLSI Circuits: Principles and Methods," *Proceedings of the IEEE*, Vol.94, No.8, 2006.
- [14] T.Y. Wang and C.C.P. Chen, "SPICE-Compatible Thermal Simulation with Lumped Circuit Modeling for Thermal Reliability Analysis based on Modeling Order Reduction," *IEEE International Symposium on Quality Electronic Design*, March 2004.
- [15] L. M. Schlitt, P. Kalla and S. Blair, "A Methodology for Thermal Characterization Abstraction of Integrated Opto-electronic Layouts," *29th Int. Conf. on VLSI Design and 15th Int. Conf. on Embedded Systems*, 2016.
- [16] X. Wang and S. Mookherjee, "Fast circuit modeling of heat transfer in photonic integrated circuits," *CLEO (OSA)*, 2017.
- [17] D. Coenen et al., "Thermal modelling of Silicon Photonic Ring Modulator with Substrate Undercut," *IEEE Journal of Lightwave Technology*, Vol.40, No.13, pp.4357-4363, Jul. 2022.
- [18] Jecdec Solid State Technology Association, "Transient Dual Interface Test Method for the Measurement of the Thermal Resistance Junction to Case of Semiconductor Devices with Heat", 2010.
- [19] M. P. Gupta, A. K. Vallabhaneni and S. Kumar, "Self-Consistent Electrothermal Modeling of Passive and Microchannel Cooling in Al-GaN/GaN HEMTs," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, Vol.7, No.8, pp.1305-1312, Aug. 2017.
- [20] K. R. Bagnall and E. N. Wang, "Transient Thermal Dynamics of GaN HEMTs," *ITherm Conference*, 2016.
- [21] S. Agarwal, "CMOS Circuitry for the Wavelength Locking of a Ring-based Silicon Photonics Transmitter," Ph.D. Thesis, Dept. of Elec. Eng., KU Leuven, Belgium, 2018.
- [22] Chen Sun et al., "A 45 nm CMOS-SOI Monolithic Photonics Platform With Bit-Statistics-Based Resonant Microring Thermal Tuning," *IEEE Journal of Solid-State Circuits*, Vol. 51, No. 4, 2016.
- [23] M. Milanizadeh, D. Aguiar, A. Melloni and F. Morichetti, "Cancelling thermal cross-talk effects in photonic integrated circuits," *Journal of Lightwave Technology*, Vol.37, No.4, pp.1325-1332, Jan. 2019.