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Challenges of Wafer-Scale Integration of 2D Semiconductors for High-Performance Transistor Circuits

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Large-area 2D-material-based devices may find applications as sensor or photonics devices or can be incorporated in the back end of line (BEOL) to provide additional functionality. The introduction of highly scaled 2D-based circuits for high-performance logic applications in production is projected to be implemented after the Si-sheet-based CFET devices. Here, a view on the requirements needed for full wafer integration of aggressively scaled 2D-based logic circuits, the status of developments, and the definition of the gaps to be bridged is provided. Today, typical test vehicles for 2D devices are single-sheet devices fully integrated in a lab environment, but transfer to a more scaled device in a fab environment has been demonstrated. This work reviews the status of the module development, including considerations for setting up fab-compatible process routes for single-sheet devices. While further development on key modules is still required, substantial progress is made for MX_2 channel growth, high-*k* dielectric deposition, and contact engineering. Finally, the process requirements for building ultra-scaled stacked nanosheets are also reflected on.

1. Introduction

Traditional Si-channel scaling is hitting performance limitations at gate lengths ≈18 nm, necessitating creative solutions in device design, material engineering and circuit and system optimization: for examples the introduction of fin field-effect transistors (finFETs), nanosheets and Forksheet devices.[1–3] Further scaling of Si-based devices below 10 nm gate length is becoming challenging due to reduced channel control.[1–3] At these gatelengths sub 5 nm thick Si channels are required. Both process-induced Si consumption and the changing behavior of ultrathin Si channels can limit the channel thickness scaling.

Today, the main contenders that allow the extension of the roadmap to smaller devices are semiconducting 2D materials.[1–3] These materials are referred to as van der Waals layers, due to their atomically layered structure and fully passivated surface, which enable them to have improved short channel behavior. A single monolayer has a channel thickness below 1 nm.

Graphene is the most studied material among the different classes of 2D materials.[4] While the absence of a bandgap renders it non-suitable for transistor application, properties such as superior electron and hole mobilities, carrier density modulation by gating, which are possible due to its unique band structure, that is, Dirac cone, makes it particularly interesting for optical applications. Therefore, this material, along with other 2D materials, has found an application space in sensor, optical and photonic devices.

These applications typically rely on a hybrid integration of scaled Si-based devices at the bottom, that provide the required drivers and read-out circuitry, with larger 2D-based devices on top. In most of these implementations, including for full wafer integration, lift-off processes are frequently used for the contact and gate patterning.[5] This offers some advantages like not requiring highly selective etches stopping on the sub 1 nm thick 2D layers. Due to larger feature sizes of the optical and sensor devices lift off processes can still be applied provided low temperature metallization is used.

Here, we focus on the use of 2D materials as a replacement for Si in scaled high-performance logic applications, which narrows down the choice of 2D materials to semiconducting channels, additional factors including the electronic conductivity type, the bandgap, mobility, etc.[6] Among the semiconducting 2D materials, black phosphorous and transition metal dichalcogenides (TMDC) that consist of a transition metal atom M (Mo, W, etc.) and a chalcogen atom X (S, Se, or Te) in an MX_2 configuration, have received most attention for use in high-performance transistors.[1] The reactivity of black phosphorous toward ambient and the consequent instability makes MX_2 materials, which are relatively more stable, the primary focus of the experimental 2D-materials-based high-performance transistor research.

Most current 2D material device demonstrators, including some top-performing ones are built using common lab integration techniques like local flake transfer and customized e-beam printing. They allow for illustrating the performance potential of MX_2-transistors but are not always compatible with fab-based wafer level production. In analogy to the graphene case, lift-off is frequently used for device demonstrators with relaxed feature sizes. It is however debatable whether lift-off can still be used reliably for the feature sizes around or below 10 nm needed for the future scaled logic. Besides the small feature size itself, the

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higher temperature typically used for the advanced metallization of small and high-aspect ratio trenches, will limit the possibility to use lift-off.

We reported earlier on a 300 mm full wafer process flow without lift-off for the integration of single layer planar logic 2D material devices.[7,8] Here more conventional damascene contact and gate process are used. The process might not be compatible with devices larger than a few 10 μm^2, since gate rip-out has been observed during gate chemical mechanical polishing (CMP) for these large square gate areas.[8] This should however not be a concern for scaled logic devices that are much smaller.

Assuming MX_2 channels will be introduced in high-performance transistor production, it is expected this happens after the introduction of Si-based stacked nanosheets, where MX_2-nanosheets will replace the Si nanosheets.[3,9]

For both Si- and MX_2-based devices, the stacking of the sheets allows a larger effective width for a given standard cell area footprint.[2] We estimate device features of metal pitch 16 nm and gate length 14 nm to be considered at the introduction point. In combination with the expected short channel improvement due to the scaling of the channel thickness and dielectric constant, the use of these ultra-thin stacks also offers a parasitic capacitance benefit, leading to a significant performance gain in the power performance area (PPA) technology metric.[2]

A particular implementation of a stacked MX_2 device-based inverter with four MX_2 layers, as virtually processed using SEMulator3D, is shown in **Figure 1**.[10] For better visibility, the MX_2- layers are simulated out of scale (2 nm instead of ≈0.7 nm for WS_2).

In the next section we will describe the used integration approach for the planar full wafer integration with special focus on the attention points for MX_2 integration, the remaining technology gaps, and possible solutions.

In the final section the developments required to replace the Si-based stacked nanosheet by a 2D material-based version will be discussed.

2. Wafer-Scale Integration of Single-Sheet 2D

Despite the final device target of stacked 2D material nanosheets, evaluation of important process understanding and integration aspects can already start from the integration of a single MX_2 sheet since the initial requirements are comparable to those for stacked nanosheet devices. Due to the less complex integration of a single nanosheet the learning cycles are also shorter.

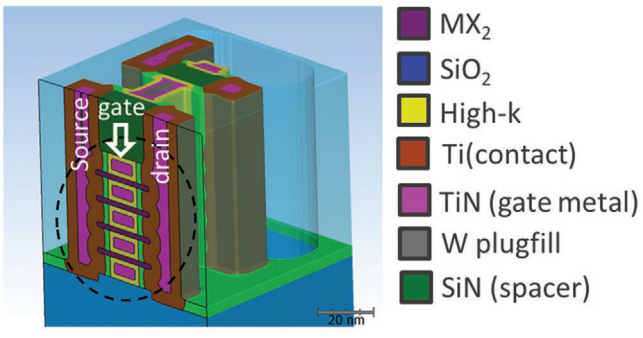

Figure 1. Example of a stacked MX_2 device-based inverter with four MX_2 layers, as virtually processed using SEMulator3D.

The first critical points to address are material selection, adhesion aspects, and deposition approaches for MX_2 channel and high-*k* dielectrics. Extra constraints are introduced by the integration in a 300 mm front-end Fab environment where most of the required equipment is shared with other applications. Dedicated equipment cannot be excluded in the final production process but is rarely used in pilot lines. Therefore, if a tool is used for baseline Si and MX_2 processing without extra checks in between, cross-contamination to other wafers needs to be avoided. Precaution needs to be taken to ensure that the newly introduced materials do not degrade the performance of regular Si devices, and cross contamination-induced process drifts are to be avoided. Thus, among the materials to be introduced, the preference is to use elements that have a history of semiconductor processing and have existing handling procedures. This is even more important in case the hybrid integration of Si- and MX_2-based devices is considered. Finally, safety aspects also strongly affect the material selection.

The key MX_2 candidate materials with expected higher mobilities and chemical stability are WS_2, MoS_2, $MoSe_2$ and WSe_2.[6–14] Sulfur-based gases are commonly used in semiconductor processing (e.g., etch gasses) and W and Mo are already used in the middle-of-line processing. Tellurides and selenides require more caution because of their high toxicity and introduce not only a risk during the deposition process itself but also by outgassing of the deposited layers.

Most MX_2 device data from literature reports focus on MoS_2 and WS_2.[1,8,15–22] For our pathfinding, we opted for the use of WS_2 because of the expected higher mobility based on theoretical calculations, though in integrated devices MoS_2 seems to outperform WS_2.[8,14]

2.1. Single-Sheet Process Flow and Adaptations for MX_2 Material Properties

An in-line transmission electron microscopy (TEM) example of a partially processed double gated WS_2 transistor, fully integrated in a 300 mm cleanroom, is shown in **Figure 2**. This side contacted WS_2 transistor has a back and top gate made of TiN with HfO_2-based gate dielectrics. The side contact has also been referred to as edge contact and corresponds to a contact where the contact metal bounds to the crystal edge of the MX_2 material.

The TiN gate material and Ti\TiN contact materials were selected based on fab and Si process compatibility and are likely not optimal for performance. Semimetals like Bi or Sn and Pt are expected to be considerably better contact metal candidates for N and PMOS channels, respectively.[14,22,23] These material choices are less compatible with front-end Si processing. As an example, the use of Pt in a fab is not likely due to the possible detrimental effect on Si devices and the difficulty to avoid cross-contamination. Once tools are contaminated, removal of the eventual Pt contamination it is very difficult due to its inert nature.

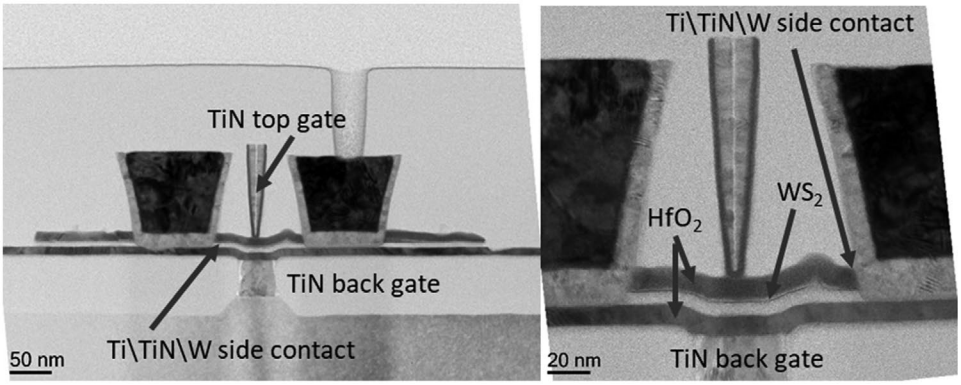

Figure 2. Left: In-line TEM of a partially processed double gated WS_2 transistor with TiN top and back gate. The channel, contacts, and the top and back gate are already present. Right: Enlarged TEM of the channel area.

The schematic process flow is shown in **Figure 3** and has been explained in more detail elsewhere.[8,15–18,24] Due to the specific properties of MX_2 materials and in particular the reduced adhesion, the sensitivity to liquid intercalation and the sub 1 nm thickness of the channel, specific adaptations of the process flow are required.

During the first module (Figure 3A) a local TiN back gate is made. In the next steps the HfO_2-based bottom dielectric layers are deposited, followed by the WS_2 formation and the top gate HfO_2 dielectric growth. The top gate dielectric and the WS_2 channel are patterned at the same time (Figure 3B), followed by the contact formation (Figure 3C,D). The contact formation consists of a trench etch in SiO_2, stopping on the top HfO_2, followed by a side contact etch through the top high-*k* and the WS_2 itself. Finally, the contact trench is filled with Ti\TiN\W using a fill and metal CMP process. The gate-last top gate processing (Figure 3E) consists of a SiO_2 trench etch stopping on the top HfO_2, followed by the metal gate TiN\W fill and CMP. Another layer of HfO_2 is deposited in the trench prior to the top gate deposition to avoid contact between the top gate and the channel at the edge of the active area in the gate overlap region. Note that the contacts and top gate are based on a damascene approach that is the industry standard for scaled devices. The final via and metal 1 module are implemented with another industry standard processes (Figure 3E).

As described above the specific properties of MX_2 materials were considered in the elaboration of this process flow. Due to the limited etch selectivity in the process to the ultrathin WS_2 channel, the $WS_2\backslash HfO_2$ stack is etched as a whole. Using the HfO_2 as an encapsulation layer, the HfO_2 protects the monolayer thick WS_2 surface from oxidation or damage during the dry etch or post etch strip. Because of the sensitivity to liquid intercalation-based delamination no wet strip is applied after the active, contact, and top gate etch. This could cause delamination and possible lift-off of the smaller active areas.[15] In general, any wet processing on open MX_2 edges is avoided and it is only applied when the MX_2 edges are covered by another material.

Non-liquid-intercalation-based delamination of the MX_2 materials is another concern. The van der Waals nature of MX_2 materials and weaker adhesion to surrounding materials compared to those typically used in Si processing is the primary

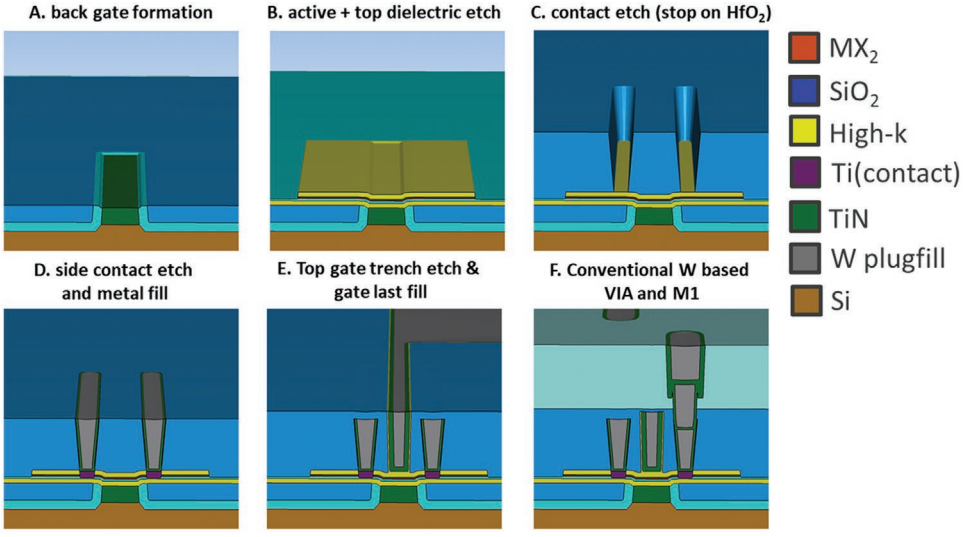

Figure 3. Simplified presentation of the process flow used to make the double-gated transistors.

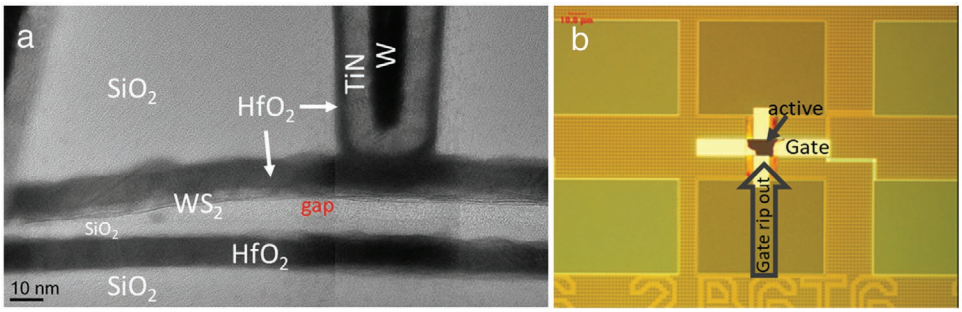

Figure 4. a) TEM of a 1 µm-long WS_2-based device that delaminated during the sample preparation, b) optical microscopy inspection after top-gate CMP showing rip out of the 20 × 10 µm top gates.

cause.[8] This is illustrated in **Figure 4**a that shows a TEM of a 1 µm-long WS_2 device. The delamination at the bottom SiO_2–WS_2 interface occurred during the double-sided ion beam milling during the TEM specimen preparation but illustrates the weakness of the bonding of the MX_2 to the neighboring materials.

The weaker adhesion of MX_2 materials also reduces the allowed stress and strain in the materials in contact with it. For too high stresses the shear force could dissociate the MX_2 from the surrounding material. Therefore, the oxide hard mask, commonly used for small area patterning, was replaced by a low-stress Spin-On-Carbon Spin-On-Glass hard mask during active patterning.[17] Since the stress-induced forces are proportional to the surface area, the initial active patterning where the whole wafer surface is covered with MX_2, is the most sensitive to delamination, the situation being more favorable after active area patterning when the MX_2 is present in the form of smaller areas. The active area is hence patterned as soon as possible.

Mechanical force-induced delamination is also observed after top gate CMP for larger gates, as illustrated in Figure 4b for 20 × 10 µm transistors. This will not necessarily be an issue for small high-performance transistors but might limit the co-integration of larger features.

The effect of mechanical stress and possible delamination is to be reviewed for each new process step. For example, no spacers are used in the current process flow to avoid the typically higher stresses of the SiN used for that purpose.

Three key process steps that need improvement can be identified in the transistor fabrication process: MX_2 growth and patterning, high-*k* dielectric deposition, and contact formation. Below, we will describe our interpretation of the current development status of these key process modules and comment on the missing gaps needed to achieve a fully successful MX_2 integration. At the expected insertion node, a device with a single or at most bilayer of MX_2 layer will be required with a high-*k* layer having an equivalent oxide thickness (EOT) of ≈1 nm, and a contact resistance below 100 Ω µm.

2.2. MX_2 Growth and Patterning

The single or bilayer channel is required to achieve sufficient electrostatic control over the entire channel and additionally the band structure of the material depends on the number of MX_2 layers present. A deposition method for single or bilayer 2D will hence be needed.

The most wafer-scale integration-friendly deposition methods are blanket full wafer depositions. Though other deposition methods are studied, currently the best full wafer results are obtained using chemical vapor deposition (CVD) MX_2 deposition.[2–13,15–26] Ideally a monolayer or bilayer of monocrystalline MX_2 should be grown that covers the entire 300 mm wafer area. In practice however, CVD methods grow a polycrystalline sheet of coalescing MX_2 with an occasional thicker layer overgrowth. An example is shown in **Figure 5**A that features a 300 mm wafer after CVD WS_2 growth using a $W(CO)_6$ and H_2S-based metal–organic (MO)CVD process.[25] When the grain boundaries within the first MX_2 layer occur within the device dimensions, they are expected to affect the effective mobility. Hence many 2D CVD growth research focuses on the increase of the grain size of the first layer, though some polycrystallinity might have to be accepted as a compromise to achieve full wafer growth. The overlayer growth is also expected to modify the device electrostatics, so it has also to be avoided or at least reduced to a level that device yield is not affected. The higher layer overgrowth occurs because of WS_2 nucleation on the initially grown material during the closure of the first layer and the higher layer crystals grow to a larger size because of the iso-material template layer below.

Reaching a single layer MX_2 growth with a sufficiently large grain size and limited overgrowth will be a key challenge for MX_2-based devices. The key resides in the appropriate control of MX_2 nucleation and lateral growth. Process parameters that can be used to tune the obtained morphology are deposition temperature, pressure, time, and precursor selection. Higher growth temperatures promote larger MX_2 grain sizes, while for lower growth temperatures smaller grains and some more out-of-plane growth is also observed.[17] The temperature can be lowered even further using an atomic layer deposition (ALD) process, but the grain size is even smaller, and the overgrowth is harder to contain.[16,27,28] The precursor selection can also be adapted to limit the nucleation of the first and/or the higher layer overgrowth and promote the lateral growth of the already formed grains.[29–35]

The upper temperature allowed will depend on the preceding processing and hence also the target application due to possible degradation of the underlying stack (e.g., wafer bending or crystallization of the underlying materials). In case of back end of line (BEOL) integration of 2D the temperature will be limited to

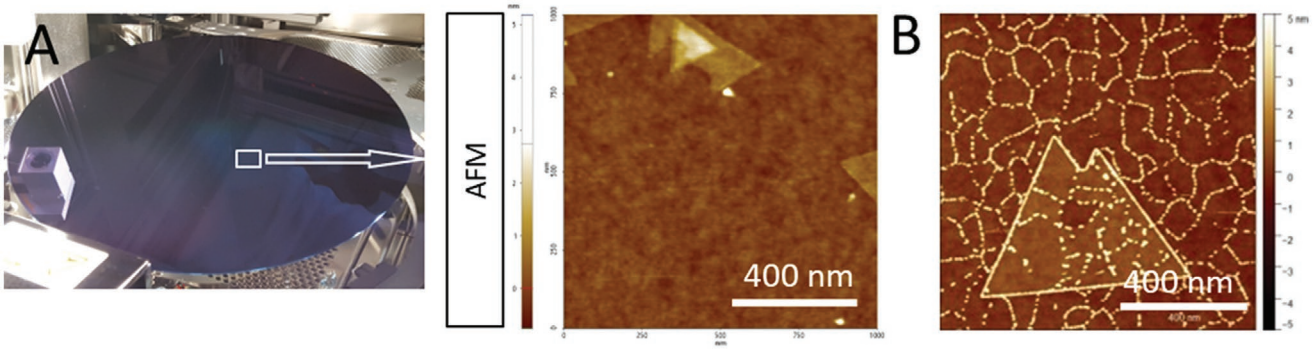

Figure 5. A) CVD WS_2 growth (non-optimized process) on a 300 mm wafer and the resulting surface morphology at 750 °C growth temperature. The first layer consists of coalescing in-plane crystals, though the grain boundaries are hard to distinguish in atomic force microscopy (AFM). Larger in-plane 2nd and higher layers overgrowth is also observed. B) AFM image of the WS_2 surface after the initial cycles of ALD AL_2O_3 growth.

500 °C. In case of front end of line (FEOL) integration typically somewhat higher temperatures are allowed.

The grain size can also be increased by using an appropriate crystalline template substrate like sapphire.[36] This implies the grown MX_2 will have to be transferred to 300 mm device wafers.[18] The transfer process involves an initial transfer of the MX_2 to an intermediate glass wafer and the final transfer to the target device wafer. A demonstration of the corresponding full 300 mm transfer process, with the source wafer in Si, is described in ref. [37]. Today, full 300 mm sapphire wafers are available, allowing wafer level templated growth. While in general we do not consider 300 mm MX_2 transfer as the preferred approach for MX_2 integration, it can be an option for specific single-sheet hybrid integration cases, where the transfer is enabled on smooth or planar surfaces. In case of logic only applications where the use of higher deposition temperature is tolerated, direct growth seems a better compromise.

Engineering challenges remain with MX_2 transfer: the complexity of the multi-step process, achieving within wafer uniformity, high sensitivity to particles and the final surface cleaning step. Specifically for pre-patterned wafers, the presence of step edges can cause voids or film rupture. Such sharp vertical edges can still occur at interfaces between different materials after CMP, used for planarization.

In case growth or transfer of a uniform single sheet of MX_2 with sufficiently large grain size cannot be obtained, a seeded localized growth can be considered.[1,14,20,21,38] In this approach closure of the entire layer is no longer targeted and growth conditions that promote lateral grain growth are used, resulting in larger grain local MX_2 crystals. A seed for growing the MX_2 crystal, that is centered inside the circuit or device area is used for selecting the target location.[1,14] Alternatively, the MX_2 material can also be grown in between the contacts, using the contact material as a seed.[20,21] For scaled nodes, where only limited crystal sizes will be needed this might be an interesting option. A disadvantage of this approach is a possible reduction in the overall wafer area usage. On amorphous substrates the crystals (e.g., triangular and hexagonal for WS_2 and MoS_2, respectively) grow arbitrarily in plane orientation. The usable wafer area for the device or circuit is hence limited to the inner inscribing circle of the grown crystal.

2.3. High-*k* Deposition

As described more in detail earlier we chose to protect the WS_2 from etch and or strip damage by capping the 2D with the gate high-*k* prior to active patterning. There are literature reports where direct patterning of the 2D material without high-*k* cap is used. The process of choice might depend on the sensitivity for plasma damage or oxidation of the used channel material and its thickness.

A high-*k* dielectric will be required to achieve the targeted ≈1 nm EOT target. The HfO_2 currently used for Si-based devices is the most likely candidate due to the maturity of the ALD deposition process used. The deposition of the high-*k* dielectric should not introduce detrimental interface traps in the MX_2 material. Like is the case for Si-based devices an interface trap free device will be difficult to achieve, and a compromise will have to be found between EOT scaling and interface traps. Additionally, the possible generation of interface traps can depend on the MX_2 material and might hence have to be optimized case by case.[39]

Hexagonal boron nitride has been used as a 2D dielectric to eliminate the generation of interface traps.[40] However, the low dielectric constant of h-BN is incompatible with a 1 nm EOT target and the required high-temperature growth is incompatible with full wafer integration. Other 2D dielectrics are proposed but these materials are entirely novel and the synthesis has to be fully developed for growth on a potentially 3D architecture, as will be described later.

In conventional Si-based device processing integration routes, the growth of high-*k* dielectrics by ALD on a Si-surface is preceded by a thin SiO_2 formation, to compensate for the absence of reactive sites on HF-last Si.[41] This hydroxyl functionalization of the surface eliminates island-like ALD growth and enables a more uniform nucleation and high-*k* growth. Due to the bulk nature of Si the band-structure of the underlying bulk Si is not disturbed by the surface modification.

An ideal MX_2 material has an intrinsically passivated surface and has no reactive surface sites and hence also no nucleation sites. It is indeed observed that the initiation of ALD high-*k* growth on MX_2 materials occurs on grain boundaries and localized nucleation sites.[42] This is illustrated in Figure 5B that shows an AFM image of the WS_2 surface after the initial

cycles of ALD Al_2O_3 growth. The high-*k* layers close by coalescence of the different grains after a sufficiently thick layer has been grown. This however results in local non-uniformity of the high-*k* thickness. The minimum thickness for layer closure is also unacceptably high for future nodes, for example, ≈20 nm in the case of ALD Al_2O_3. Unlike the case of Si, for a single layer of MX_2 the top surface cannot be converted into a functionalized 2D as it would modify the single layer of 2D present and destroy the band structure of the semiconductor. Therefore, an interface layer with uniform coverage on van der Waals surfaces, that can be deposited without damaging the underlying MX_2 layer is required. This interface layer must be sufficiently thin and/or have a sufficiently high-*k* value in order not to limit the EOT scaling needed for future nodes. Additionally, the deposition of the interface layer should not introduce detrimental interface traps.

Different approaches to realize this interface layer have been used with varying degrees of success.[42] The approaches can be summarized in four main categories: surface functionalization, low damage deposition, physisorption, and deposition of organic self-assembled monolayers.

In the case of surface functionalization, the top MX_2 surface is converted to contain reactive sites by, for example, chemical gas phase reaction, plasma, or UV–O_3 treatments. This method is likely not compatible with scaled nodes where the presence of single layer MX_2 is expected, the surface modification will modify the 2D material itself. This method can only work if perfect bilayers of MX_2 materials can be grown without higher layer overgrowth, which is a harder challenge than controlling a single-sheet MX_2 layer growth. Additionally, the converted MX_2 layer must have appropriate dielectric properties in order not to limit the EOT scaling.

In the case of low-damage deposition, a low-energy deposition process is used to limit the damage to the underlying MX_2. This has been successfully used for both Al_2O_3 and SiO_2 interlayers.[1,2,17,43] In all cases the low damage PVD deposition is followed by a controlled oxidation, resulting in an appropriate seed layer for further ALD high-*k* growth. These PVD like methods are compatible with planar single-sheet devices but will no longer be applicable for horizontally or vertically stacked MX_2 devices. In these cases, there will be no deposition on at least some surfaces where the deposition beam cannot reach.

Though not experimentally demonstrated on stacked devices, the physisorption-based interface layer and the low-temperature ALD, that is fundamentally the same, is more appropriate for a stacked layer configuration with areas that are not accessible for direct beam methods.[42–45] Such processes were applied successfully on single layer MX_2, using Al-based interface layers consisting of Al_2O_3 and AlN.[44,45]

The use of organic molecules like titanyl phthalocyanina (TiOPc) and perylenetetracarboxylic dianhydride (PTCDA) as nucleation layer has been demonstrated in literature.[46,47] Using vapor phase self-assembled PTCDA an EOT down to 1 nm EOT has been achieved for single-sheet MX_2 devices, a value consistent with the target values for scaled nodes.[46] Its application for stacked structures with less accessible MX_2 surfaces must be confirmed but is not intrinsically impossible. The thermal stability of these organic compounds during the post processing, that typically reaches 450 C during the BEOL processing, has still to be confirmed.

Conventional ALD-growth on polycrystalline MX_2 layers is enabled by nucleation at the grain boundaries which results in a local thickness variation of the fully grown high-*k* layer.[17] These local variations in the top high-*k* layer, shown in Figures 2 and 4, results in electrostatic variations and hence also in device variability.[16,40,48,49] Hence, high-*k* uniformity will be a strict requirement.

2.4. Contact Formation

In order not to limit the device performance a contact resistance below 100 Ω µm (same value as high-performance complementary metal–oxide–semiconductor (CMOS)) will be required for MX_2 devices along with higher mobility channels. For contacts using non-optimized metals the contact resistances are typically in excess of 1 kΩ µm range and therefore, typically one order of magnitude to high.

Per MX_2 material an optimal contact material is required matching the different band energies. Often, high Schottky barriers are measured. By considering the proper alignment of the Fermi level of the contact material to the conduction or valence band of the MX_2 for N and PMOS devices, respectively, a down selection of relevant contact metals is done. Metal reactivity and oxidation sensitivity are also taken into account. Another consideration of contacts to MX_2 materials has been Fermi level pinning (FLP), especially for MoS_2, where P-type conduction is very difficult to observe due to FLP near the conduction band edge; consequently, contact resistance to MX_2 doesn't merely follow the predictions from theoretical work-function arguments. However, some general trends can be observed, for example, MoO_x which has a work function of as high as 6.6 eV, has been shown to be a good candidate for P-type MoS_2.[50] The main contact metal candidates for P-channel metal–oxide–semiconductor (PMOS) MX_2 devices are noble metals like Pd, Pt, or Ru.[23,14,51] The best results have been obtained with Ru where a value of 2.7 kΩ µm had been observed.[14] A considerable gap to the target contact resistance remains. However, the acceptance of Ru is higher for semiconductor processing, since it is already implemented for the middle of line metallization and is being considered for buried power rails, nevertheless extra protocols to avoid cross-contamination might be required. Typically, it requires at least a partially separate toolset that is not used for FEOL Si-based processing. These constraints will be even stricter when Pd and Pt are considered.

The main contact metal candidates for N-channel metal–semiconductor (NMOS) MX_2 devices are: Ti, Ni, Au, and semimetals such as Bi and Sb.[3,14,23,52–56] Considering the fact that Au processing is typically banned in a Si-based fab, the introduction of Au would be accompanied by a very strict contamination protocol like is the case for Pd or Pd. The best contact results for NMOS so far were obtained with Bi and Sb contacts.[14,23] Among the NMOS contact metals Ti and Ni are easier to use in a fab environment since they are frequently used for Si-based contacts and for silicides. To allow maximal toolset flexibility in our integration we opted for an industry standard Ti\TiN contact, where Ti is the contact metal and the in situ TiN dep

serves to avoid the Ti oxidation.[14] A contact resistance in the range of 1.3 to 5 kΩ µm is obtained for Ti contacts to WS_2,[24] which is at the high end compared to 100–200 Ω µm for Bi and Sb recently reported.[14,23] Today, there is limited experience in fab processing for Bi and Sb. Due to their low melting point being 271 and 631 °C, respectively, the process window is very narrow and even below the BEOL temperature budget. Therefore, Sb with a melting point above that of the BEOL processing temperature is currently the preferred option.

Also, the contact resistance is not only affected by the contact materials but also by the contact configuration. For a single-sheet transistor with side contacts as shown in Figure 2 the contact area is small compared to conventional top contacts since it is limited to the thickness of the MX_2 layer. Variability in the etch process might also manifest itself as a variation in the contact resistance. Our experimental data indicate a good within wafer distribution of the obtained devices, but a full deconvolution of the channel and contact behavior could not yet be performed.[8,24] In the case of top contacts, a larger effective contact length can be obtained.[57] On the other hand, the bonding of the contact metal to the MX_2 might not be optimal in top contacts due to the presence of a possibly varying van der Waals gap.[58,59]

More experimental data will be needed to clarify which is the best contact configuration. Simulations indicate that the effective contact length for MX_2-based top contacts is rather small and that most of the injection of the current in the MX_2 happens at the contact-edge of the channel.[57] If this can be confirmed experimentally side contacts might be a good alternative for 2D-based devices.

Using an etch-based contact approach, either direct etch or damascene etch-based, side contacts are easier to implement since no etch selectivity is required toward the extremely thin MX_2 material. Etch and strip process chemistries that do not modify the surface and hence possibly affect the band-structure of the single layer MX_2 are to be developed. The fabrication of top contacts for single-sheet transistors is easier with lift-off, and this technique is hence regularly used for lab-based or large-area devices. This technique can however not be applied for highly scaled devices.

Despite the possibility to design using unipolar logic,[5] typical scaled logic circuits use CMOS to improve the area scaling. The doping techniques typically used for Si processing to produce the N and PMOS devices can no longer be used for MX_2-based devices making the process very complex. The needed N and PMOS devices can still be obtained by using different MX_2 materials that have an opposite conduction type. To obtain MX_2 materials of both polarities, different growth conditions will have to be applied at the same process height in the stack. This could be possible using selective growth, but that is currently not available and likely hard to achieve. Alternatively, a sequential deposition–etch–deposition–etch approach could be used to deposit the N and P MOS materials in their dedicated areas.

It has been demonstrated that different capping layers or gate dielectrics can also be used to dope the $MX_2$to the different polarities.[1] Similarly, a sequential deposition–etch–deposition–etch approach could be used to deposit the N and P MOS modifying dielectrics.

We believe implementing MX_2-based CMOS with the transistors in a single plane will involve deposition and etch of either the MX_2 material and/or the dielectric layers, will introduce a too high process complexity. Considering the monolayer nature of the MX_2, these etch processes will require extremely high selectivity, and likely require atomic layer etching. Therefore, this option is rather unlikely.

A last possible option for the N versus PMOS selection might be to use ambipolar material and different contact metals for the N and PMOS devices. This however relies entirely on the contact metal selection such that they have barrier heights that promote conduction in one of the device types while blocking the complementary one. Contact materials that satisfy these conditions while still providing low enough contact resistivity for a specific device polarity are to be identified.

3. Toward Stacked 2D

A more likely option for high-performance CMOS logic integration is to use the different N and PMOS MX_2 materials and or dielectrics in stacked planes on top of each other. Full wafer deposition or transfer can be used in that case and the localized selective etches or depositions are no longer needed. This approach was demonstrated using a sequential integration, where the N and PMOS transistors were integrated on top of each other.[60]

Taking into account the ultrathin body of the MX_2 channel and the expected projected footprint, device dimensions of 16 and 14 nm for metal pitch and gate length respectively, stacking of MX_2 sheets of the same polarity is required to enlarge the effective device width to sustain the needed current.[2] A similar stacking is already required for Si-based devices. In FinFET devices multiple fins are frequently used for a single device. Also, for nanosheets and complementary FET (CFET) devices that are currently in development, multiple sheets of silicon are considered.[61] Initial estimations indicate that about 4 to 8 stacked MX_2 sheets are needed to achieve the required performance.[2,62] For cases where more than 2 layers are required a more cost-efficient approach would be the monolithic integration approach. In this case the stacked MX_2 and (dummy) dielectric layers are grown on top of each other and etched in one step. This reduces the risk for misalignment of the superimposed transistors required for scaled nodes.

3.1. Stacking Orientation

The stacking of the MX_2 sheets can be implemented either in horizontal or vertical direction.[60,63] In lab environment horizontal monolithic stacking has been demonstrated for 2 layers, while vertical stacking has been demonstrated only morphologically.[60,63] Vertically stacked device integration is based on the formation of a dummy fin, where the MX_2 material is grown on the sidewall after which the dummy fin is subsequently removed. For the horizontally stacked devices we assume a monolithic approach considering the expected number of sheets. A SEMulator3D-based virtual process simulation was performed to compare both options. The schematics of the final

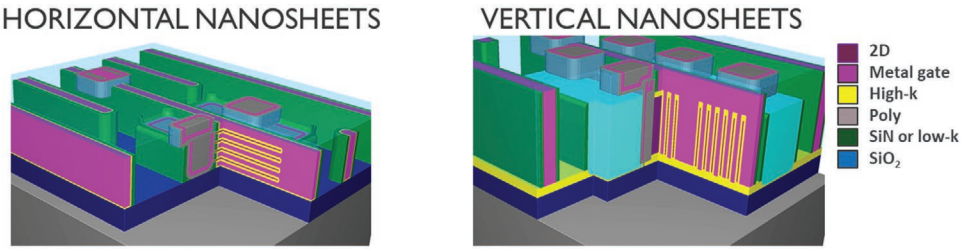

Figure 6. SEMulator3D-based illustrations of horizontal and vertically stacked nanosheets.

devices are shown in **Figure 6**. The advantages and disadvantages of both approaches are summarized in **Table 1**. Based on this assessment the horizontal stacking provides a better CMOS potential and scalability, which corresponds better with the expected introduction node. The improved scalability is due to the reduced sheet to sheet spacing, that is only limited by the minimal material deposition depth and/or the thickness needed to remove the sacrificial material when a replacement metal gate (RMG) is used. The horizontal stacking is also compatible with both the direct grown and the transferred MX_2, which is not the case for vertical stacking. Additionally, the horizontal configuration is more forgiving for morphological imperfections during the processing.

The horizontally stacked architecture of superposed N and PMOS sheets is currently being developed for Si-based CFET devices. In this device multiple NMOS and PMOS Si- or SiGe-based sheets are integrated on top of each other and some N to P device connections are moved in the vertical direction. It is expected that the introduction of MX_2 channels for high-performance transistors will happen after the introduction of the Si CFET in production, by replacing the Si-based sheets by MX_2 sheets[3,9] Provided the Si-based CFET development turns out to be non-realistic the replacement might also happen for the stacked nanosheet devices. Once the stacked MX_2-based devices are developed, it is expected that the methodology to stack them as a CFET device can be similar as for the Si-based case.

3.2. Process Challenges for Stacked MX_2 Integration

An example of a stacked unipolar MX_2-based gate-all-around device with four MX_2 layers, as virtually processed using SEMulator3D is shown in Figure 1. In the specific example an inverter like structure with two interconnected transistors and a common gate is shown. For better visibility, the MX_2- layers are simulated out of scale (2 nm instead of ≈0.7 nm for WS_2). This virtual processing assumes idealized process steps and ideal stack and material behavior, which is not always the case. Some of the involved processes did not yet reach maturity or must be fully developed. Nevertheless, this simulation is a useful aid to identify the expected process challenges and the existing gap.

Relying on the Si-based stacked nanosheet integration knowledge and replacing the Si-based sheets by MX_2 sheets seems a natural extension in terms of device structure.[1,61] However, with respect to integration the transition from Si or SiGe sheets to WS_2 sheets is however not straightforward. Some of the Si-based processes might be applied to the MX_2 case, but for other processes considerable process tuning and development is required. **Figure 7** illustrates the main challenges using the scaled device from Figure 1 as an example. **Table 2** elaborates further on these challenges, the approach used for Si-based processing, and the suggested approach for MX_2 materials.

A possible SEMulator3D-based virtual process flow schematic for the possible gate-all-around stacked MX_2 transistor shown in Figure 1 is represented in **Figure 8**. In this specific case a replacement gate approach is assumed. Multiple developments will be required for the actual implementation of this integration scheme.

The critical development is the stacked growth or multiple transfers of the MX_2-based multilayer with high intrinsic material quality and mechanical stability (Figure 8a). This will be the case when a replacement gate approach is considered, but also when a direct stack growth is implemented. The development status of the MX_2 growth was described in detail in the preceding section and we believe that a CVD material with a

Table 1. The advantages and disadvantages of horizontal and vertical nanosheet stacking.

Horizontal stacking	Vertical stacking
Electrostatics equivalent for horizontal and vertical 2D nanosheets (unlike for the thicker Si sheet case, edge gating on the 1–2 monolayer thick sheet-end has limited electrical impact)	
• Easily scalable (sheet spacing only limited by the minimal material deposition depth and/or the thickness needed to remove the sacrificial material when a RMG is used).	• Less scalable (sheet to sheet spacing limited by the fin formation, that requires litho or spacer defined patterning).
• Channel deposition possible with direct growth and transferred layers.	• Channel deposition only possible with direct growth.
• No limitation in sheet width.	• Sheet width defined by the supporting fin stability (height limitation).
• Less susceptible for geometric imperfections.	• Perfectly straight supporting fins needed, due to the presence of spacer like etch processes to remove the MX_2 on the horizontal planes in the device.
• CMOS integration possible by stacking N and PMOS devices on top of each other.	• CMOS integration will require selective deposition and or a complex deposition–etch–deposition–etch process.

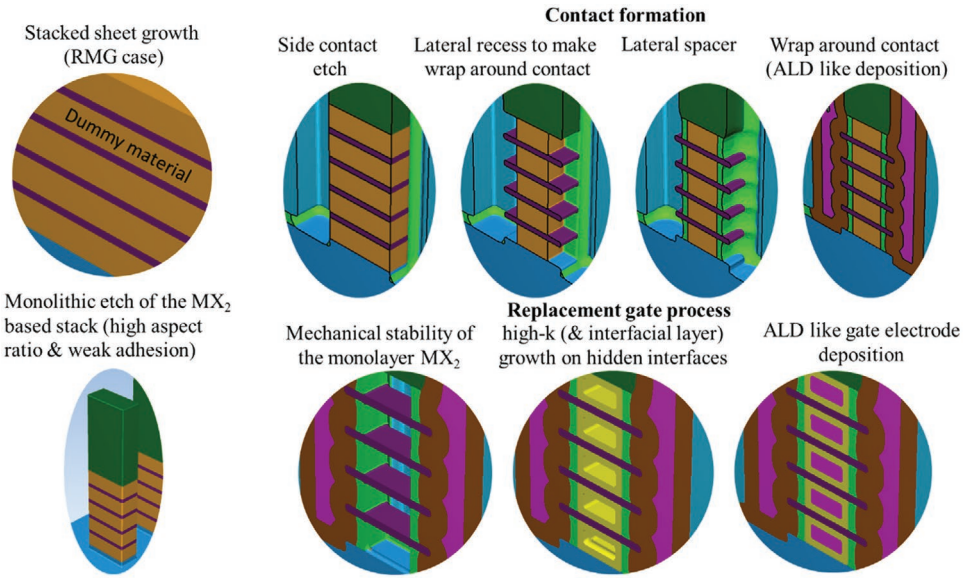

Figure 7. Illustration of the main challenges expected for stacked MX_2 sheet integration based on the example device from Figure 1, using a replacement metal gate approach. The shown area is the circled area in Figure 1 at different processing stages. Note that the single monolayer of MX_2 material is simulated as 2 nm tick for better visibility while it is only ≈0.7 nm thick, rendering the mechanical stability even more perilous. The same color code is used as in Figures 1 and 8.

sufficiently good quality (larger grain size and limited overgrowth) will become available. The MX_2 transfer-based approach would be rather not cost-effective but cannot be fully excluded.

In case a replacement gate approach is considered, a low stress dummy gate material that can be easily removed selective to the MX_2 material, the inner spacer material, and SiO_2, could be used. We also consider the replacement gate approach to be more likely, but dummy material options remain to be screened and tested. In case the final stack is grown directly through a successive deposition of metal gate, gate dielectric, MX_2-channel deposition sequence; the mechanical stress in the stack will be essential to control. We have observed that stress induced MX_2 delamination occurs easily at full wafer level, however this risk is mitigated after patterning in sufficiently

Table 2. The main challenges for stacked sheet integration for Si and their equivalent approach for MX_2-based devices.

Integration challenge	Si-based approach	MX_2-based approach
Stacked sheet growth	Growth of epitaxial Si\SiGe multilayers and selective removal of one of the two, followed by RMG formation	Repeated subsequent deposition or transfer of dummy gate dielectric (material to be identified) and high quality MX_2 channel, combined with an RMG approach OR repeated subsequent deposition or transfer of metal gate, gate dielectric, MX_2, metal gate, gate dielectric, ... (without replacement gate). In this case the mechanical stress during the full wafer deposition must be contained as the van der Waals bonded 2D delaminate easily.
Active etch	Monolithic etch of the Si- and SiGe-based stack.	Monolithic etch of the MX_2-based stack. The mechanical integrity of the etch stack toward delamination around the weaker MX_2 interfaces is to be confirmed.
Lateral spacer between the sheets.	Lateral etch followed by spacer fill and etch back, but other options are also considered.	It is expected that the Si-based sheet approach can also be applied to the MX_2 case, but enhanced selectivity to the ultrathin MX_2 will be requited.
Source and drain contact	Lateral epitaxy on the sheet edges and subsequent contact etches and metal fill. ALD contact materials will be required because of the aspect ratio of the trenches.	In case of MX_2 the contact must directly contact the MX_2, either in a side contact mode or a wrap-around contact mode. The wrap-around contact corresponds to the top contact in the single-sheet case.
Replacement gate process	Dummy gate removal, reactive SiO_2 interfacial layer growth, ALD high-*k* growth, and finally ALD replacement gate metal deposition.	In the replacement gate case, a similar process is expected but: the interfacial layer growth can no longer be reactive as the MX_2 cannot be consumed; and the mechanical strength of the ≈7 Å thick MX_2 sheets after sheet release must be evaluated (at the considered small feature sizes it might be OK).
Direct deposited gate stack process.	Not considered in Si sheet integration.	This option cannot be excluded for the MX_2 case, but a lateral gate metal etch selective to MX_2 will be needed. The advantage of this approach is the guaranteed mechanical integrity of the 2D material.

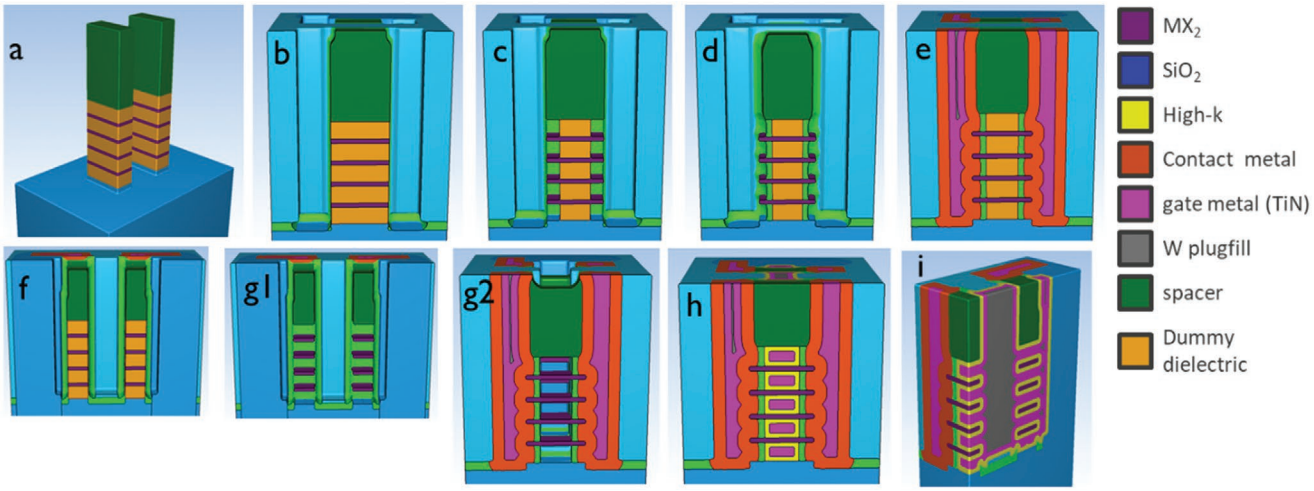

Figure 8. SEMulator3D-based process simulation of the FEOL part of a possible gate all around (GAA) stacked MX_2 transistor. a) Stacked deposition and active etch. b) Contact hole formation (cut through channel of the transistor shown). c) Lateral dummy dielectric recess etch. d) Lateral spacer formation. e) Contact metal deposition and contact hole fill. f) Gate hole formation (cut through the gate and both transistors are shown). g) Dummy dielectric removal (cut through channel and the gate and both transistors shown in (g1) and (g2), respectively). h) High-*k* and RMG fill. i) Final situation before BEOL processing (this figure has both the gate and the channel cut).

small areas.[17] The mechanical integrity of the stack also plays an important role after active etch. At his point, high pillars with lower adhesion around the MX_2 interfaces are formed. One option is to stabilize those pillars in a surrounding matrix (Figure 8b).

Similar to the stacked Si sheet case, lateral inner spacers are used to isolate the contacts from the gate region (Figure 8b–d). We assume much of the Si-based inner spacer development can be reused for the MX_2 channels with some tuning. Compared to the Si integration higher etch selectivity to the MX_2 is required due to the intrinsic atomic thin channel.

Depending on whether side contact only is sufficient or whether the surface of the MX_2 material also needs to be contacted, which is still an open debate, a small lateral recess of the spacer might be needed to form a wrap-around contact. In this example, already a wrap-around contact is assumed. Considering the very small contact sizes and their aspect ratio (Figure 8e,g), the horizontal orientation between the sheets and the intersheet distance of a few nanometers (Figure 8h), the contact metal and gate metal are best deposited with an ALD like technique. Depending on the final metal selection extra process development might also be required. Some metals like TiN and Ru can be deposited by ALD, while for others it is not yet been demonstrated.

For the same reason the high-*k* deposition used in the RMG process is ALD-based (Figure 8h). The typical HfO_2 process used for Si-based processing is already an ALD process and allows the deposition in narrow gaps. Provided the use of HfO_2 on MX_2 does not introduce extra defect states in the channel, this should not be a major complication for MX_2-based stacked channels. More development will be needed for the interfacial layer used prior to high-*k* growth. For Si-based devices part of the Si channel is converted to an OH terminated SiO_2 that serves as a seed for the HfO_2 growth. As explained in the preceding section dedicated to single-sheet transistors this will no longer be the case for MX_2 materials. Among the possible approaches discussed surface functionalization and low damage deposition cannot be used anymore for hidden surfaces as is the case for these stacked MX_2 sheets. Only physisorption and deposition of organic self-assembled monolayers might work, depending on the size of the molecules used for the self-assembly. However, the thermal stability remains an open question.

Critical for the success of the RMG and contact process is the mechanical stability of the single layer free hanging MX_2 after dummy gate removal, and after the contact recess etch (Figure 8c,g). Some build in mechanical stress, introduced during the processing, could further degrade the mechanical integrity of the MX_2 sheets during the dummy gate removal process. The relatively small target gate length of ≈14 nm or shorter and a comparable gate width might provide sufficient mechanical stability for the MX_2 though this needs validation. Besides the mechanical integrity, the chemical integrity of the MX_2 material must be guaranteed, and the removal process should not degrade the quality or modify the single layer MX_2 material.

Many aspects do hence interfere with the choice of the dummy material (growth possibilities for MX_2 growth on the dummy material, growth possibilities of the dummy material on MX_2, selective removal, and limited mechanical stress) render the choice of the dummy gate material a complex exercise and the final choice is hence still pending. The case of a directly grown stacked structure, containing the final materials, is considered as a backup option in case the dummy material cannot be found. This will however come with a new set of challenges, which we will not address here.

4. Conclusion

It is expected that MX_2-based devices will be introduced for high-performance circuits after the Si-sheet-based CFET devices. Full 300 mm fab-based single-sheet devices have been successfully demonstrated and opened the path to

further development of the process flow. The status of technology, focused on fab compatible scaled logic integration was described. For larger feature sizes that could be used for optical applications or BEOL incorporated devices a lift-off-based patterning might still be possible, but for future logic the feature sizes require a more classical damascene integration. Though the final required targets are not yet met, significant progress is made in the key modules: MX_2 deposition, high-*k* growth, and contact engineering. Further process transfer from the research grade lab environment to the fab will require creative engineering solutions and scaled devices will require extra effort.

We believe that for producing CMOS circuits the implementation of MX_2-based N and PMOS devices at different horizontal stack levels is the easiest approach. Combined with the use of stacked sheets this will lead to a stacked multi-sheet CFET like device. Besides the fundamental challenges occurring in the single-sheet case, the stacking will introduce some extra challenges among which the most important are: stacked growth or transfer of MX_2 with sufficient material quality, the choice of an appropriate dummy dielectric and a related removal method without MX_2 damage, the mechanical stability of the monolayer free hanging MX_2 layers, and a 3D compatible high-*k* and metal deposition. These challenges are primarily related to the stacking of the MX_2 layers. For the CFET-related aspects of the process flow, we expect them to be similar to the Si case, and that the related technology can be reused to a large extent.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

integration, MoS_2, MX_2, transition metal dichalcogenides, wafer-scale, WS_2

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