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Design and Mask Optimization Toward Low Dose EUV Exposure

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ABSTRACT

The throughput of extreme ultraviolet lithography (EUVL) is a key factor in the cost of ownership of EUVL patterning at advanced nodes, and low dose exposure is a direct way to increase the wafer throughput. However, low dose exposure typically leads to poor CD uniformity and line-width roughness. In the paper, we investigate low dose EUV exposure via design and mask optimization, and experimentally show the methodology to achieve low dose EUV exposure while maintaining the process performance. The impact of mask CD bias, mask stack and the tonality on the exposure dose and the process performance will be discussed, together with the design retarget and OPC strategy.

Keywords: Low Dose Exposure, EUV Single Patterning, EUV throughput, Logic, DRAM

1. INTRODUCTION

To extend Moore's law, extreme ultraviolet lithography (EUVL) is critical to keep scaling logic devices, which offers a compelling alternative to 193nm-immersion lithography in manufacturing for advanced technology nodes. Nowadays, number of layers using EUVL patterning are increasing significantly to further reduce the cost in high-volume-manufacturing (HVM) at advanced nodes.[1] At imec, the patterning activities of pushing 0.33NA EUV single patterning to its limits for metal layers has been developing and evaluating.[2–5] Furthermore, EUVL has been applied for DRAM production in industry to provide a cost effective solution. However, the occurrence of stochastic printing failures in EUVL patterning is critical at tight pitches.[6–9] To remain lithographic process window at tight pitches, the dose regime in EUVL remains a big challenge.[10] On the other hand, to meet HVM requirement, the key challenge of EUVL patterning is achieving sufficient high wafer throughput, and the most straight forward way is lower EUV exposure dose. These conflicting requirements must be compromised.

Figure 1 shows the exposure dose pentagon trade-off relationship among patterning process, resist materials, wafer stack, mask type and resolution enhancement technique (RET, including source and mask optimization (SMO), optical proximity correction (OPC), and design retarget etc.):

1. **Pattering process**, patterning quality guaranteed by an appropriate process. For example, certain resists (e.g. chemically amplified resist) require post exposure bake (PEB), and dose-to-size could be reduced via longer PEB times.[11] However, long PEB time or high PEB temperature leads to poor local CD uniformity (LCDU), large line-width roughness (LWR) and small overall process window (OPW);[11–13]
2. **Resist materials**, low dose exposure requires high-performance photoresists with high dose sensitivity. However, compared to low dose exposure, the development of resists that can sustain the yield, delivering high resolution and defectivity free processes has higher priority for advanced node. The EUV resist triangle trade-off relationship among resolution, line-edge roughness (LER) and dose/sensitivity (RLS) has been formulated in multiple ways.[14–17] There are contradictory requirements for a resist to have low LER, high dose sensitivity and high resolution simultaneously;
3. **Wafer stack**, resist thickness and underlayers of the wafer stack impacts the light absorption efficiency and resist performance,[18] leading to different dose-to-size;
4. **Mask type**, different mask types result in different light diffraction and image formation, which impacts the used light efficiency. For instance, EUV bright field reflects more light than dark field mask, it could potentially lower the exposure dose. The advanced low-n attenuated phase shift mask (attPSM) has been demonstrated its advantaged to lower the exposure dose both in simulations and experiments;[19]

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5. **Resolution enhancement technique (RET)**, design retargeting and OPC strategy impact on the pattern density on the mask and the optimized source shape. Moreover, the optimized source, design retargeting and OPCed layouts impact the imaging diffraction efficiency.

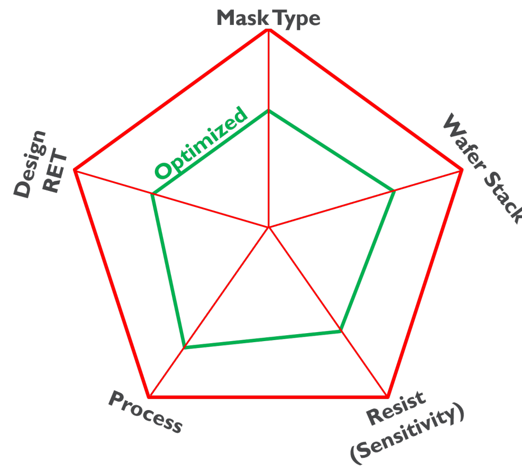

Figure 1: Exposure dose pentagon trade-off relationship among patterning process, resist materials, wafer stack, mask type and resolution enhancement technique (RET, including source and mask optimization (SMO), optical proximity correction (OPC), and design retarget etc.).

Therefore, low dose exposure methodology is a holistic optimization between the final design and the chosen process. In this paper, we take the BKM (Best Known Method) patterning condition at imec and focus on the optimization between RET strategy and mask types, to lower exposure dose while maintains a reasonable OPW. The simulations and experiments of the use case are performed at conditions of imec's 0.33NA NXE:3400 EUV scanner.[20] Section 2 investigates the low dose exposure methodology for logic M1 at pitch 28nm use case. Section 3 introduces the low dose exposure methodology on Memory DRAM at pitch 40nm. Section 4 will provide the summary and future work.

2. LOGIC M1 AT PITCH 28NM USE CASE

Since negative tone development (NTD) process can obtain better imaging quality and OPW,[21,22] which is used in our study of logic M1 use case. Figure 2 shows the schematic of NTD process. The scanner exposes a bright field mask, and the exposed area of the resist is made inert to chemical development. The remaining resist acts as a patterning mask for etch process. After post integration, the resist trench CD is transferred as the metal CD in the device.

2.1 Process Anchor and Design Retarget Optimization

A patterning process always starts with the process anchoring. Figure 3 shows the relationship between the resist trench CD and exposure dose. There are several options for target 14nm resist trench CD at pitch 28nm, either using 12/13nm mask CD with the lower dose or 14nm mask CD with a higher dose. 18% dose reduction can be achieved by -2nm mask CD bias (Fig. 3 (a)).

However, the cross section of metal layer (shown in Fig. 2) is an inverted trapezoid, the metal CD is varying from the top to the bottom, which means the absolute target metal CD does not exist. Slightly metal CD variation does not have any negative impacts on the electric performance of the device, but has the impact on the exposure dose. Figure 3 (a) shows that 1nm larger resist trench CD (metal CD) retarget is able to gain additional 7% dose reduction. Finally, totally 25% dose reduction can be achieved by process anchor and design retarget co-optimization.

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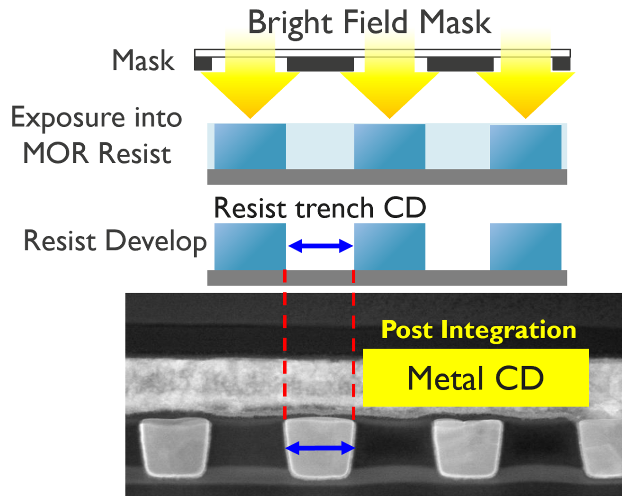
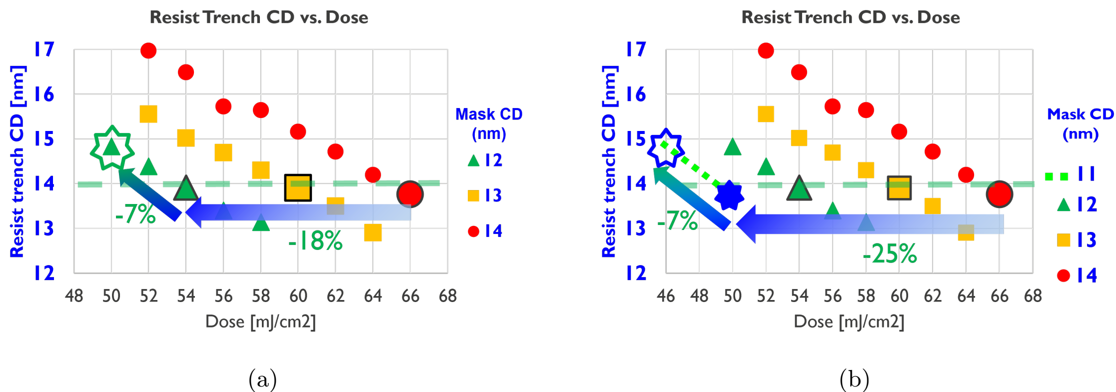


Figure 2: Schematic of negative tone development process.



(a) (b)

Figure 3: The relationship among exposure dose, process anchor and design retarget.

Another option of process anchor optimization is shown in Fig. 3 (b), to further increase mask CD bias directly. As shown in the figure, using 11nm mask CD to target 14nm wafer CD. The same (25%) dose reduction can be achieved by -3nm mask CD bias. Furthermore, additional +1nm resist trench CD retarget can obtain 7% dose reduction. In this way, totally 32% dose reduction can be achieved.

Figure 4 shows an example of the patterning fidelity for Line/Space at pitch 28nm with two different anchor and target options. These two options have similar line-width roughness (LWR) and pattern fidelity, however, the left anchor option delivers us $\sim$ 20% lower dose EUV exposure.

2.2 SMO and OPC Optimization

The anchor and design retarget optimization in Section 2.1 only considers the patterning printability at pitch 28nm. However, lithographic patterning process typically deal with various configurations of Line/Space and Tip-to-Tip (T2T) patterns. As shown in Figure 5 (a), an imec N3 random logic design clip with design retarget, which contains dense, isolated, semi-isolated with symmetric or asymmetric context of Line/Space and T2T. To evaluate the mask CD bias impacts on the OPW, the red cutlines are placed across this design clip. The OPW can be obtained by overlapping the process window of each cutline. And the fitting ellipses is used to compute exposure latitude (EL) and depth of focus (DoF) of the OPW.

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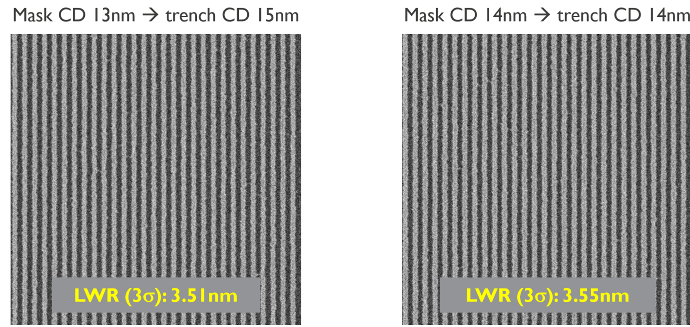
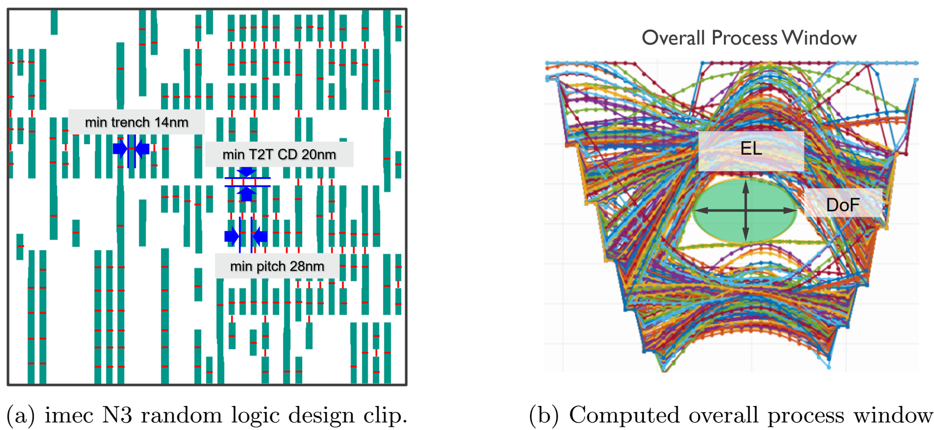


Figure 4: Patterning fidelity of Line/Space at pitch 28nm with two different anchor and target options, and the line-width roughness (LWR) value is only for the comparison purpose.



(a) imec N3 random logic design clip.

(b) Computed overall process window.

Figure 5: imec N3 random logic design clip and the computed overall process window (OPW): minimum pitch is 28nm, the trench CD variations are between 14nm for dense features, and up to 18nm for isolated ones; the minimum T2T CD is 20nm. The red cutlines are used for OPW evaluation.

Figure 6 shows the OPW variation with respect to different anchor mask CD bias proposed in Section 2.1. The computed OPW is decreasing with respect to the large mask CD bias. Notably, there is a large EL and Image Log-Slope (ILS) decreasing at -3nm mask CD bias, which increases the risk of stochastic failures during patterning. To enable low dose exposure with large mask CD bias, an uniform design is very helpful to simplify SMO/OPC strategy and enlarge obtained OPW.

Overall Process Window @Target CD 14nm

	Mask Bias(nm)	EL (%)	DoF(nm)	ILS(1/um) [Min, Max]
Lower dose	-3	8.8	77	[89, 145]
	-2	11.3	83	[104, 153]
	-1	11.5	80	[105,160]
Higher dose	0	13.0	81	[106, 165]

Figure 6: Overall process window variation with respect to different mask CD bias proposed in Section 2.1.

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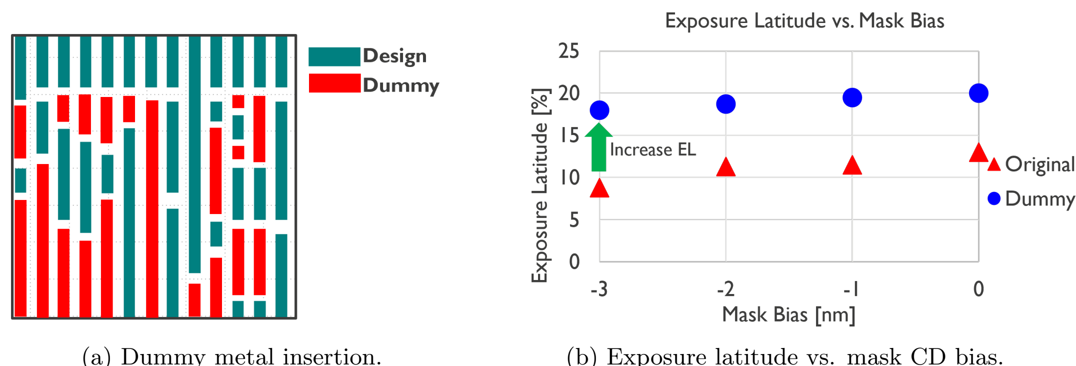
Dummy metal insertion is a strategy that is used in DUV lithography patterning to achieve a highly uniform density of design layout.[23] Figure 7 (a) shows the clip of dummy metal insertion, which is significantly simplified the feature configurations. Figure 7 (b) shows the EL improvement by inserting dummy metals with respect to the non-dummy metal version. Dummy metal insertion delivers much higher EL with respect to non-dummy metal version, the EL is around 18% at -3nm mask CD bias. The electrical test demonstrates the capacitance increase remains acceptable with dummy metal insertion.[2,5]



(a) Dummy metal insertion. (b) Exposure latitude vs. mask CD bias.

Figure 7: Dummy metal insertion clip (a) and the impact of mask CD bias on the exposure latitude (b).

2.3 Brief Summary

The same excises are also performed on the low-n attPSM, however, there is no further dose reduction observed for metal layer use case. Figure 8 briefly summarize the low dose exposure methology on metal layer use case. With respect to the reference anchor point (binary pitch 28nm, using mask CD 14nm to print wafer CD 14nm), the totally 32% dose reduction can be achieved by anchor mask CD and design optimization.

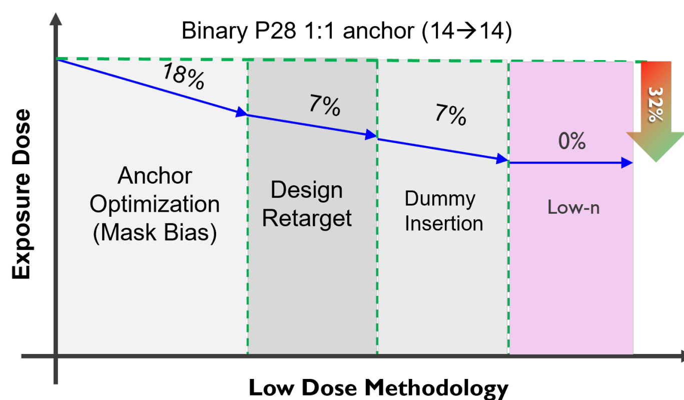


Figure 8: Low dose methology via anchor, design retarget and OPC co-optimization for metal layer use case.

3. MEMORY DRAM AT PITCH 40NM

EUVL has been introduced for DRAM patterning to overcome technological challenges in cell scaling. To have a good control of stochastic effects, a higher dose is required, this is cause of low throughput. Therefore, it is more critical to lower exposure dose for DRAM patterning. Figure 9 shows the design clip of pitch 40nm contact hole. Compared to metal design shown in Fig. 5, it is rather simpler and uniform. Therefore, the same methodology of OPC or design optimization for metal layer do not help to lower the exposure dose. However, there are a few options we can optimize:

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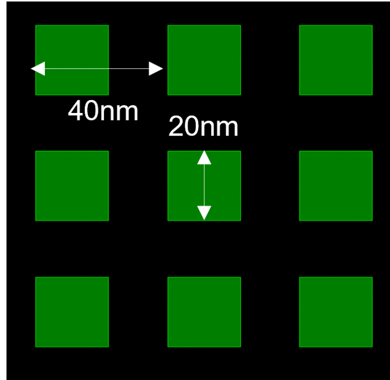

Figure 9: Design clip of pitch 40nm contact hole.

1. Mask CD bias together with SMO anchor optimization;
2. Mask stacks optimization, we compare low-n attPSM vs. standard Ta-based binary mask in this paper;
3. Mask tonality optimization, different mask tonality has different impact on the light reflective efficiency, thus impacts the exposure dose;
4. Novel design, the shape of contact hole can be further optimized, corner rounding, SRAF etc., which impacts the light diffraction efficiency.

However, all these options will impact the exposure dose and the pattern printabity, we need to verify all the aspects with the wafer data.

3.1 Impact of Mask CD Bias

Figure 10 shows the impact of mask CD bias on the exposure dose of binary dark field mask. As shown in Fig. 10, our target CD is 20nm. There are several options to print this target CD, either using mask CD 20nm or 22nm. However, 2nm large mask CD bias is able to reduce the dose by 23%, and slightly enable better LCDU. Additional 7% dose reduction is gained by design CD retarget to 18nm, but the LCDU becomes slightly worse, since the stochastic effect becomes sever for smaller features.

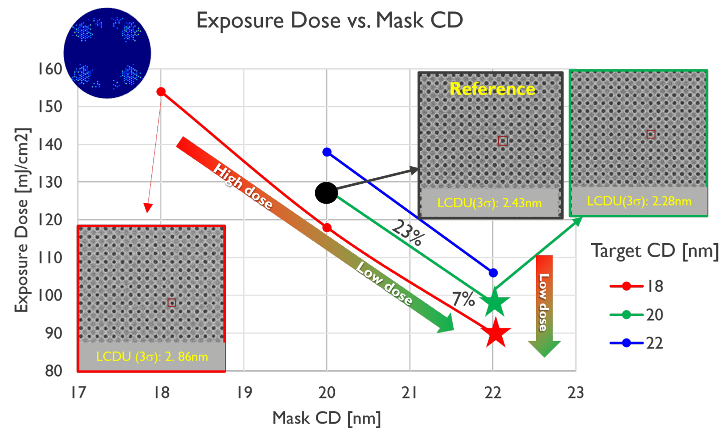

Figure 10: Impact of mask CD bias on the exposure dose for binary dark field mask. LCDU is not measured by BKM, and only used for comparison.

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3.2 Impact of Mask Type

Figure 11 shows the impact of mask CD bias on the exposure dose when using dark field low-n attPSM. 8% dose reduction can be achieved by switching from dark field binary mask to low-n attPSM. Moreover, the dark field low-n attPSM enables larger mask CD bias, additional 28% dose reduction can be achieved by +8nm mask CD bias. As shown in the figure, large mask CD bias of dark field low-n attPSM delivers better LCDU as well.

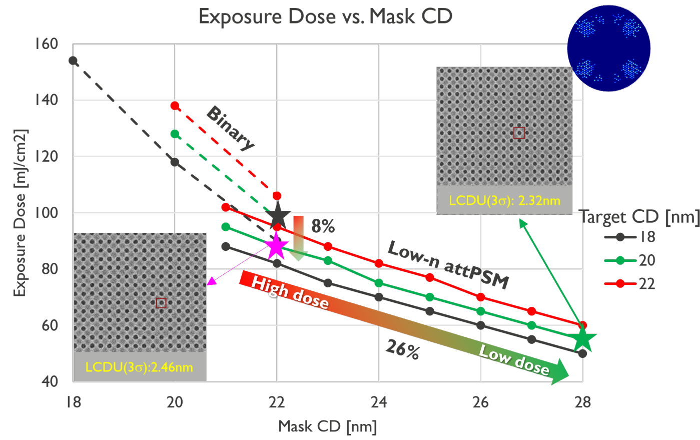

Figure 11: Design clip of pitch 40nm contact hole, dotted lines are the results of binary mask, solid lines are the results of low-n attPSM. LCDU is not measured by BKM, and only used for comparison.

Figure 12 shows the NILS trend versus mask CD bias for targeting 20nm wafer CD. The sub-figure in the top left is the source that is used for the wafer data evaluation both for dark field binary mask and low-n attPSM. The solid lines in the figure shows the corresponding NILS with respect to different mask CD. The NILS of the dark field binary mask is decreasing as the mask CD bias becoming larger, while NILS of dark field low-n attPSM is increasing first and then decreasing. The dotted lines shows a dedicated SMO at each point is able to push the NILS slightly higher. The sources shown on the right side of the figure shows a larger mask CD bias slightly impacts the source shape. To have a better process performance with large mask CD bias, a dedicated source is required.

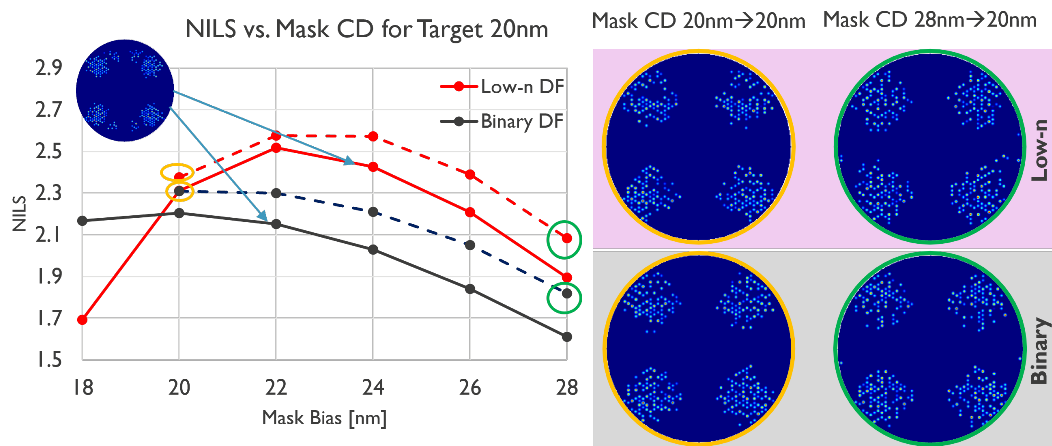

Figure 12: NILS trend vs. mask CD bias for targeting 20nm wafer CD using dark field low-n attPSM and binary mask.

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3.3 Impact of Mask Tonality

Figure 13 compares the low-n attPSM tonality impact vs. different mask CD. Bright field low-n attPSM is able to further lower the dose with poor LCDU. To enable a good LCDU, a large mask CD bias is needed. Figure 14

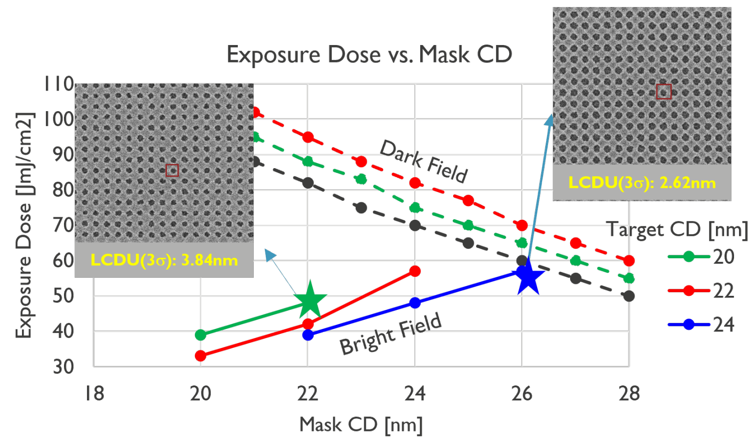

Figure 13: Design clip of pitch 40nm contact hole. LCDU is not measured by BKM, and only used for comparison.

shows the NILS comparison between binary mask and low-n attPSM for both dark field and bright field mask tonality. Both dark field and bright field low-n attPSM could deliver better NILS with respect to the standard binary mask with large positive mask CD bias. The dark field low-n attPSM has the highest NILS among all the four configurations. However, Figure 13 shows that larger mask CD bias of bright field low-n attPSM delivers similar exposure dose as the dark field low-n attPSM. Therefore, switching mask tonality does not reduce the exposure dose, the process impact needs to be considered as well.

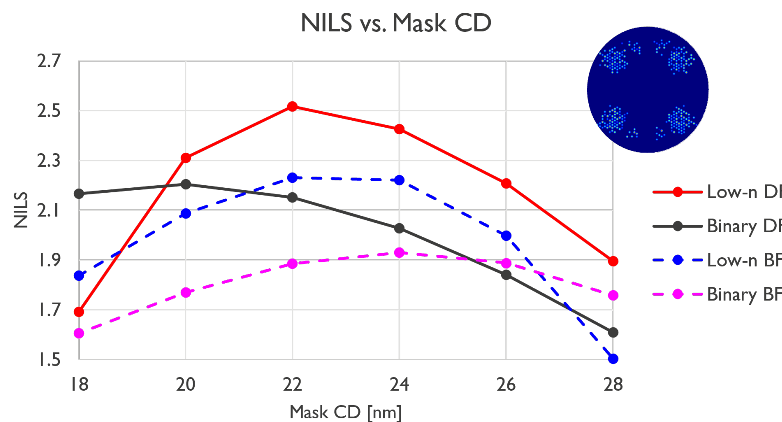

Figure 14: NILS comparison between binary mask and low-n attPSM for both dark field and bright field mask tonality (DF dark field; BF: bright field).

3.4 Brief Summary

Figure 15 briefly summarizes the low dose exposure methology of DRAM use case. We only consider using dark field mask for DRAM capacitor patterning. The dark field binary mask with the optimized mask CD bias

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enables 23% dose reduction. Design retarget enables 7% further dose reduction. On the other hand, by using low-n attPSM with optimized mask CD bias could enable additional 34% dose reduction directly without considering design retarget. Therefore, totally 57% dose reduction achieved without considering any design optimization.

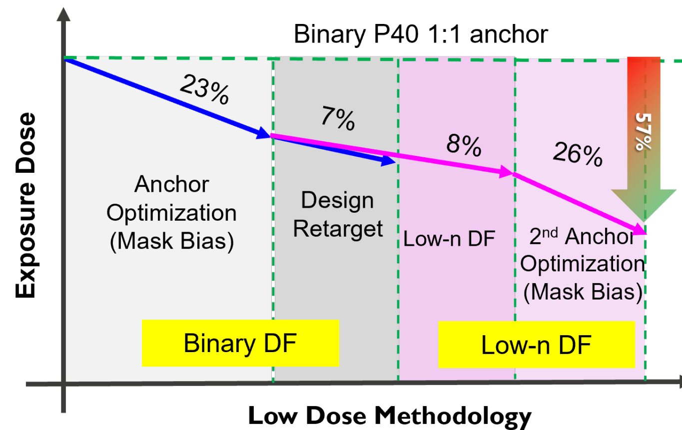

Figure 15: Low dose methology via anchor and mask type co-optimization for DRAM use case (DF: dark field).

4. SUMMARY

In this paper, we investigate the methology to enable EUVL low dose exposure through design and mask optimization for both logic and memory designs. Mask CD bias has a significant impact on the exposure dose, optimizing the mask CD bias is able to lower the exposure dose without deteriorate the patterning performance. For logic M1 layer, design retarget and dummy metal insertion could enable further dose reduction down to 32%. However, for memory DRAM capacitor layer, which has a uniform contact holes, there is no much room for playing design retarget and OPC. Instead, an alternative mask stack is employed. The dark field low-n attPSM delivers good image performance with larger mask CD bias, and achieves more than 30% dose reduction with respect to the binary dark field mask by using large mask CD bias. By using low-n attPSM, totally 57% dose reduction achieved.

However, for hexagonal array contact hole design, large mask CD design limited by mask rule check (MRC) of corner-to-corner. Therefore, to enable larger mask CD bias without hitting MRC, rounding corners has been investigated. The experiments show contact hole area is reduced and must be compensated either by a higher exposure dose or by a larger mask CD bias.[24] Therefore, the new designs to avoid the corner-to-corner MRC issue and SRAF insertion to optimize the reflective efficacy are considered. All these designs will be evaluated by SMO and together with wafer data, and the results will be presented.

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